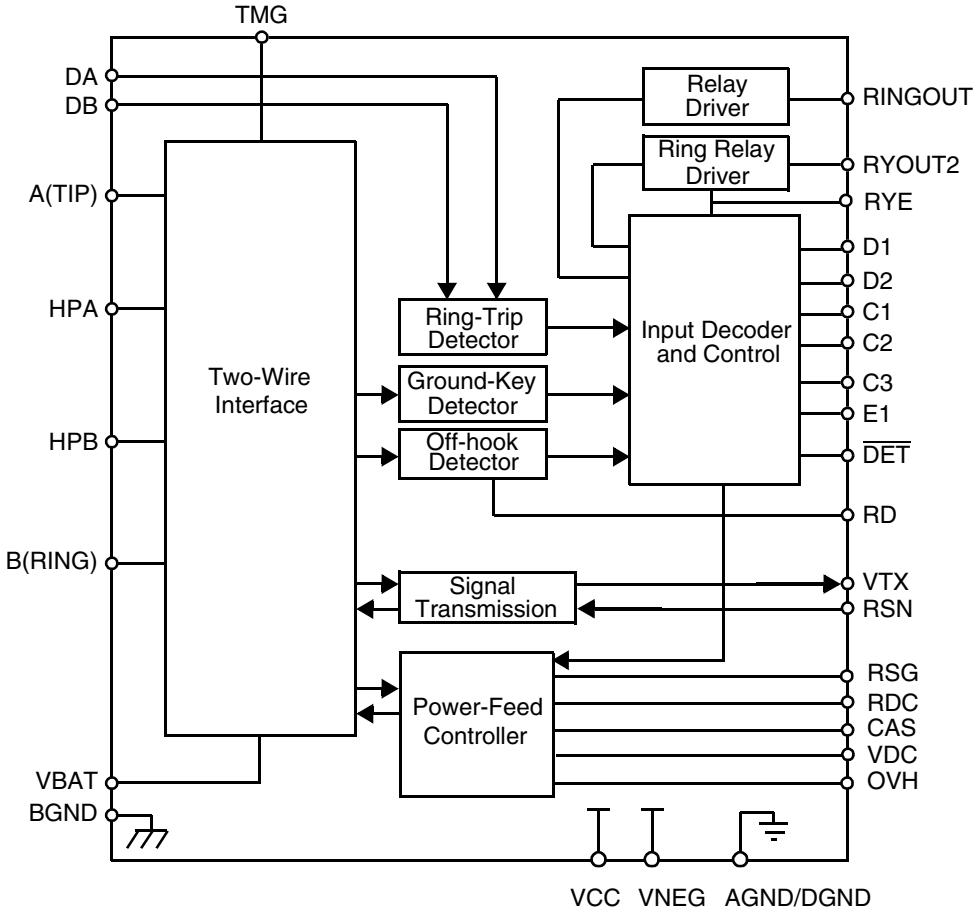
Am7946

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- **Ideal for long loop applications**
- **On-hook transmission**
- **–40 V to –58 V battery operation**
- **On-hook transmission**
- **Internal V_{EE} regulator**
- **Low standby power**
- **On-chip Thermal Management (TMG) feature**
- **Scaled line voltage (VAB) output**
- **Logic selectable for 2.2 V metering or long loop feed**
- **Two-wire impedance set by scaled external impedance**
- **Programmable constant-current feed**
- **Programmable loop-detect threshold**
- **Current gain = 500**
- **Ground-key detector**
- **Tip Open state for ground-start lines**
- **Polarity reversal option available**
- **Three on-chip relay drivers and snubber circuits (32-PLCC only)**

BLOCK DIAGRAM



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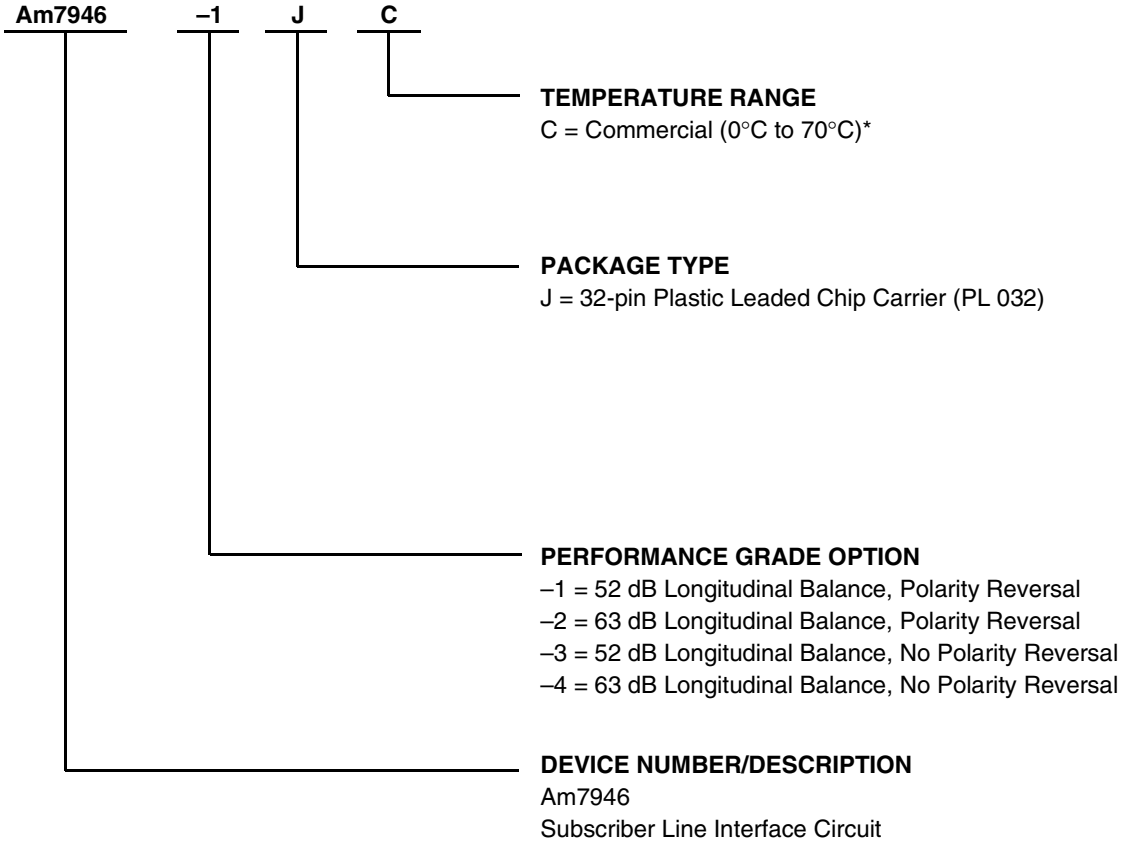
ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am7946	–1 –2 –3 –4	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military–grade products.

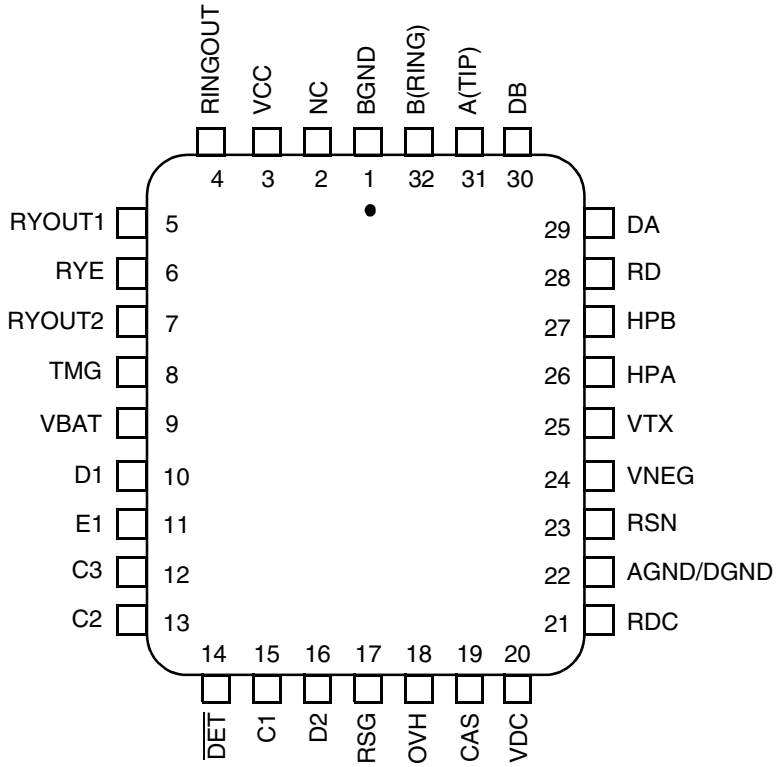
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAMS

Top View

32-Pin PLCC



Notes:

1. Pin 1 is marked for orientation.

2. NC = No Connect

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Inputs	Decoder. SLIC control pins. C3 is MSB and C1 is LSB. TTL compatible.
CAS	Capacitor	Anti-Saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
D2–D1	Input	Relay Driver Control. D2–D1 control the relay drivers RYOUT1 and RYOUT2. A logic Low on D1 activates the RYOUT1 relay driver. A logic Low on D2 activates the RYOUT2 relay driver. TTL compatible.
DA	Input	Ring-Trip Negative. Negative input to ring-trip comparator.
DB	Input	Ring-Trip Positive. Positive input to ring-trip comparator.
DET	Output	Switchhook Detector. When enabled, a logic Low indicates that a selected condition is detected. The detect condition is selected by the logic inputs (C3–C1 and E1). The output is open collector with a built-in 15 kΩ pull-up resistor.
E1	Input	Ground-Key enable. A logic High selects the off-hook detector. A logic Low selects the ground-key detector. TTL compatible.
HPA	Capacitor	High-pass filter capacitor. A(TIP) side of the high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor. B(RING) side of the high-pass filter capacitor.
OVH	Input	Overhead voltage control. A logic High enables nonmetering overhead. A logic Low enables 2.2 V metering DC overhead. TTL compatible.
RD	Resistor	Detect resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). The sign of V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver. Open collector driver with emitter internally connected to BGND. This is activated in the ringing state.
RSG	Input	Saturation guard. A resistor from this pin to ground allows the saturation cut in voltage to be increased while maintaining AC transmission overhead voltage.
RSN	Input	Receive summing node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.
RYE	Output	Common emitter of RYOUT1/2. Emitter output of RYOUT1 and RYOUT2. Normally connected to relay ground.
RYOUT1, RYOUT2	Output	(Option) Relay/Switch driver. Open collector driver with emitter internally connected to RYE.
TMG	—	Thermal management. An external resistor connects between this pin and VBAT to offload power dissipation from the Am7946 SLIC. Functions during Normal Polarity and Reverse Polarity states.
VBAT	Battery	Battery supply and connection to substrate.
VCC	Power	+5 V power supply.
VDC	Output	Scaled VAB output. $V_{DC} = \|(V_{AB} / 20)\|$. Range of 0 V to 2.5 V. This output is filtered by C_{HP}.
VNEG	Power	–4.75 V to VBAT negative supply. This pin is the return for the internal VEE regulator.
VTX	Output	Transmit audio. The voltage at this output is equal to the metallic voltage across A(TIP) and B(RING). VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... –55°C to +150°C

V_{CC} with respect to AGND/DGND ..... –0.4 V to +7.0 V

V_{NEG} with respect to AGND/DGND ..... +0.4 V to V_{BAT}

V_{BAT} with respect to AGND/DGND:

Continuous ..... +0.4 V to –80 V
10 ms ..... +0.4 V to –85 V

BGND with respect to AGND/DGND..... +3 V to –3 V

A(TIP) or B(RING) to BGND:

Continuous ..... –70 V to +1 V
10 ms (f = 0.1 Hz) ..... –70 V to +5 V
1 µs (f = 0.1 Hz) ..... –80 V to +8 V
250 ns (f = 0.1 Hz) ..... –90 V to +12 V

Current from A(TIP) or B(RING)..... ±150 mA

RINGOUT or RYOUT1 or RYOUT2 current..... 75 mA

RINGOUT voltage..... BGND to +7 V

RINGOUT transient..... BGND to +10 V

RYE voltage ..... BGND to V_{BAT}

RYOUT1 or RYOUT2 voltage ..... RYE to +7 V

RYOUT1 or RYOUT2 transient ..... RYE to +10 V

DA and DB inputs

Voltage on ring-trip inputs..... V_{BAT} to 0 V
Current into ring-trip inputs..... ±10 mA

C3–C1, D2–D1, E1, OVH

Input voltage .....–0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, continuous,
T_A = 85°C, No heat sink (See note):

In 32-pin PLCC package..... 1.33 W

Thermal Data..... θ_{JA}

In 32-pin PLCC package..... 45°C/W typ

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Device

Ambient temperature ..... 0°C to +70°C*

V_{CC} ..... +4.75 V to +5.25 V

V_{NEG} ..... –4.75 V to V_{BAT}

V_{BAT} ..... –40 V to –58 V

AGND/DGND ..... 0 V

BGND with respect to
AGND/DGND..... –100 mV to +100 mV

Load resistance on VTX to ground ..... 20 kΩ min

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{VTX}, Analog output offset voltage	0°C to +70°C –40°C to +85°C	–35 –40		+35 +40	mV	— 4
Overload level, 2-wire	Active state, OVH = High	2.5			Vpk	2a
Overload level, 2-wire	Active state, OVH = Low	6.0				
Overload level	On hook, R_{LAC} = 600 Ω, OVH = High	1.06			Vrms	2b
Total Harmonic Distortion (THD)	0 dBm +7 dBm		–64 –55	–50 –40	dB	
THD, On hook	0 dBm, R_{LAC} = 600 Ω			–36		5
Longitudinal Performance (See Test Circuit C)						
Longitudinal to metallic L-T, L-4 balance	200 Hz to 1 kHz: –1, –3* Normal polarity –2, –4 Reverse polarity –2 Normal polarity, –2, –4 –40°C to +85°C	52 63 58 58			dB	 4
	1 kHz to 3.4 kHz: –1, –3* Normal polarity –2, –4 Reverse polarity –2 Normal polarity, –2, –4 –40°C to +85°C	52 58 54 54				 4
Longitudinal signal generation 4-L	200 Hz to 800 Hz normal polarity	40				
Longitudinal current per pin (A or B)	Active or OHT state	27	35		mArms	
Longitudinal impedance at A or B	0 to 100 Hz		10	35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	R_{LDC} = 600 Ω +25°C to +85°C R_{LDC} = 600 Ω –40°C to +25°C		+7	+10 +12	dBrnC	— 4
Psophometric weighted noise	R_{LDC} = 600 Ω +25°C to +85°C R_{LDC} = 600 Ω –40°C to +25°C		–83	–80 –78	dBmp	— 4
Insertion Loss and Balance Return Signal (See Test Circuits A and B)						
Gain accuracy 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz, nonmetering 0 dBm, 1 kHz, 2.2 V metering On hook, OHT	–6.22 –6.12 –6.37	–6.02 –5.92 –6.02	–5.82 –5.72 –5.67	dB	 4
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz, nonmetering 0 dBm, 1 kHz, 2.2 V metering On hook, OHT	–0.20 –0.20 –0.35	0 0 0	+0.20 +0.20 +0.35		
Gain accuracy over frequency	300 to 3400 Hz 0°C to +70°C relative to 1 kHz –40°C to +85°C	–0.10 –0.15		+0.10 +0.15		4 4
Gain tracking Relative to 0 dBm	+3 dBm to –55 dBm 0°C to +70°C –40°C to +85°C	–0.10 –0.15		+0.10 +0.15		4 4
Gain tracking, on hook, OHT Relative to 0 dBm	0 dBm to –37 dBm 0°C to +70°C –40°C to +85°C +3 dBm to 0 dBm	–0.10 –0.15 –0.35		+0.10 +0.15 +0.35		4 4 4
Group delay	0 dBm, 1 kHz		3		µs	4, 6

Note:

** Performance Grade*

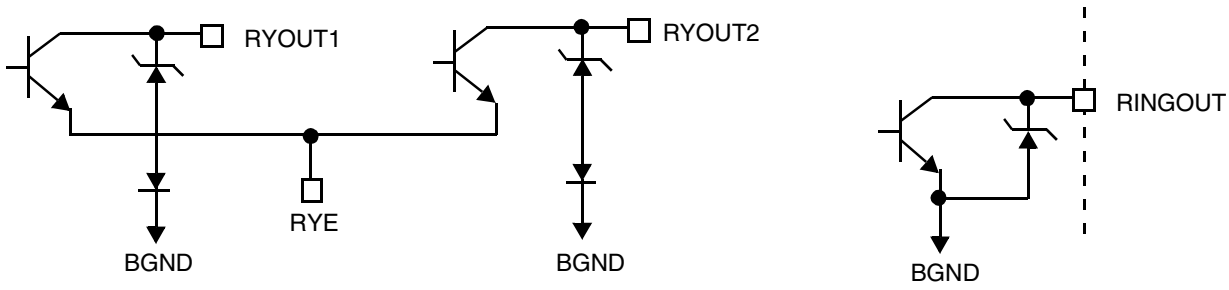
ELECTRICAL CHARACTERISTICS (continued)

Line Characteristics						
I_L, Loop-current accuracy	I_L in constant-current region	$0.915I_L$	I_L	$1.085I_L$		
I_L, Long loops, Active state	R_{LDC} = 1840 Ω, V_{BAT} = –50 V, OVH = Low	20.5				
	R_{LDC} = 2030 Ω, V_{BAT} = –50 V, OVH = High	20.5				
I_L, Accuracy, Standby state	$I_L = \frac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 400}$ T_A = 25°C	$0.8I_L$	I_L	$1.2I_L$	mA	
	Constant-current region	16	22	39		
I_LLIM	Active, A and B to ground OHT, A and B to ground		100 50	130		4
I_L, Open Circuit state	R_L = 0 Ω			100	µA	
I_A, pin A leakage, Tip Open state	R_L = 0 Ω			100		
I_B, pin B current, Tip Open state	B to ground B to V_{BAT} + 6 V		26 15		mA	
V_A, Standby state, ground-start signaling	A to –48 V = 7 kΩ, B to ground = 100 Ω	–7.5	–5		V	4
V_{AB}, Open Circuit voltage	BAT = –50 V	42.75	44.5			8
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC}	50 Hz to 3.4 kHz	30	40		dB	5
V_{NEG}	50 Hz to 3.4 kHz	30	50			
V_{BAT}	50 Hz to 3.4 kHz	28	55			
Effective internal resistance	CAS pin to ground	85	170	255	kΩ	4
Power Dissipation						
On hook, Open Circuit state			30	70	mW	
On hook, Standby state			60	85		
On hook, OHT state			120	180		
On hook, Active state	R_{TMG} = 2.5 kΩ		180	270		
Off hook, Standby state			860	1300		
Off hook, Active state	R_L = 300 Ω, R_{TMG} = 2.5 kΩ		550	800		
Supply Currents, Battery = –58 V						
I_{CC}, On-hook V_{CC} supply current	Open Circuit state Standby state OHT state Active normal state		2.7 3.3 4.9 6.3	3.8 4.4 7.5 8.5	mA	
I_{NEG}, On-hook V_{NEG} supply current	Open Circuit state Standby state OHT state Active normal state		0 0 0.70 0.70	0.1 0.1 1.1 1.1		
I_{BAT}, On-hook V_{BAT} supply current	Open Circuit state Standby state OHT state Active normal state		0.35 1.0 1.9 3.0	1.0 1.5 4.7 5.7		
RFI Rejection						
RFI rejection	100 kHz to 30 MHz, (See Figure F)			1.0	mVrms	4

ELECTRICAL CHARACTERISTICS (continued)

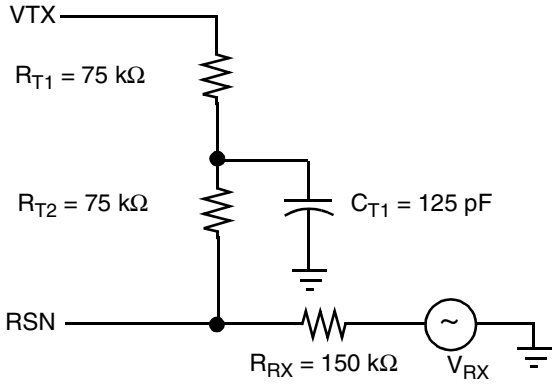
Logic Inputs (C3–C1, D2–D1, E1, OVH)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				
Logic Output ($\overline{DET}$)						
V_{OL}, Output Low voltage	I_{OUT} = 10 mA			1.0	V	
V_{OL}, Output Low voltage	I_{OUT} = 0.8 mA			0.40		
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA	2.4				
Ring-Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6
Loop Detector						
I_T, Loop-detect threshold	R_D = 35.4 kΩ, Active state	$330/R_D$	$375/R_D$	$420/R_D$	mA	
	R_D = 35.4 kΩ, Standby state	$380/R_D$	$430/R_D$	$480/R_D$		
Ground-Key Detector Thresholds						
Ground-key resistive threshold	B to ground	2	5	10	kΩ	
Ground-key current threshold	B to ground		10		mA	
Relay Driver Output (RYOUT1, RYOUT2, and RINGOUT)						
V_{OL}, On voltage (each output)	I_{OL} = 30 mA		+0.25	+0.4	V	
V_{OL}, On voltage (each output)	I_{OL} = 40 mA		+0.35	+0.6		4
I_{OH}, Off leakage (each output)	V_{OH} = +5 V			100	µA	
Zener breakover (each output)	I_Z = 100 µA	6.6	7.9		V	
Zener On voltage (each output)	I_Z = 30 mA		11			

RELAY DRIVER SCHEMATICS



Notes:

1. *Unless otherwise noted, test conditions are BAT = –52 V, V_{CC} = +5 V, V_{NEG} = –5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 28.4 kΩ, R_D = 35.4 kΩ, R_{SG} = 0 Ω to GND, R_{TMG} = 2.5 kΩ, no fuse resistors, C_{HP} = 0.22 µF, C_{DC} = 0.1 µF, C_{CAS} = 0.1 µF, D1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on linecard performance also may be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.*
8. *If |BAT| drops below 50 V, the VAB voltage tracks the battery to preserve transmission capability. Open-circuit VAB can be modified using R_{SG}.*

Table 1. SLIC Decoding

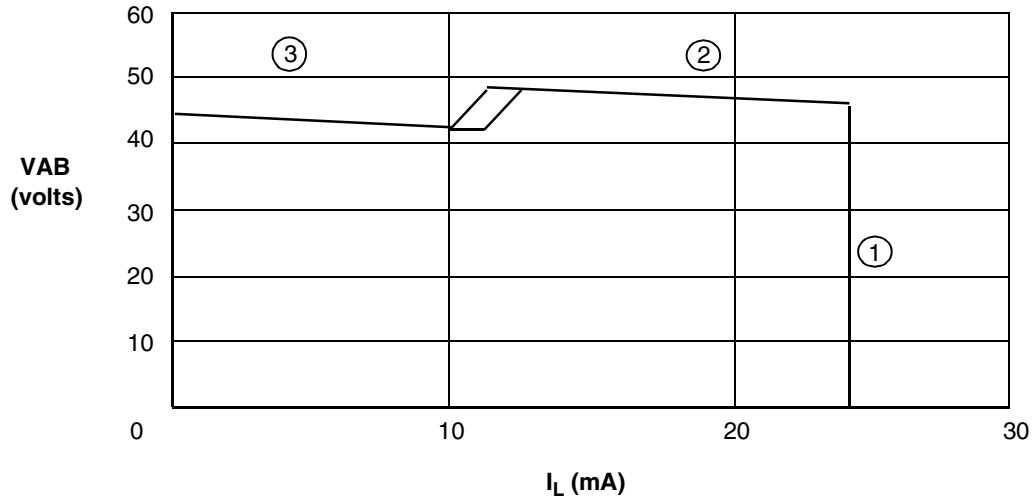
					$\overline{\text{DET}}$ Output	
State	**C3**	**C2**	**C1**	**Two-Wire Status**	**E1 = 1**	**E1 = 0**
0	0	0	0	Open Circuit	Ring trip	Ring trip
1	0	0	1	Ringing	Ring trip	Ring trip
2	0	1	0	Active	Loop detector	Ground key
3	0	1	1	On-hook TX (OHT)	Loop detector	Ground key
4	1	0	0	Tip Open	Loop detector	Ground key
5	1	0	1	Standby	Loop detector	Ground key
6	1	1	0	Active Polarity Reversal	Loop detector	Ground key
7	1	1	1	OHT Polarity Reversal	Loop detector	Ground key

Note:
Only –1 and –2 performance grade devices support polarity reversal.

Table 2. User-Programmable Components

$Z_T = (250(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{1250}{I_L}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_L is the desired loop current in the constant-current region.
$R_D = \frac{375}{I_T},\ C_D = \frac{0.5\ ms}{R_D}$	R_D and C_D form the network connected from R_D to GND and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the filter regulator filter capacitor and f_c is the desired filter cutoff frequency.
Thermal Management Equations (Normal Active, Polarity Reverse Active, and Tip Open States)	
$R_{TMG} \geq \frac{\lvert V_{BAT}\rvert - 6\ V}{I_L}$	R_{TMG} is connected from T_{MG} to V_{BAT} and is used to limit power dissipation within the SLIC in Active and Tip Open states only.
$P_{RTMG} = \frac{(\lvert V_{BAT}\rvert - 6\ V - \lvert I_L \bullet R_L\rvert)^2}{R_{TMG}}$	Power dissipated in the resistor, R_{TMG}, during Active and Tip Open states.
$P_{SLIC} = \lvert V_{BAT} \bullet I_L\rvert - P_{RTMG} - R_L(I_L)2 + 0.12W$	Power dissipated in the SLIC while in Active and Tip Open states.

DC FEED CHARACTERISTICS



$R_{DC} = R_{DC1} + R_{DC2} = 56.8\ k\Omega$

Notes:

1. $|V_{BAT}| < 48$ V, OVH = 1

$$VAB_1 = \frac{1250}{R_{DC}} \bullet R_L$$

$$VAB_2 = 0.818 \bullet |V_{BAT}| + 5.356 - I_L \bullet \frac{R_{DC}}{369}$$

$$VAB_3 = 0.818 \bullet |V_{BAT}| + 2.740 - I_L \bullet \frac{R_{DC}}{359}$$

$|V_{BAT}| < 52$ V, OVH = 0

$$VAB_1 = \frac{1250}{R_{DC}} \bullet R_L$$

$$VAB_2 = 0.818 \bullet |V_{BAT}| + 5.356 - I_L \bullet \frac{R_{DC}}{369}$$

$$VAB_3 = 0.818 \bullet |V_{BAT}| + 2.740 - I_L \bullet \frac{R_{DC}}{359}$$

2. $|V_{BAT}| \geq 48$ V, OVH = 1

$$VAB_1 = \frac{1250}{R_{DC}} \bullet R_L$$

$$VAB_2 = 0.818 \bullet |V_{BAT}| - 2.276 - I_L \bullet \frac{R_{DC}}{369} + \frac{18587 + \left(R_{SG} + \frac{35500}{|V_{BAT}| - 48}\right)}{1777 + 0.131 \bullet \left(R_{SG} + \frac{35500}{|V_{BAT}| - 48}\right)}$$

$$VAB_3 = 0.818 \bullet |V_{BAT}| - 4.894 - I_L \bullet \frac{R_{DC}}{359} + \frac{18587 + \left(R_{SG} + \frac{35466}{|V_{BAT}| - 48}\right)}{1777 + 0.131 \bullet \left(R_{SG} + \frac{35466}{|V_{BAT}| - 48}\right)}$$

a. Load Line (Typical)

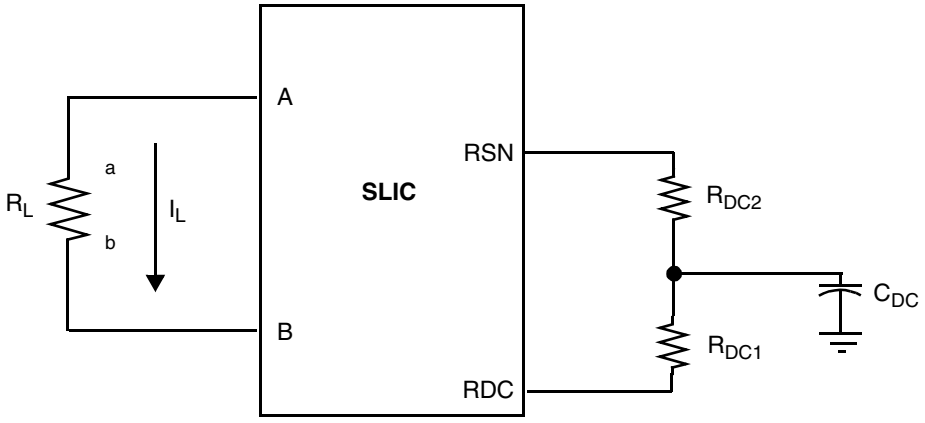
DC FEED CHARACTERISTICS (continued)

3. $|V_{BAT}| \geq 52$ V, OVH = 0

$$VAB_1 = \frac{1250}{R_{DC}} \bullet R_L \text{ where } R_L = R_{LOAD} + R_{FUSE}$$

$$VAB_2 = 0.904 \bullet |V_{BAT}| - 11.031 - I_L \bullet \frac{R_{DC}}{369} + \frac{18587 + \left(R_{SG} + \frac{174000}{|V_{BAT}| - 48}\right)}{1777 + 0.131 \bullet \left(R_{SG} + \frac{174000}{|V_{BAT}| - 48}\right)}$$

$$VAB_3 = 0.904 \bullet |V_{BAT}| - 13.649 - I_L \bullet \frac{R_{DC}}{359} + \frac{18587 + \left(R_{SG} + \frac{174000}{|V_{BAT}| - 48}\right)}{1777 + 0.131 \bullet \left(R_{SG} + \frac{174000}{|V_{BAT}| - 48}\right)}$$

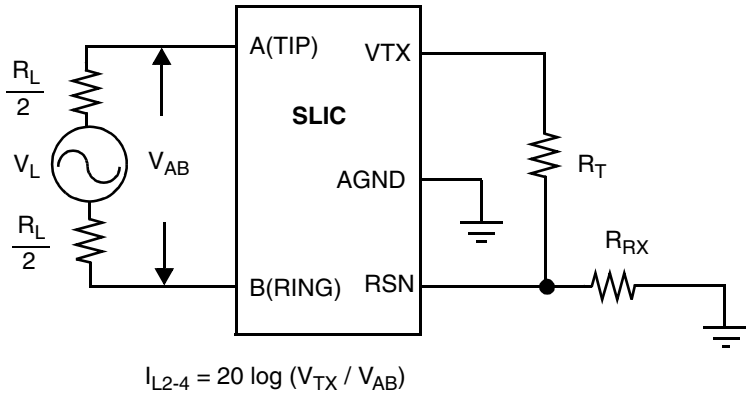


Feed current programmed by R_{DC1} and R_{DC2}

b. Feed Programming

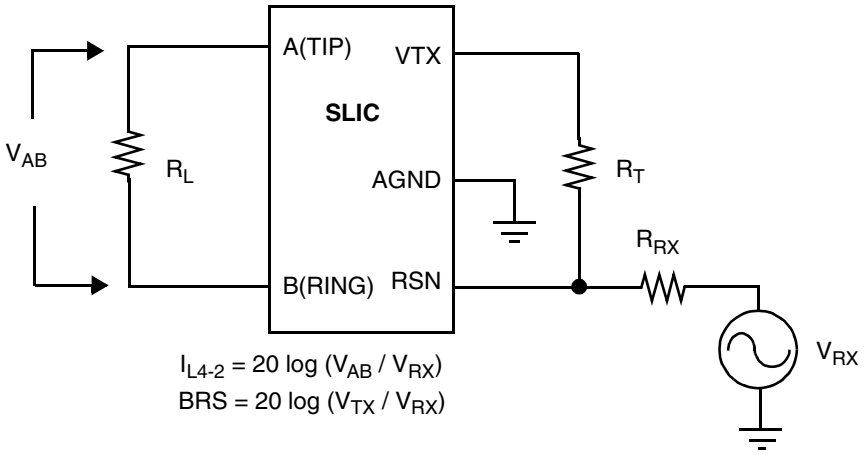
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

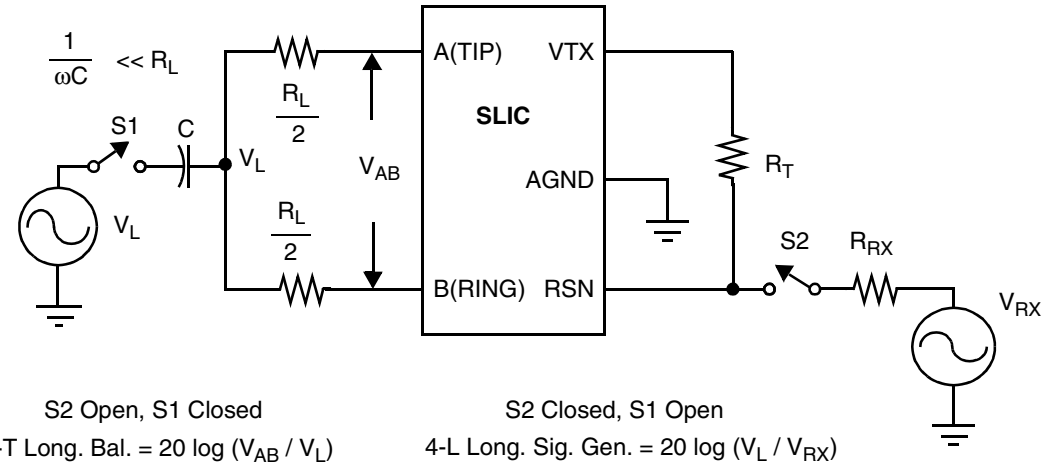
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

L-T Long. Bal. = 20 log (V_{AB} / V_L)

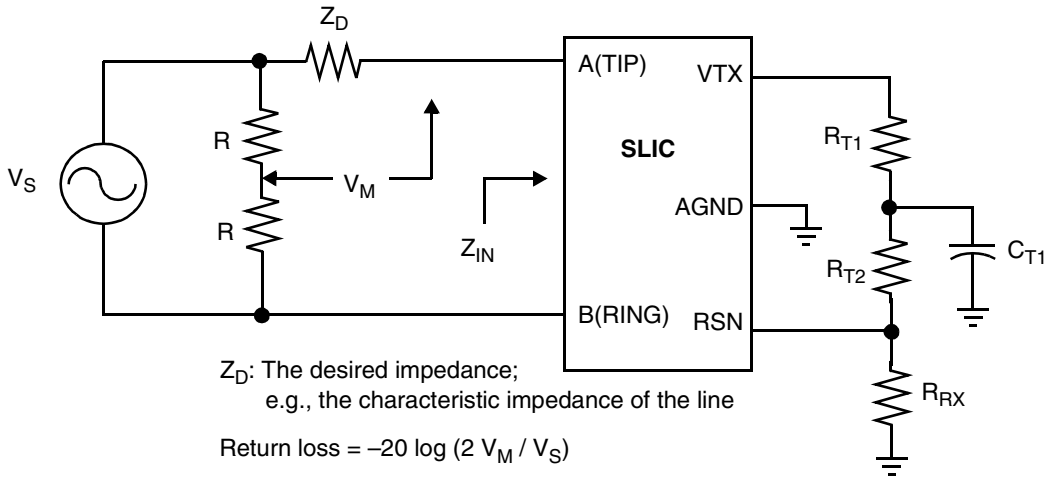
L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open

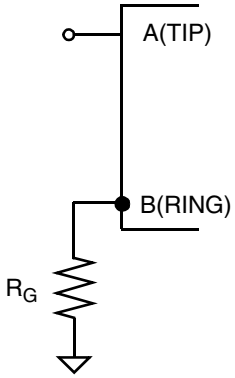
4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance

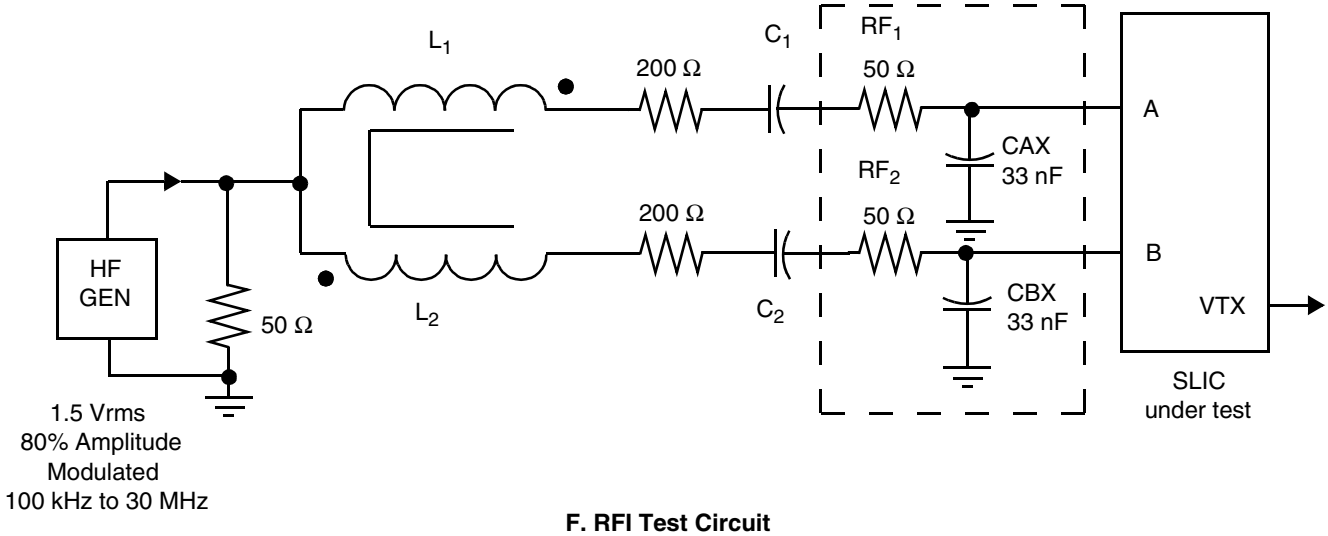
TEST CIRCUITS (continued)



D. Two-Wire Return Loss Test Circuit

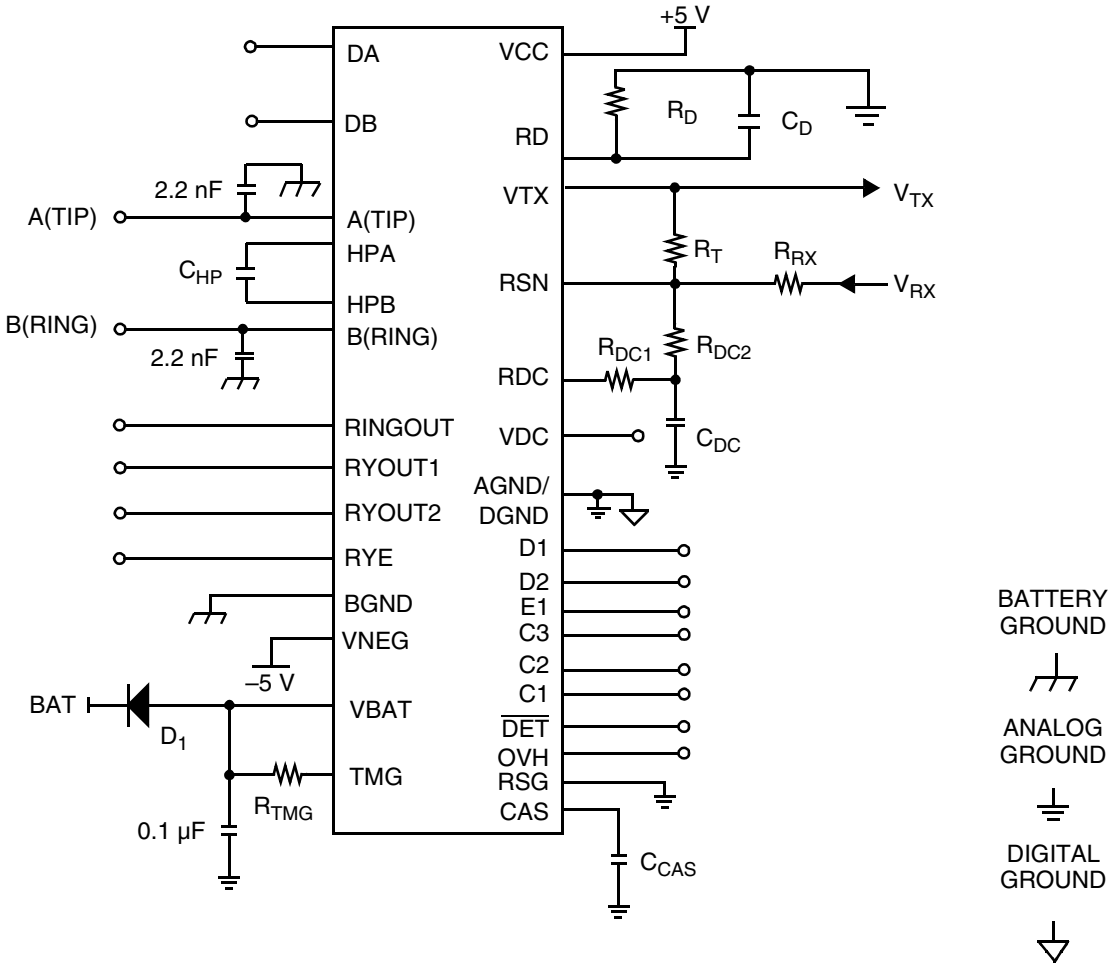


E. Ground-Key Switching



F. RFI Test Circuit

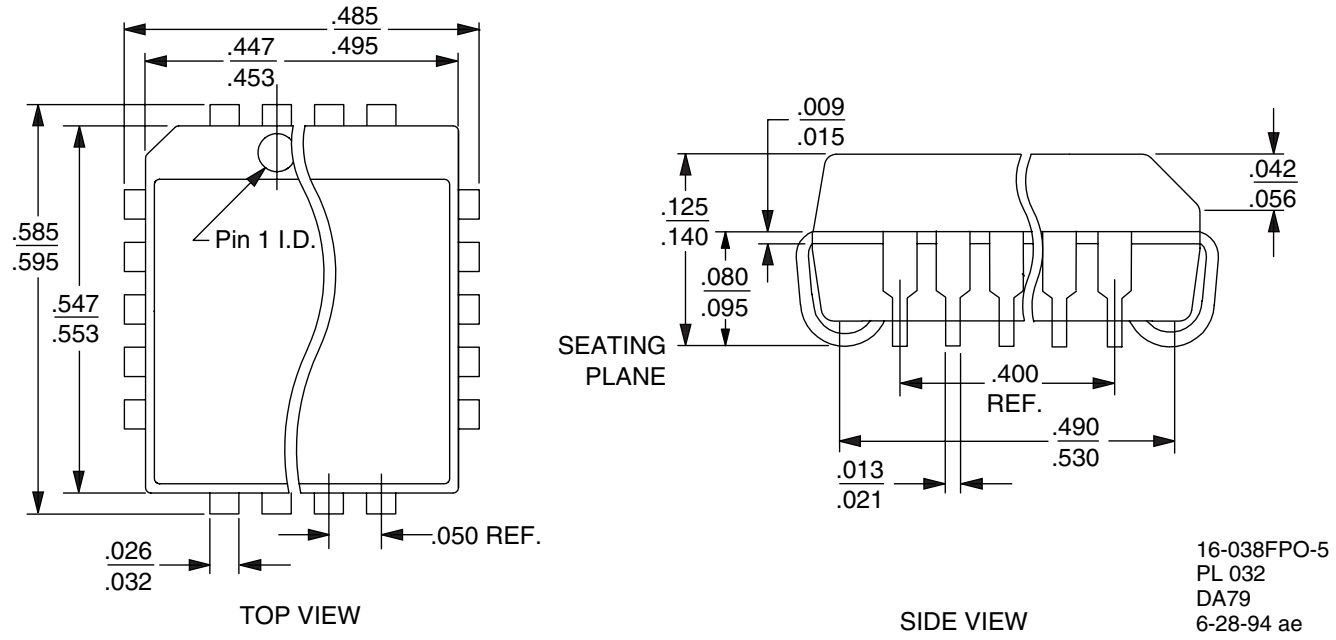
TEST CIRCUITS (continued)



G. Am7946 Test Circuit

PHYSICAL DIMENSION

PL032



REVISION SUMMARY

Revision A to B

- Minor changes were made to the data sheet style and format to conform to Legerity standards.

Revision B to Revision C

- In Table 2, User-Programmable Components, added “Polarity Reverse Active” to the “Thermal Management...” header.
- Minor changes were made to the data sheet style and format to conform to Legerity standards.

Revision C to Revision D

- The physical dimension (PL032) was added to the Physical Dimension section.
- Updated the Pin Description table to correct inconsistencies.

Notes:

Legerity provides silicon solutions that enhance the performance, speeds time-to-market, and lowers the system cost of our customers' products. By combining process, design, systems architecture, and a complete set of software and hardware support tools with unparalleled factory and worldwide field applications support, Legerity ensures its customers enjoy a smoother design experience. It is this commitment to our customers that places Legerity in a class by itself.

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