Winbond Electronics Corp.

ISDN S-CONTROLLER

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1. GENERAL DESCRIPTION

The Winbond's single chip ISDN S/T interface controller (W6690) is an all-in-one device suitable for ISDN Internet access. Three HDLC controllers are incorporated in the chip, one for D channel and the other two for B channels. These HDLC controllers facilitate efficient access to signalling and data services. The PCM codec interface provides voice service or other services. For PC ISA bus add-on card application, the built-in plug and play controller is used for automatic card identification and resource assignment. The plug and play controller can be disabled for traditional ISA card applications. Furthermore, an Intel or Motorola 8-bit micro-controller compatible interface is provided.

2. FEATURES

- Full duplex 2B + D S/T-interface transceiver compatible with ITU-T I.430 Recommendation
  - Four wire operation
  - Received clock recovery
  - Layer 1 activation/deactivation procedures
  - D channel access control
  - Supports multiframe synchronization
- Supports LAPD protocol
  - Flag generation/recognition
  - Bit stuffing (zero insertion/deletion)
  - Frame Check Sequence (FCS) generation/check
  - Maskable address recognition
  - FIFO buffer (2 x 64 bytes)
- Two B channel HDLC controllers
  - Maskable address recognition
  - Bit rate options: 56 or 64 Kbps
  - Transparent or extended transparent mode
  - FIFO buffer (2 × 64 bytes) per B channel
- Two PCM codec interfaces for speech and POTS application
- Various B channel switching capabilities
- Serial EEPROM interface for ISA plug and play configuration
- Glueless ISA plug and play interface for passive card application
- Direct ISA compatible or 8-bit microprocessor interfaces for active card and Terminal Adaptor (TA) applications
- +5 volt power supply
- Advanced CMOS technology
- Low power consumption

- 68-pin PLCC and 100-pin QFP package

3. PIN CONFIGURATIONS

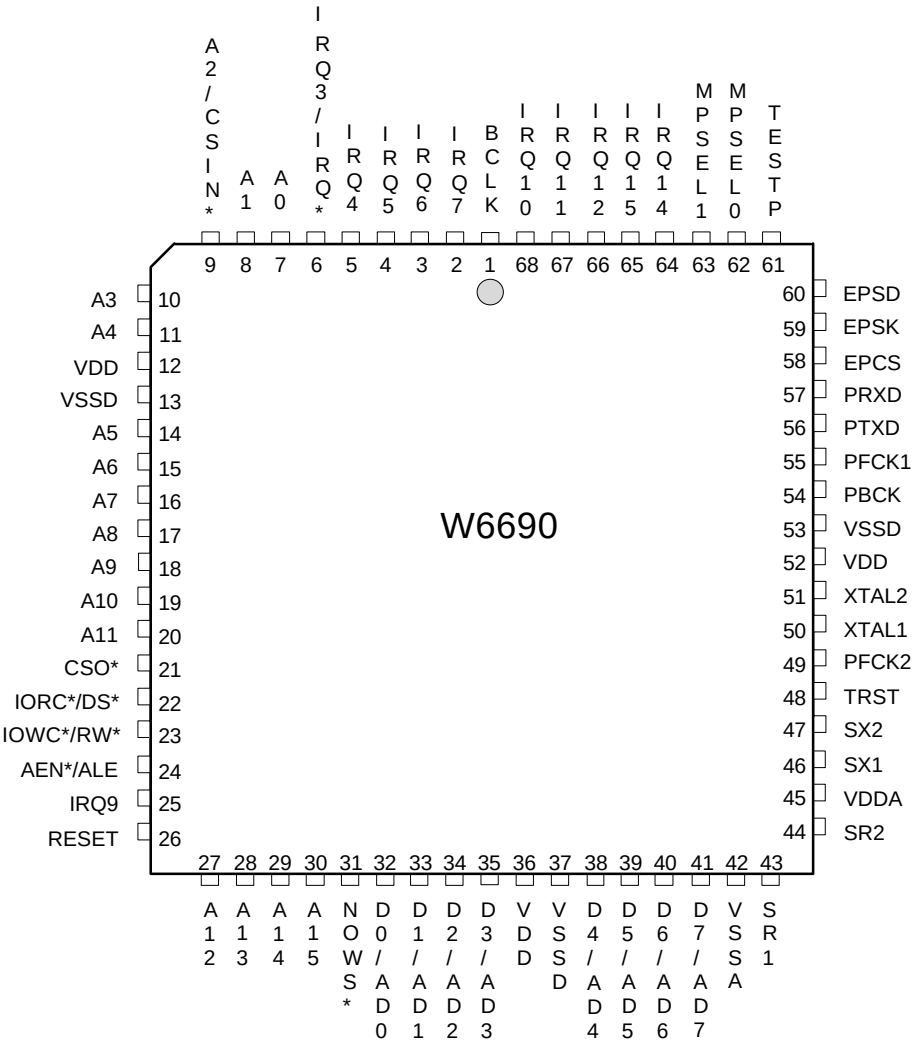


Figure 3.1 PLCC-68

Pin Configurations, continued

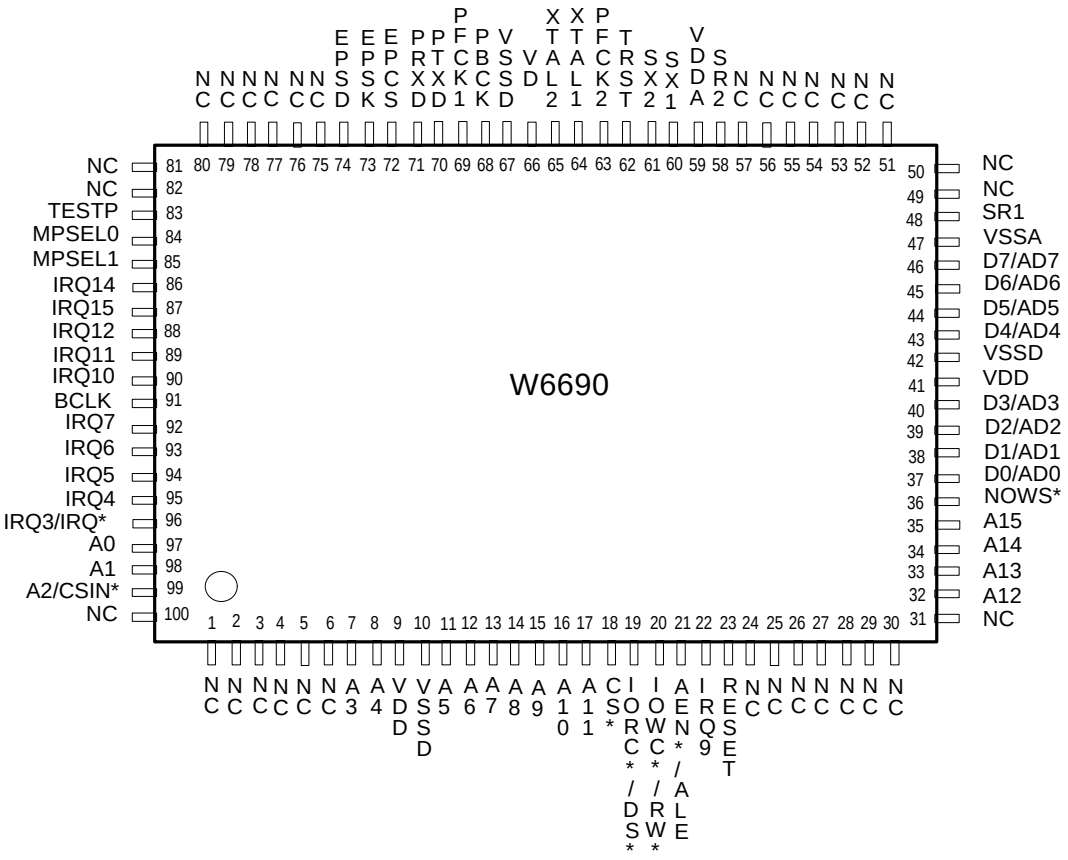


Figure 3.2 QFP-100

4. PIN DESCRIPTION

Table 4.1 W6690 Pin Descriptions

Notation: The suffix "*" indicates an active LOW signal.

PIN NAME	PLCC-68	QFP-100	TYPE	DESCRIPTIONS
MPSEL0 MPSEL1	62 63	84 85	I I	These two pins select the type of micro-processor interface: MPSEL1 MPSEL0 FUNCTION 0 0 PNP ISA mode 0 1 ISA mode 1 0 Intel multiplexed micro-processor mode 1 1 Motorola micro-processor mode
TESTP	61	83	I	Used to enable normal operation (1) or enter test mode (0)
A0 A1 A2/CSIN* A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15	7 8 9 10 11 14 15 16 17 18 19 20 27 28 29 30	97 98 99 7 8 11 12 13 14 15 16 17 32 33 34 35	I	PNP ISA mode: 16 bit ISA addresses. During PNP ISA auto-configuration, A0–A11 are needed. After configuration, A0–A1 are used to select S/T controller's internal registers, and A2–A15 are used by the PNP controller to generate the S/T controller's chip select signal. ISA mode: A0–A1 are used to select S/T controller's internal registers, and A2 is used as the chip select input. Intel microcontroller mode: A2 is used as the chip select input. All other pins are unused. Motorola microcontroller mode: A0–A1 are used to select S controller's internal registers, and A2 is used as the chip select input.
CSO*	21	18	O, 4 mA	PNP ISA mode: This is the chip select signal generated by the internal PNP controller. Other modes: Unused.

4. Pin Description, continued

PIN NAME	PLCC-68	QFP-100	TYPE	DESCRIPTIONS
D0/AD0	32	37	I/O, 12 mA	PNP ISA mode: 8 bit ISA data bus.
D1/AD1	33	38		ISA mode: 8 bit ISA data bus.
D2/AD2	34	39		Intel microcontroller mode: 8 bit data multiplexed with 2 bit address (AD0–AD1).
D3/AD3	35	40		Motorola microcontroller mode: 8 bit data bus
D4/AD4	38	43		
D5/AD5	39	44		
D6/AD6	40	45		
D7/AD7	41	46		
RESET	26	23	I	PNP ISA mode: ISA bus reset signal, active high ISA mode: ISA bus reset signal, active high Intel & Motorola microcontroller mode: Reset signal, active high
TRST	48	62	O, 4 mA	Used if terminal equipment function is enabled. The reset pulse has a pulse width of : - 125 μS when generated by the watchdog timer - 16 mS when generated by exchange awake indication code change
BCLK	1	91	I	PNP ISA & ISA mode: This is the ISA bus clock signal. Its frequency is between 8.333 Mhz and 6 Mhz with a normal duty cycle of 50 %. Intel & Motorola microcontroller mode: Not used.
AEN*/ALE	24	21	I	PNP ISA mode: ISA bus AEN* signal ISA mode: ISA bus AEN* signal Intel microcontroller mode: ALE, address latch enable. The falling edge of this signal is used to latch a valid address. Motorola microcontroller mode: Not used.
IORC*/DS*	22	19	I	PNP ISA mode: ISA bus I/O read signal ISA mode: ISA bus I/O read signal Intel microcontroller mode: Read signal Motorola microcontroller mode: Data strobe. The rising edge marks the end of a valid read or write operation.

4. Pin Description, continued

PIN NAME	PLCC-68	QFP-100	TYPE	DESCRIPTIONS
IOWC*/RW*	23	20	I	PNP ISA mode: ISA bus I/O write signal ISA mode: ISA bus I/O write signal Intel microcontroller mode: Write signal Motorola microcontroller mode: Read/write. A "1" identifies a read operation, a "0" identifies a write operation.
NOWS*	31	36	O,4 mA	PNP ISA mode: ISA bus No Wait signal. Used to shorten a I/O access cycle. Normally, a 8-bit ISA I/O slave cycle spends 6 clock time. The cycle can be reduced to 3 clocks when NOWS* is used. NOWS* is sampled on each falling edge of clock during the time that the ISA command signal is asserted. The cycle ends when NOWS* is sampled LOW. ISA mode: Same as in PNP ISA mode. Intel & Motorola microcontroller mode: Not used.
IRQ3/IRQ* IRQ4 IRQ5 IRQ6 IRQ7 IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	6 5 4 3 2 25 68 67 66 64 65	96 95 94 93 92 22 90 89 88 86 87	OD	PNP ISA mode: IRQ3–7, 9–12, 14–15 are ISA bus interrupt request signals. For the selected IRQ pin, it is high impedance when no interrupt and is driven to LOW for more than 130 nS when interrupt occurs. For other unselected pins, they are open drain. ISA mode: Only IRQ3/IRQ* is used as the interrupt request signal. It is high impedance when no interrupt occurs and is driven to LOW for more than 130 nS when interrupt occurs. Intel & Motorola microcontroller mode: Only IRQ3/IRQ* is used as the interrupt request signal. It is active LOW, level triggered. It is open drain when no interrupt occurs and is driven to LOW when interrupt occurs.
XTAL1	50	64	I	Connection for crystal input or oscillator clock input. The clock frequency is 7.68 Mhz ±100 ppm.
XTAL2	51	65	O, 4 mA	Connection for crystal output. Left unconnected if oscillator clock is used.
SR1	43	48	I	S/T bus receiver input (negative)
SR2	44	58	I	S/T bus receiver input (positive)
SX1	46	60	O	S/T bus transmitter output (positive)
SX2	47	61	O	S/T bus transmitter output (negative)
PFCK1	55	69	O, 4 mA	PCM port 1 frame synchronization signal of 8 KHz
PFCK2	49	63	O, 4 mA	PCM port 2 frame synchronization signal of 8 KHz

4. Pin Description, continued

PIN NAME	PLCC-68	QFP-100	TYPE	DESCRIPTIONS
PBCK	54	68	O	PCM bit synchronization clock of 1.536 MHz
PTXD	56	70	O, 4 mA	PCM transmit data output with 64 kbit/s per port
PRXD	57	71	I	PCM receive data input with 64 kbit/s per port
EPCS	58	72	O,4 mA	Serial EEPROM chip select. This signal is active HIGH.
EPSK	59	73	O,4 mA	Serial EEPROM serial data clock. The frequency is below 250 KHz.
EPSD	60	74	I/O, 4 mA	Serial EEPROM serial data input/output.
V_{DD}	12, 36, 52	9, 41, 66	I	Digital power supply (5V ±5 %)
V_{DDA}	45	59	I	Analog power supply (5V ±5 %)
V_{SSD}	13, 37, 53	10, 42, 67	I	Digital ground
V_{SSA}	42	47	I	Analog ground
NC	-	1–6, 24–31, 49–57, 75–82, 100		Not connected

5. SYSTEM DIAGRAM AND APPLICATIONS

Typical Applications include:

– Highly suitable for ISDN Internet ISA passive S-Card

– ISDN Internet active S-Card

– ISDN TA

The all-in-one characteristic of W6690 makes it excellent for ISDN Internet-access passive card applications. The booming home PC market and powerful CPU capability make it possible to make a very low-cost ISDN Internet access card by using CPU's computing power and user friendly PnP ISA interface. W6690 is designed for this type of scenario. W6690 integrates three HDLC controllers in the chip and interfaces to ISA bus directly. All the commodities needed on the card can be reduced to a one W6690, one crystal, front end transformers and protection circuits, and an optional PCM codec if voice service is required.

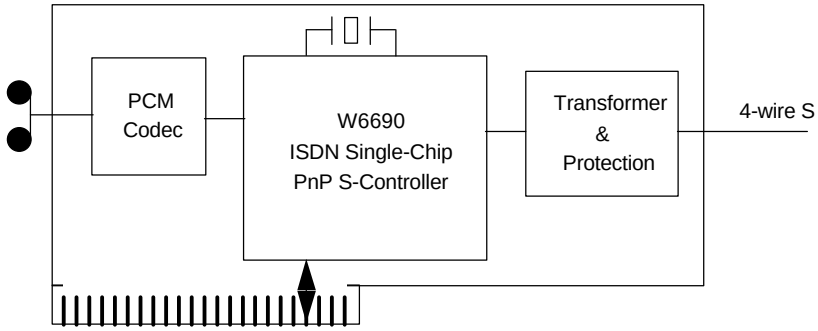


Figure 5.1 ISDN Internet Passive S-card

The bypass-able ISA PnP circuit of W6690 also allows it to be used on active cards and external module applications.

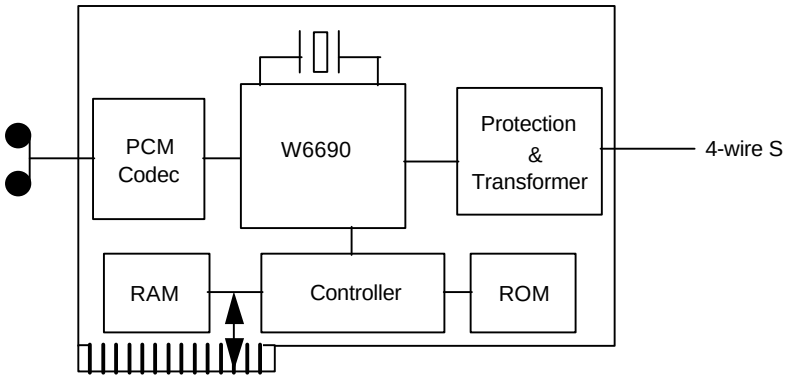


Figure 5.2 ISDN Internal Active S-Card

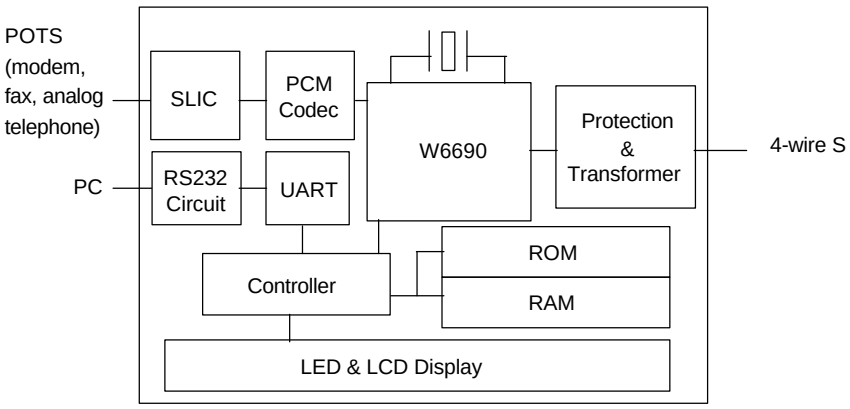


Figure 5.3 ISDN External TA

6. BLOCK DIAGRAM

The block diagram of W6690 is shown in Figure 6.1

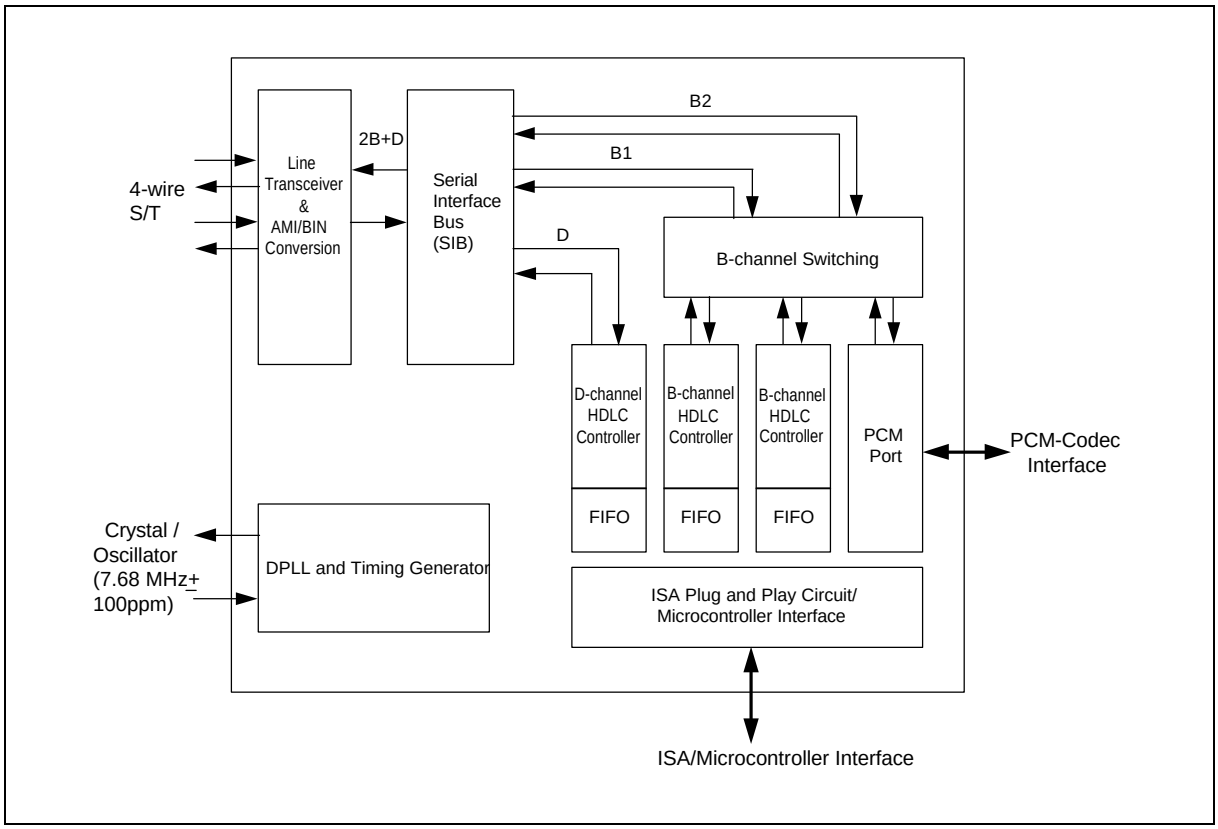


Figure 6.1 W6690 System Diagram

7. FUNCTIONAL DESCRIPTIONS

7.1 Main Block Functions

The functional block diagram of W6690 is shown in Figure 6.1. The main function blocks are :

- Layer 1 function according to ITU-T I.430
- Serial Interface Bus (SIB)
- B channel switching
- PCM port
- D channel LAPD controller
- B channel HDLC controllers (x 2)
- Plug and Play (PNP) circuit / Micro-processor interface

The layer 1 function includes:

– S/T bus transmitter/receiver
– Timing recovery using digital Phase Locked Loop (DPLL) circuit
– Layer 1 activation/deactivation
– D channel access control
– Frame alignment
– Multiframe synchronization
– Test functions

The serial interface bus performs the multiplexing/demultiplexing of D and 2B channels.

The B channel switching determines the connection between layer1, layer 2 and PCM.

The PCM port provides two 64 Kbps clear channels to connect to PCM codec chips.

The D channel HDLC controller performs the LAPD (Link Access Procedure on the D channel) protocol according to ITU-T I.441/Q.921 recommendation.

There are two independent B channel HDLC controllers. They can be used to support HDLC-like protocols such as Internet PPP.

The ISA bus Plug and Play (PNP) circuit implements the necessary Plug and Play functions if enabled. If disabled, W6690 can interface to a ISA bus or a 8-bit micro-processor.

7.2 Layer 1 Functions Descriptions

The layer 1 functions includes :

– Transmitter/Receiver which conform to the electrical specifications of ITU-T I.430
– Receiver clock recovery and timing generation
– Output phase delay (deviation) compensation
– Layer 1 activation/deactivation procedures
– D channel access control
– Frame alignment
– Multiframe synchronization
– Test functions

7.2.1 S/T Interface Transmitter/Receiver

According to ITU-T I.430, pseudo-ternary code with 100% pulse width is used in both directions of transmission on the S/T interface. The binary "1" is represented by no line signal (zero volt), whereas a binary "0" is represented by a positive or negative pulse.

Data transmissions on the S/T interface are arranged as frame structures. The frame is 250 μS long and consists of 48 bits, which corresponds to a 192 kbit/s line rate. Each frame carries two octets of B1 channel, two octets of B2 channel and four D channel bits. Therefore, the 2B+D data rate is 144 kbit/s. The frame structure is shown in Figure 7.1.

The frame begin is marked by a framing bit, which is followed by a DC balancing bit. The first binary "0" following the framing bit balancing bit is of the same polarity as the framing bit balancing bit, and subsequent binary zeros must alternate in polarity.

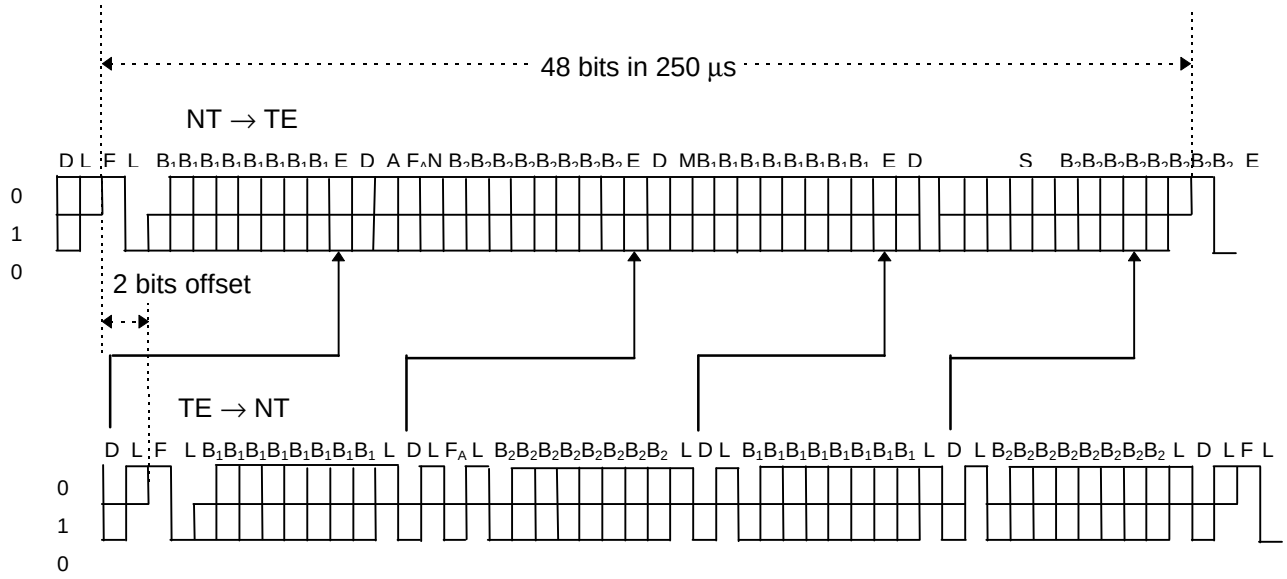
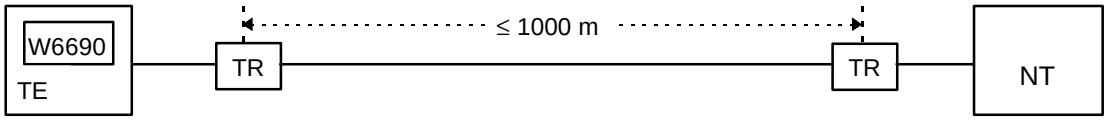
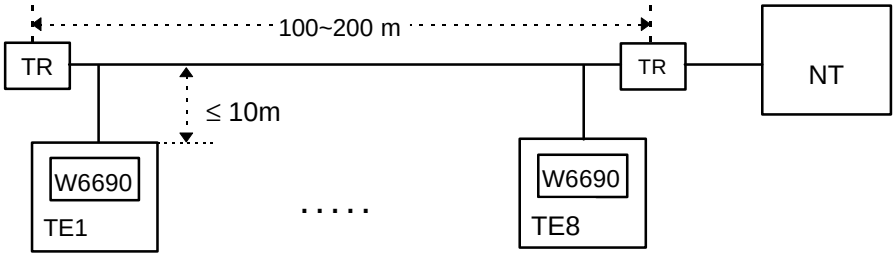


Figure 7.1 Frame Structure at S/T Interface

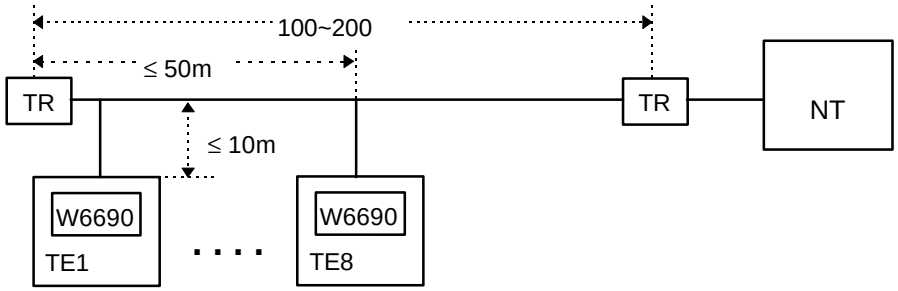
There are three wiring configurations according to I.430: point-to-point, short passive bus and extended pass bus. They are shown in Figure 7.2.



(a) Point-to-point configuration



(b) Short passive bus configuration



(c) Extended passive bus configuration

TR: Terminating Resistor

Figure 7.2 W6690 Wiring Configuration in The Spplications

The transmitter and receiver are implemented by differential circuits to increase signal to noise ratio (SNR). The nominal differential line pulse amplitude at 100 Ω termination is 750 mV, zero to peak. Transformers with 2:1 turn ration are needed at transmitter and receiver for voltage level translation and DC isolation.

To meet the electrical characteristic requirements in I.430, some additional circuits are needed. At the transmitter side, the external resistors (22 to 47 Ω) are used to adjust the output pulse amplitude and to meet the transmitter active impedance (≥ 20 Ω when transmitting binary zeros). At the receiver side, the 1.8 kΩ resistors protect the device inputs, while the 10 kΩ resistors (1.8 kΩ +8.2 kΩ) limit the peak current in impedance tests. The diode bridge is used for overvoltage protection.

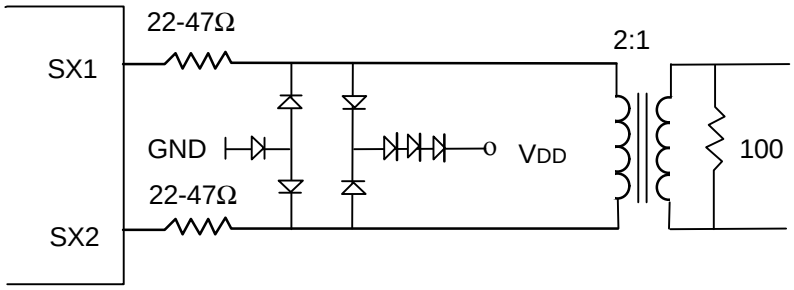


Figure 7.3 External Transmitter Circuitry

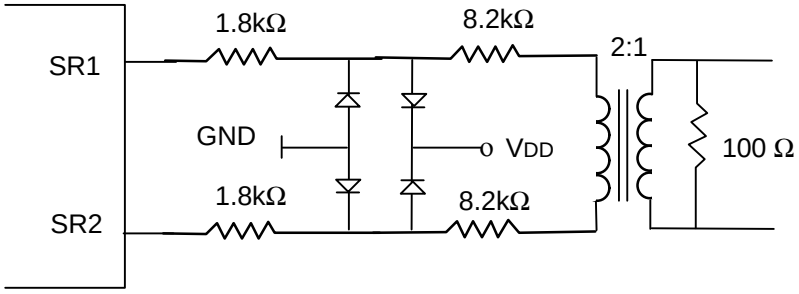


Figure 7.4 External Receiver Circuitry

After hardware reset, the receiver may enter power down state to save power. In thist state, the internal clocks are turned off, but the analog level detector is still active to detect signal coming from the S interface. The power down state is left either by non-INFO 0 signal from S interface or C/I command from micro-processor.

7.2.2 Receiver Clock Recovery And Timing Generation

A digital phase locked loop (DPLL) circuit is used to derive the receive clock from the received data stream. This DPLL uses a 7.68 MHz clock as reference. According to I.430, the transmit clock is delayed by 2 bit time from the receive clock. The "total phase deviation input to output" is -7% to +15% of a bit period. In some cases, delay compensation may be needed to meet this requirement (see OPS1–0 bits in D_CTL register).

Table 7.1 Output phase delay compensation table

OPS1	OPS0	EFFECT
0	0	No phase delay compensation
0	1	Phase delay compensation 260 nS
1	0	Phase delay compensation 520 nS
1	1	Phase delay compensation 1040 nS

The PCM output clocks (PFCK1-2, PBCK) are synchronous to the S-interface timing.

7.2.3 Layer 1 Activation/Deactivation

The layer 1 activation/deactivation procedures are implemented by a finite state machine. The state transitions are triggered by signals received at S interface or commands issued from micro-processor. The state outputs signals to S interface and indication to micro-processor. The CIX register is used by micro-processor to issue command, and the CIR register is used by micro-processor to receive indication.

Some commands are used for special purposes. They are "layer 1 reset", "analog loopback", "send continuous zeros" and "send single zero".

7.2.3.1 States Descriptions And Command/Indication Codes

F3 Deactivated without clock

This is the "deactivated" state of ITU-T I.430. The receive line awake unit is active except during a hardware reset pulse. After reset, once the indication "1111" has been read out, internal clocks will turn off and stay at this state if INFO 0 is received on the S line. The turn off time is approximate 93 mS. The command ECK must be issued to activate the clocks.

F3 Deactivated with clock

This state is identical to "F3 Deactivated without clock" except the internal clocks are enabled. The state is entered by a ECK command. The clocks are enabled approximately 0.5 mS to 4 mS after the ECK command, depending on the crystal capacitances. (It is about 0.5 mS for 12 to 33 pF capacitance).

F3 Awaiting Deactivation

The W6690 enters this state after receiving INFO 0 (in states F5 to F8) for 16ms (64 frames). This time constant prevents spurious effect on S interface. Any non-INFO 0 signal on the S interface causes transition to "F5 Identifying Input" state. If this transition does not occur in a specific time (500–1000 mS), the micro-processor may issue DRC or ECK command to deactivate layer 1.

F4 Awaiting Signal

This state is reached when an activate request command has been received. In this state, the layer 1 transmits INFO1 and INFO 0 is received from the S interface. The software starts timer T3 of I.430 when issuing activate request command. The software deactivates layer 1 if no signal other than INFO 0 has been received on S interface before expiration of T3.

F5 Identifying Input

After the receipt of any non-INFO 0 signal from NT, the W6690 ceases to transmit INFO 1 and awaits identification of INFO 2 or INFO 4. This state is reached at most 50 μS after a signal different from INFO 0 is present at the receiver of the S interface.

F6 Synchronized

When W6690 receives an activation signal (INFO 2), it responds with INFO 3 and waits for normal frames (INFO 4). This state is reached at most 6 mS after an INFO 2 arrives at the S interface (in case the clocks were disabled in "F3 Deactivated without clock").

F7 Activated

This is the normal active state with the layer 1 protocol activated in both directions. From state "F6 Synchronized", state F7 is reached at most 0.5 mS after reception of INFO 4. From state "F3 Deactivated without clock" with the clocks disabled, state F7 is reached at most 6 mS after the W6690 is directly activated by INFO 4.

F8 Lost Framing

This is the state where the W6690 has lost frame synchronization and is awaiting resynchronization by INFO 2 or INFO 4 or deactivation by INFO 0.

Special States:

Analog Loop Initiated

On Enable Analog Loop command, INFO 3 is sent by the line transmitter internally to the line receiver (INFO 0 is sent to the line). The receiver is not yet synchronized.

Analog Loop Activated

The receiver is synchronized on INFO 3 which is looped back internally from the transmitter. The indication 'TI" or "ATI" is sent depending on whether or not a signal different from INFO 0 is detected on the S interface.

Send Continuous Pulses

A 96 KHz continuous pulse with alternating polarities is sent.

Send Single Pulses

A 2 KHz isolated pulse with alternating polarities is sent.

Layer 1 Reset

A layer 1 reset command forces the transmission of INFO 0 and disables the S line awake detector. Thus activation from NT is not possible. There is no indication in reset state. The reset state can be left only with ECK command.

Table 7.2 Layer 1 command codes

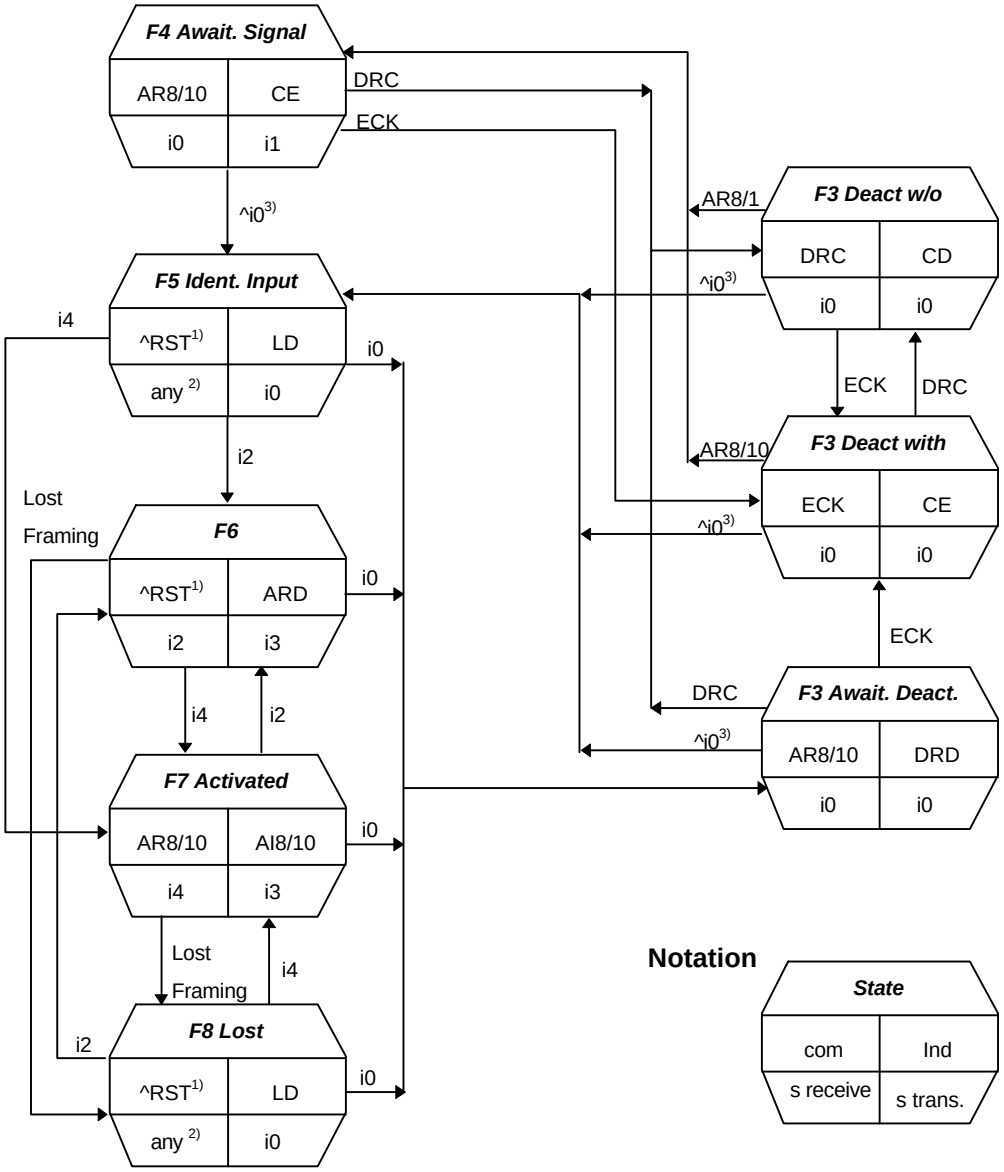
COMMAND	SYM.	CODE	DESCRIPTION
Enable clock	ECK	0000	Enable internal clocks
Layer 1 reset	RST	0001	Layer 1 reset
Send continuous pulses	SCP	0100	Send continuous pulses at 96 KHz
Send single pulses	SSP	0010	Send isolated pulses at 2 KHz
Activate request at priority 8	AR8	1000	Activate layer 1 and set D channel priority level to 8
Activate request at priority 10	AR10	1001	Activate layer 1 and set D channel priority to 10
Enable analog loopback	EAL	1010	Enable analog loopback
Deactivate layer 1	DRC	1111	Deactivate layer 1 and disable internal clocks

Table 7.3 Layer 1 indication codes

INDICATION	SYM.	CODE	DESCRIPTIONS
Clock Enabled	CE	0111	Internal clocks are enabled
Deactivate request downstream	DRD	0000	Deactivation request by S interface, i.e INFO 0 received
Level detected	LD	0100	Signal received, receiver not synchronous
Activate request downstream	ARD	1000	INFO 2 received
Test indication	TI	1010	Analog loopback activated or continuous zeros or single zeros transmitted
Awake test indication	ATI	1011	Level detected during test function
Activate indication with priority class 1	AI8	1100	INFO 4 received, D channel priority is 8 or 9
Activate indication with priority class 2	AI10	1101	INFO 4 received, D channel priority is 10 or 11
Clock disabled	CD	1111	Layer 1 deactivated, internal clocks are disabled

7.2.3.2 State Transition Diagrams

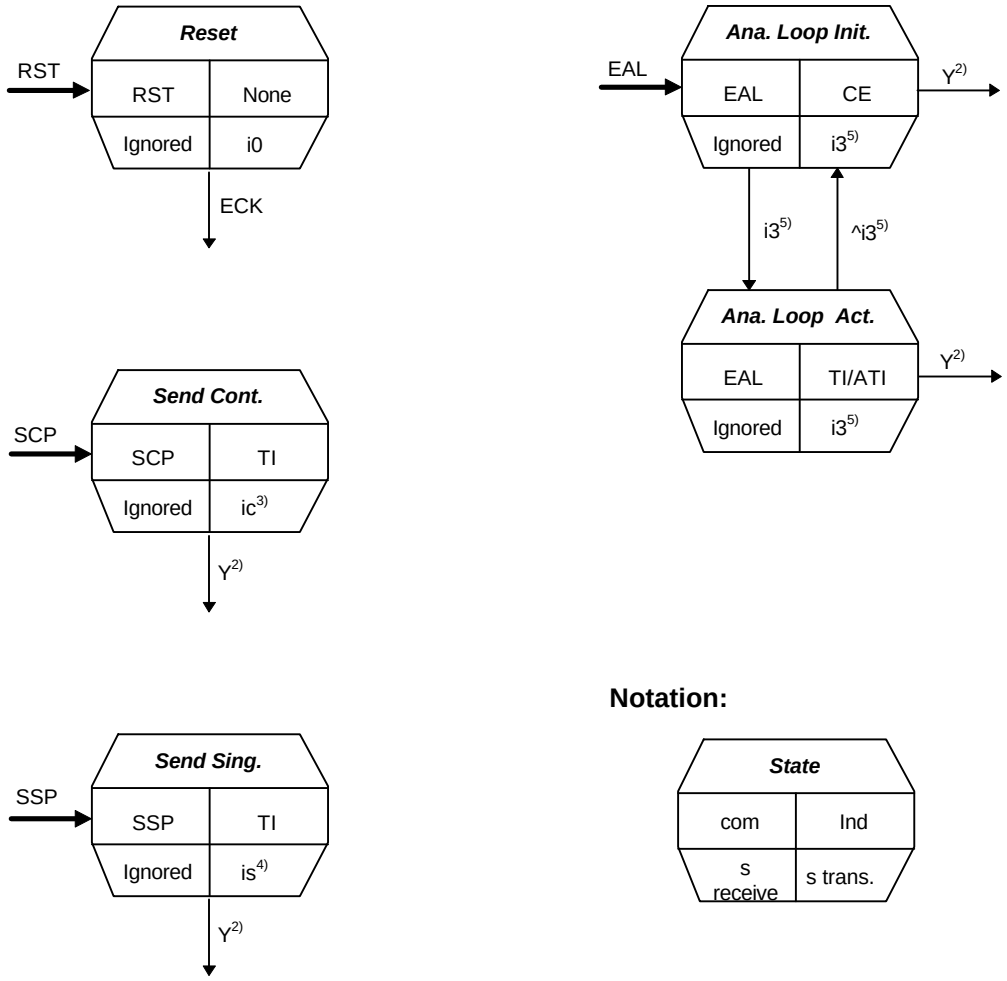
The followings are the state transition diagrams which implement the activation/deactivation state matrix in I.430 (TABLE 5/I.430). The "command" and "s receive" entries in each state octagon keeps the state, the "indication" and "s transmit" entries in each state octagon are the state outputs. For example, at "F3 Deactivated with clock" state, the layer 1 will stay at this state if the command is "ECK" and the INFO 0 is received on S interface. At this state, it provides "CE" indication to the micro-processor and transmits INFO 0 on S interface. A "AR8/10" command causes transition to F4 and non-INFO 0 signal causes transition to F5. Note that the command code writtern by the micro-processor in CIX register and indication code written by layer 1 in CIR register are transmitted repeatedly until a new code is written.



Notes :

1. "^RST" means "NOT layer 1 reset command".
2. "Any" means any signal other than i0, which has not yet been determined.
3. "^i0" means any signal other than i0.

Figure 7.5 Layer 1 Activation/S Diagram - Normal Mode



Notes:

1. RST can be issued at any state, while SCP, SCZ and EAL can be issued only at F3 or F7.
2. Y is one of the commands : ECK, DRC, RST.
3. Continuous pulses at 96 KHz.
4. Isolated pulses at 2 KHz.
5. The INFO 3 is transmitted internally only.

Figure 7.6 Layer 1 Activation/Deactivation State Diagram - Special Mode

7.2.4 D Channel Access Control

The D channel access control includes collision detection and priority management. The collision detection is always enabled. The priority management procedure as specified in ITU-T I.430 is fully implemented in W6690.

A collision is detected if the transmitted D bit and the received echo bit do not match. When this occurs, D channel transmission is immediately stopped and the echo channel is monitored to attempt the next D channel access. The layer 1 module uses an internal signal to inform layer 2 module of the collision condition (DRDY bit goes inactive in CIR register).

There are two priority classes : class 1 and class 2. Within each class, there are normal and lower priority levels.

Table 7.4 D priority classes

	NORMAL LEVEL	LOWER LEVEL
Priority Class 1	8	9
Priority Class 2	10	11

The selection of priority class is via the AR8/AR10 command. The following table summarizes the commands/indications used for setting the priority classes :

Table 7.5 D Priority commands/indications

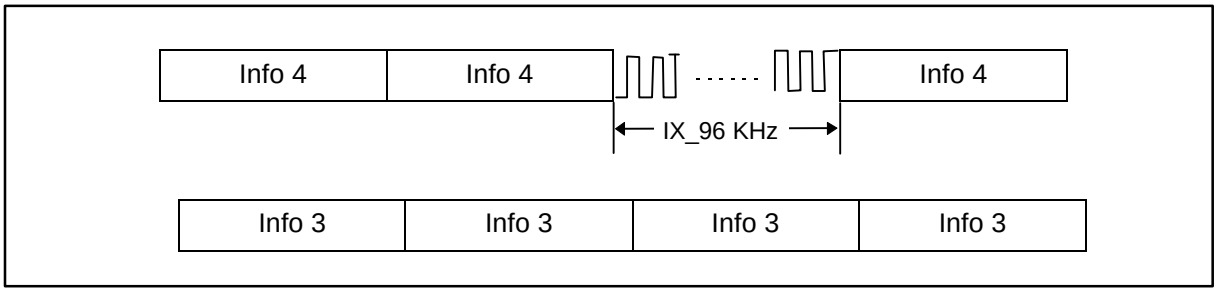
COMMAND	SYM.	CODE	REMARKS
Activate request, set priority 8	AR8	1000	Activation command, set D channel priority to 8
Activate request, set priority 10	AR10	1001	Activation command, set D channel priority to 10
INDICATION	**ABBR.**		**REMARKS**
Activate indication with priority 8	AI8	1100	Info 4 received, D channel priority is 8 or 9
Activate indication with priority 10	AI10	1101	Info 4 received, D channel priority is 10 or 11

7.2.5 Frame Alignment

The following sections describe the behavior of W6690 in respect to the CTS-2 conformance test procedures for frame alignment. Please refer to ETSI-TM3 Appendix B1 for detailed descriptions.

7.2.5.1 FAinfA_1fr

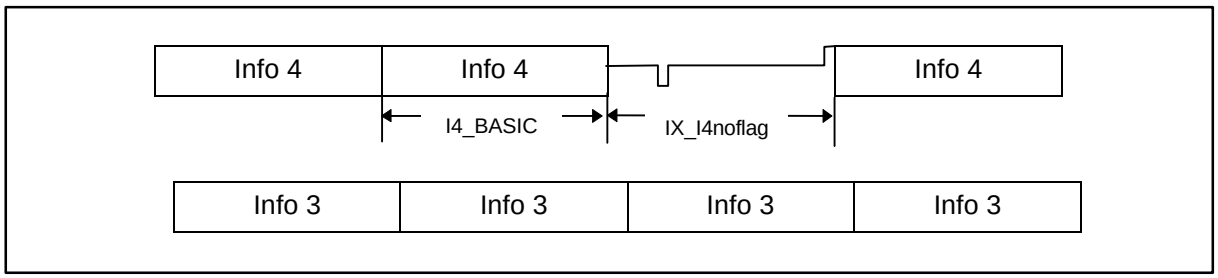
This test checks if TE does not lose frame alignment on receipt of one bad frame. The pattern for the bad frame is defined as IX_96 KHz. This pattern consists of alternating pulses at 96 KHz during the whole frame.



DEVICE	SETTINGS	RESULT
W6690	None	Pass

7.2.5.2 FAinfB_1fr

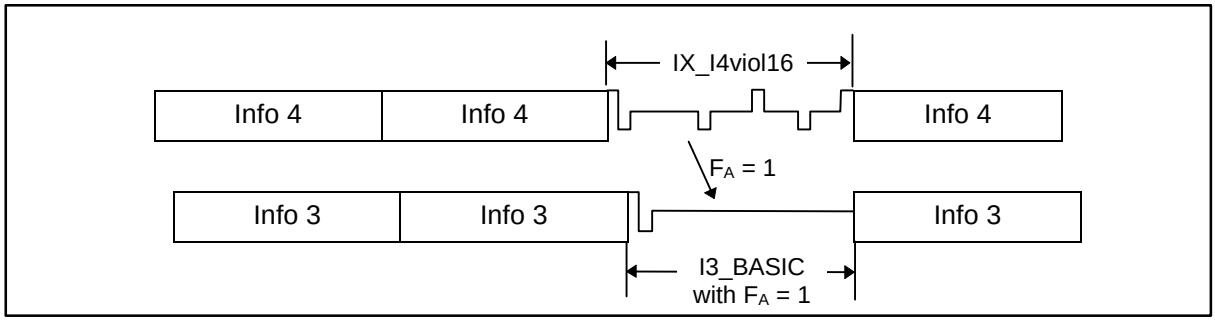
This test checks if TE does not lose frame alignment on receipt of one IX_I4noflag frame which has no framing and balancing bit. The following figure indicates one possible IX_I4noflag waveform.



DEVICE	SETTINGS	RESULT
W6690	None	Pass

7.2.5.3 FAinfD_1fr

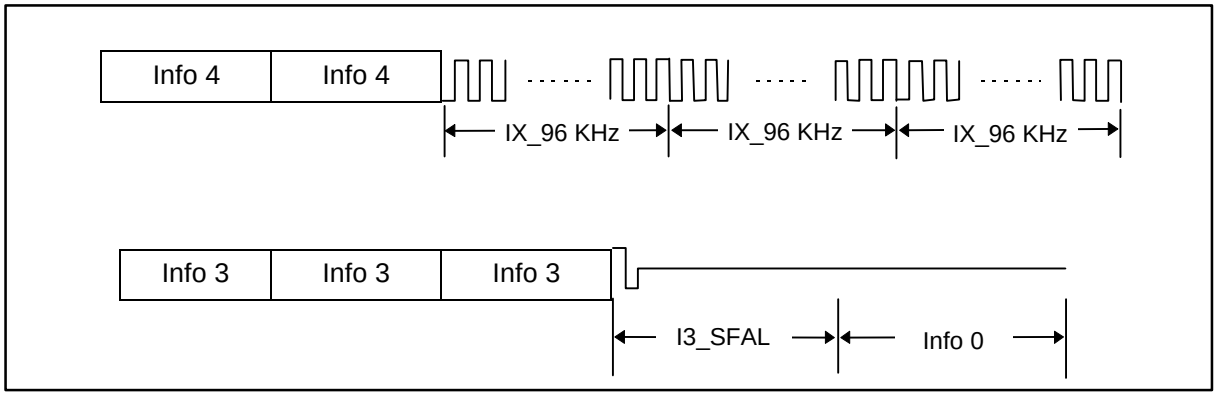
This test checks if TE does not lose frame alignment on receipt of one IX-I4viol16 frame. The IX_I4viol16 frame remains at binary "1" until the first B2 bit which is bit position 16. The pulse sequences are: Framing bit, balancing bit, B2 bit, M bit, S bit, balancing bit. The TE should reflect the received FA bit (FA = "1") in the transmitted frame.



DEVICE	SETTINGS	RESULT
W6690	None	Pass

7.2.5.4 FAinfA_kfr

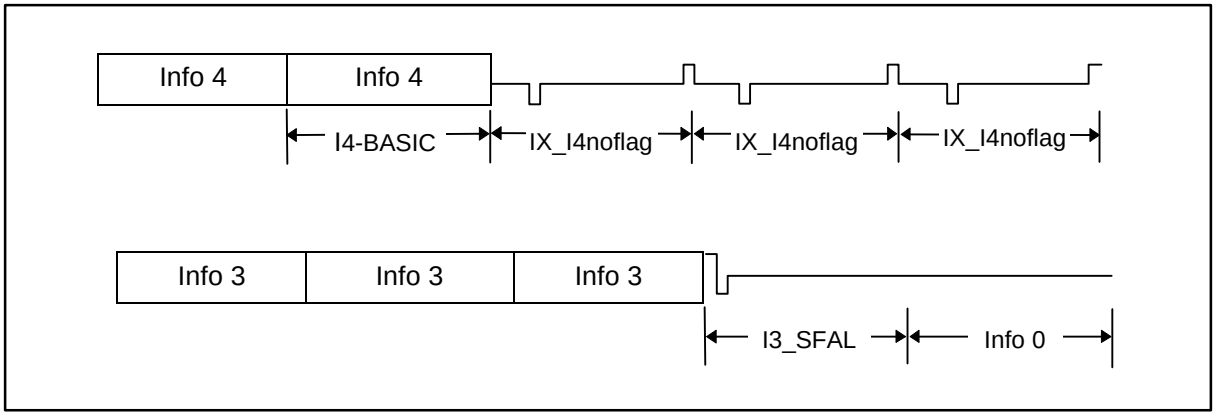
This is to test the number k of IX_96 KHz frames necessary for loss of frame alignment.



DEVICE	SETTINGS	RESULT
W6690	k = 2	Pass

7.2.5.5 FAinfB_kfr

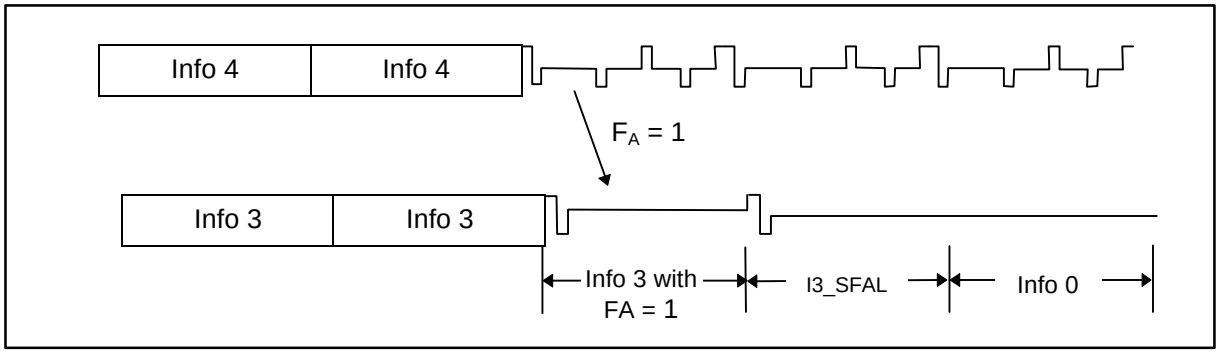
This is to test the number k of IX_I4noflag frames necessary for loss of frame alignment.



DEVICE	SETTINGS	RESULT
W6690	k = 2	Pass

7.2.5.6 FAinfD_kfr

This is to test the number k of IX_I4noflag frames necessary for loss of frame alignment.

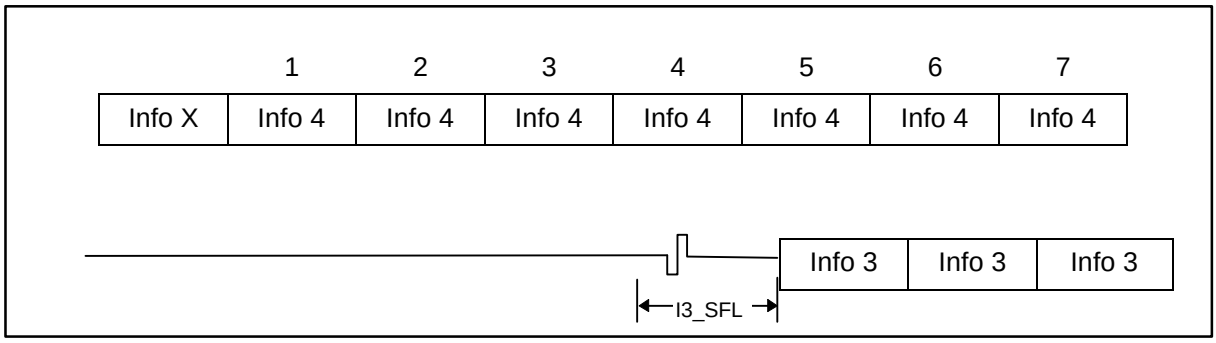


DEVICE	SETTINGS	RESULT
W6690	k = 2	Pass

7.2.5.7 Faregain

This is to test the number m of good frames necessary for regain of frame alignment. The TE regains frame alignment at m+1 frame.

The W6690 achieves synchronization after 5 frames, i.e m = 4.



DEVICE	SETTINGS	RESULT
W6690	m = 4	Pass

7.2.6 Multiframe Synchronization

As specified by ITU-T I.430, the Q bit is transmitted from TE to NT in the position normally occupied by the auxiliary framing bit (FA) in one frame out of 5, whereas the S bit is transmitted from NT to TE. The S and Q bit positions and multiframe structure are shown in Table 7.6.

The functions provided by W6690 are:

- Multiframe synchronization: Synchronization is achived when the M bit pattern has been correctly received during 20 consecutive frames starting from frame number 1.

  Note: Criterion for multiframe synchronization is not defined in I.430 Recommendation.
- S bits receive and detect: When synchronization is achieved, the four received S bits in frames 1, 6, 11, 16 are stored as S1 to S4 in the SQR register respectively. A change in the recived four bits (S1-4) is indicated by an interrupt (ISC in D_EXIR register and SCC in CIR register).
- Multiframe synchronization monitoring: Multiframe synchronization is constantly monitored. The synchronization state is indicated by the MSYN bit in the SQR register.
- Q bits transmit and F_A mirroring: When multiframe synchronization is achived, the four bits Q1-4 stored in the SQXR register are transmitted as the four Q bits (F_A-bit position) in frames 1, 6, 11 and 16. Otherwise the F_A bit transmitted is a mirror of the received F_A-bit. At loss of synchronization, the mirroring is resumed at the next F_A-bit.
- The multiframe synchronization can be disabled by setting MFD bit in the D_MODE register.
- According to I.430 Recommendation, the S/Q channel can be used as operation and maintenance signalling channel. At transmitter, a S/Q code for a message shall be repeated at least six times or as many as necessary to obtain the desired response. At receiver, a message shall be considered received only when the proper codes is received three consecutive times.

Table 7.6 Multiframe structure in S/T interface

Frame Number	NT-to-TE F_A-bit position	NT-to-TE M bit	NT-to-TE S bit	TE-to-NT F_A-bit position
1	ONE	ONE	S1	Q1
2	ZERO	ZERO	ZERO	ZERO
3	ZERO	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO	ZERO
6	ONE	ZERO	S2	Q2
7	ZERO	ZERO	ZERO	ZERO
8	ZERO	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO	ZERO
11	ONE	ZERO	S3	Q3
12	ZERO	ZERO	ZERO	ZERO
13	ZERO	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO	ZERO

Table 7.6 Multiframe structure in S/T interface, continued

Frame Number	NT-to-TE F_A-bit position	NT-to-TE M bit	NT-to-TE S bit	TE-to-NT F_A-bit position
16	ONE	ZERO	S4	Q4
17	ZERO	ZERO	ZERO	ZERO
18	ZERO	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO	ZERO
1	ONE	ONE	S1	Q1
2	ZERO	ZERO	ZERO	ZERO
etc.				

7.2.7 Test Functions

The W6690 provides loop and test functions as follows:

– Dgital loop via DLP bit in D_MODE register: In the layer 2 block, the transmitted 2B+D data are internally looped (from HDLC transmitter to HDLC receiver), and in the PCM ports, the transmitted B channels are internally looped (from PCM inputs to PCM outputs). The clock timings are generated internally and are independent of the S bus timing. This loop function is used for test of PCM and higher layer functions, excluding layer 1. After hardware reset, W6690 will power down if S bus is not connected or if there is no signal on the S bus. In this case, the C/I command ECK must be issued to power up the chip.

– Aalog loop via the C/I command EAL: The analog S interface transmitter is internally connected to the S interface receiver. When the receiver has synchronized itself to the internal INFO 3 signal, the message "Test Indication" or "Awake Test Indication" is delivered to the CIR register. No signal is transmitted over the S interface.

  In this mode, the S interface awake detector is enabled. Therefore if a level (INFO 2/ INFO 4) is detected on the S interface, this will be reported by the "Awake Test Indication (ATI)" indication.

– Rmote loopback via RLP bit in D_MODE register: The digital 2B data received from the S interface receiver is loopbacked to the S interface transmitter. The D channel is not looped. When RLP is enabled, layer 1 D channel is connected to HDLC port and DLP cannot be enabled.

– Tansmission of special test signals via layer 1 command :

  * Send Single Pulses (SSP): To send isolated single pulses of alternating polarity, with pulse width of one bit time, 250 μS apart, with a repetition frequency of 2 KHz.

  * Send Continuous Pulses (SCP): To send continuous pulses of alternating polarity, with pulse width of bit time. The repetition frequency is 96 KHz.

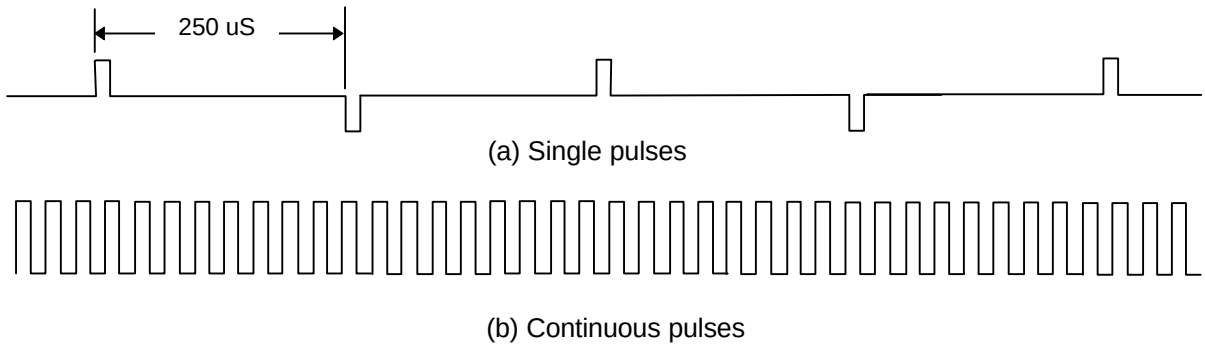


Figure 7.7 SSP and SCP Test Signals

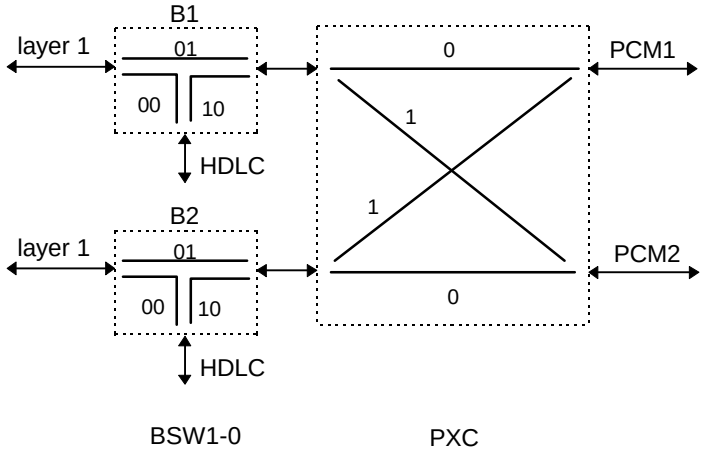
7.3 Serial Interface Bus

The 192 Kbps S/T interface signal consists of two B channels (64 Kbps each), one D channel (16 Kbps) and other control signals. The multiplexing/demultiplexing functions are carried out in the Serial Interface Bus (SIB) block. In addition, the B1 and B2 channels can be individually set to carry 64 Kbps or 56 Kbps traffic.

7.4 B Channel Switching

Each B channel in S/T bus can be individually programmed to connect to one of the three data ports: B channel HDLC controller , PCM port 1 or PCM port 2. In addition, the PCM ports can be programmed to connect to the B channel HDLC controller for voice recording/ retrieving from main memory in answering machine applications. In this case, only extended transparent mode can be used.

The switching matrix is controlled by PXC bit in PCTL register and BSW1–0 bits in B1_MODE and B2_MODE registers as follows:



A special mode is provided (BSW1–0 = 11B) in which case the PCM port can receive data from layer 1 and the HDLC receiver can receive data from PCM port simultaneously.

7.5 PCM Port

There are two PCM ports in W6690. Each PCM port can connect to a PCM codec filter chip. These two PCM ports share the same signals except for the frame synchronization clocks. The frame synchronization clocks (PFCK1-2) are 8 KHz and the bit synchronization clock (PBCK) is 1.536 MHz. The bit data rate is 64 Kbps per port.

7.6 D Channel HDLC Controller

There are two HDLC protocols that are used for ISDN layer 2 functions: LAPD and LAPB. Their frame formats are shown below.

LAPB modulo 8:

Flag (1 octet)	Address (1octet)	Control (1octet)	Information (0 or N octets)	FCS (2 octets)	Flag

Control field bits	7	6	5	4	3	2	1	0
I frame	N(R)			P	N(S)			0
S frame	N(R)			P/F	S	S	0	1
U frame	M	M	M	P/F	M	M	1	1

LAPB modulo 128:

Flag (1 octet)	Address (1octet)	Control (1 or 2 octets)	Information (0 or N octets)	FCS (2 octets)	Flag

	1st octet								2nd octet							
Control field bits	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I frame	N(S)							0	N(R)							P
S frame	X	X	X	X	S	S	0	1	N(R)							P/F
U frame	M	M	M	P/F	M	M	1	1								

LAPD: modulo 128 only

Flag (1 octet)	Address (2 octets)	Control (2 octets)	Information (0 or N octets)	FCS (2 octets)	Flag (1 octet)

	1st octet								2nd octet							
Control field bits	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I frame	N(S)							0	N(R)							P/F
S frame	0	0	0	0	S	S	0	1	N(R)							P/F
U frame	M	M	M	P/F	M	M	1	1								

7.6.1 D Channel Message Transfer Modes

The D channel HDLC controller operates in transparent mode.

Chracteristics:

- Receive frame address recognition
- Address comparison maskable bit-by-bit
- Flag generation/deletion
- Zero bit insertion/deletion
- Frame Check Sequence (FCS) generation/ check with CRC_ITU-T

Note: The LAPD protocol uses the CRC_ITU-T for Frame Check Sequence. The polynominal is $X^{16} + X^{12} + X^5 + 1$.

For address recognition, the W6690 provides four programmable registers for individual SAPI and TEI values, SAP1-2 and TEI1-2, plus two fixed values for group SAPI and TEI, SAPG and TEIG. The SAPG equals FEH or FCH which corresponds to SAPI = 63 for layer management procedure. The TEIG equals FFH which corresponds to TEI = 127 for automatic TEI assignment procedure. The address combinations are:

- SAP1 + TEI1
- SAP1 + FFH
- SAP2 + TEI2
- SAP2 + FFH
- FEH (FCH) + TEI1
- FEH (FCH) + TEI2
- FEH (FCH) + FFH

The receive frame address comparisons can be disabled (masked) per bit basis with the D_SAM and D_TAM registers, but comparisons with the SAPG or TEIG cannot be disabled.

7.6.2 Reception of Frames in D Channel

A 64-byte FIFO is provided in the receive direction. The data movement between receive FIFO and micro-processor is handled by interrupts.

There are two interrupt sources: Receive Message Ready (D_RMR) and Receive Message End (D_RME). The D_RMR interrupt indicates that at least 32 bytes of data have been received and the message/ frame is not ended. Upon D_RMR interrupt, the micro-processor reads out 32 bytes of data from the FIFO. The D_RME interrupt indicates the last segment of a message or a message with length ≤ 32 bytes has been received. The length of data is less than or equal to 32 and is specified in the D_RBCL register.

If the length of the last segment of message is 32, only D_RME interrupt is generated and the RBC4-0 bits in D_RBCL register are 00000B.

The data between the opening flag and the CRC field are stored in D_RFIFO. For LAPD frame, this includes the address field, control field and information field.

When a D_RMR or D_RME interrupt is generated, the micro-processor must read out the data from D_RFIFO and issues the Receive Message Acknowledgement command (D_CMDR: RACK bit) to explicitly acknowledge the interrupt. The micro-processor must handle the interrupt before more than 32 bytes of data are received. This corresponds to a maximum micro-processor reaction time of 16 mS at 16 Kbps data rate.

If the micro-processor is late in handling the interrupt, the incoming additional bytes will result in a "data overflow" interrupt and status bit.

7.6.3 Transmission of Frames in D Channel

A 64-byte FIFO is provided in the transmit direction. If the transmit FIFO is ready (which is indicated by a D_XFR interrupt), the micro-processor can write up to 32 bytes of data into the FIFO and use the XMS command bit to start frame transmission. The HDLC transmitter sends the opening flag first and then sends the data in the transmit FIFO.

The micro-processor must write the address, control and information field of a frame into the transmit FIFO.

Every time no more than 32 bytes of data are left in the transmit FIFO, the transmitter generates a D_XFR interrupt to request another block of data. The micro-processor can then write further data to the transmit FIFO and enables the subsequent transmission by issuing an XMS command.

If the data written to the FIFO is the last segment of a frame, the micro-processor issues the XME (Transmit Message End) and XMS command bits to finish the frame transmission. The transmitter then transmits the data in the FIFO and appends CRC and closing flag.

If the micro-processor fails to respond the D_XFR interrupt within a given time (16 mS), a data underrun condition will occur. The W6690 will automatically reset the transmitter and send inter frame time fill pattern (all 1's) on D channel. The micro-processor is informed about this condition via an XDUN (Transmit Data Underrun) interrupt in D_EXIR register. The microprocessor must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

It is possible to abort a frame by issuing a D_CMDR: XRST (D channel Transmitter Reset) command. The XRST command resets the transmitter and causes a transmit FIFO ready condition.

After the micro-processor has issued the XME command, the successful termination of transmission is indicated by an D_XFR interrupt.

The inter-frame time fill pattern must be all 1's, according to ITU-T I.430.

Collisions which occur on the D channel of S interface will cause an D_EXIR: XCOL interrupt. A XRST (Transmitter Reset) command must be issued and software must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

7.7 B Channel HDLC Controller

There are two B channel HDLC controllers. Each B channel HDLC controller provides two operation modes:

– Transparent mode

characteristics:

* 2 byte address field
* Receive address comparison maskable bit-by-bit
* Data between opening flag and CRC (not included) stored in receive FIFO
* Flag generation/ deletion
* Frame Check Sequence generation/ check with CRC_ITU-T polynominal
* Zero bit insertion/ deletion

– Extended transparent mode

characteristics:

* All data transmitted/received without modification
* No address comparison
* No flag generation/ detection
* No FCS generation/ check
* No bit stuffing

For PCM-HDLC connection, only extended transparent mode can be selected.

The data rate in B channel can be set at 64 Kbps or 56 Kbps by the B1_MODE (B2_MODE): SW56 bit.

7.7.1 Reception of Frames in B Channel

A 64-byte FIFO is provided in the receive direction. The receive FIFO threshold can be set at 48 or 32 bytes by the Bn_MODE register. If the number of received data reaches the threshold, a Receive Message Ready (RMR) interrupt will be generated.

The operations for reception of frames differ in each mode:

Transparent mode: The received frame address is compared with the contents in receive address registers. In addition, the comparisons can be selectively masked bit-by-bit via address mask registers. Comparison is disabled when the corresponding mask bit is "1".

In addition, flag recognition, CRC check and zero bit deletion are also performed. The result of CRC check is indicated in Bn_STAR: CRCE bit. The data between opening flag and CRC field (not included) is stored in receive FIFO. Two interrupts are used for the reception of data. The RMR interrupt in Bn_EXIR register indicates at least a threshold block of data have been put in the receive FIFO. The RME interrupt in Bn_EXIR register indicates the end of frame has been received. The

micro-processor can read out a threshold length of data from receive FIFO at RMR interrupt, or all the data in receive FIFO at RME interrupt. At each RMR/ RME interrupt, micro-processor must issue a Receive Message Acknowledgement (RACK) command to explicitly acknowledge the interrupt.

The micro-processor reaction time for RMR/RME interrupt depends on the FIFO threshold setting and B channel data rate. For example, it is 4 mS if the FIFO threshold is 32 and the B channel data rate is 64 Kbps.

If the micro-processor is late in handling the interrupt, the incoming additional bytes will result in a "data overflow" interrupt and status bit.

Extended transparent mode:

In this mode, all data received are stored in the receive FIFO without any modification. Every time up to a threshold length of data has been stored in the FIFO, a Bn_RMR interrupt is generated.

In this mode, there is no RME interrupt.

The micro-processor must react to the RMR interrupt in time, otherwise a "data overflow" interrupt and status bit will be generated.

7.7.3 Transmission of Frames in B Channel

A 64-byte FIFO is provided in the transmit direction. The FIFO threshold can be set at 32 or 48 bytes. The transmitter and receiver use the same FIFO threshold setting.

The transmit operations differ in both modes:

Transparent mode:

In this mode, the following functions are performed by the transmitter automatically :

- Flag generation
- CRC generation
- Zero bit insertion

The fields such as address, control and information are provided by the micro-processor and are stored in transmit FIFO. To start the frame transmission, the micro-processor issues a XMS (Transmit Message Start) command. The transmitter requests another block of data via XFR interrupt when no more than a threshold length of data are left in the FIFO.The micro-processor then writes up to a threshold length of data into the FIFO and activates the subsequent transmission of the frame by a XMS command too. The micro-processor indicates the end of the frame transmission by issuing XME (Transmit Message End) and XMS commands at the same time. The transmitter then transmits all the data left in the transmit FIFO and appends the CRC and closing flag. After this, a XFR interrupt is generated.

The inter-frame time fill pattern can be programmed to 1's or flags.

During the frame transmission, the micro-processor reaction time for the XFR interrupt depends on the FIFO threshold setting and B channel data rate. For example, it is 4 mS if the FIFO threshold is 32 and the B channel data rate is 64 Kbps. If the micro-processor fails to responds within the given reaction time, the transmit FIFO will be underrun. In this case, the W6690 will automatically reset the transmitter and send the inter frame time fill pattern on B channel. The micro-processor is informed about this via a Transmit Data Underrun interrupt (XDUN bit in Bn_EXIR register). The

microprocessor must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

The micro-processor can abort a frame transmission by issuing a Transmitter Reset command (XRES bit in Bn_CMDR register). The XRES command resets the transmitter and sends inter frame time fill pattern on B channel. It also results in a transmit pool ready condition.

Extended transparent mode:

All the data in the transmit FIFO are transmitted without any modification, i.e. no flags and CRCs are inserted, and no bit stuffing is performed.

Transmission is started by a XMS command. The transmitter requests another block of data via XFR interrupt when no more than a threshold length of data is left in the FIFO. The micro-processor reacts to this condition by writing up to a threshold length of data into the transmit FIFO and issues a XMS command to continue the message transmission.

The micro-processor reaction time depends on the FIFO threshold setting and B channel data rate. For example, it is 4 mS if the FIFO threshold is 32 and the B channel data rate is 64 Kbps. If the micro-processor fails to responds within the given reaction time, the transmit FIFO will hold no data to transmit. In this case, the W6690 will automatically reset the transmitter and send the inter frame time fill pattern on B channel. The micro-processor is informed about this via a Transmit Data Underrun interrupt (XDUN bit in Bn_EXIR register). The microprocessor must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

7.8 ISA Plug and Play Controller/Micro-processor Interface

7.8.1 Modes of Operations

The micro-processor interface provides four modes of operation:

- ISA bus with Plug and Play (PNP) capability
- ISA bus without PNP
- 8-bit Intel multiplexed address/data mode
- 8-bit Motorola micro-processor mode

The first mode is used in systems which supports plug and play utility. In this case, the I/O ports and interrupt line are configured automatically by the system software. In second case, the configurations are done manually. The third mode is used for connection to a 8 bit Intel type micro-processor and the fourth mode is used to connect a Motorola type micro-processor.

The plug and play resource requirements are : three contiguous I/O ports and one interrupt request line.

The serial identifier and resource data are stored in a 9346/93C46 type serial EEPROM. Only read operation is provided by W6690. W6690 connects with this EEPROM via the following diagram:

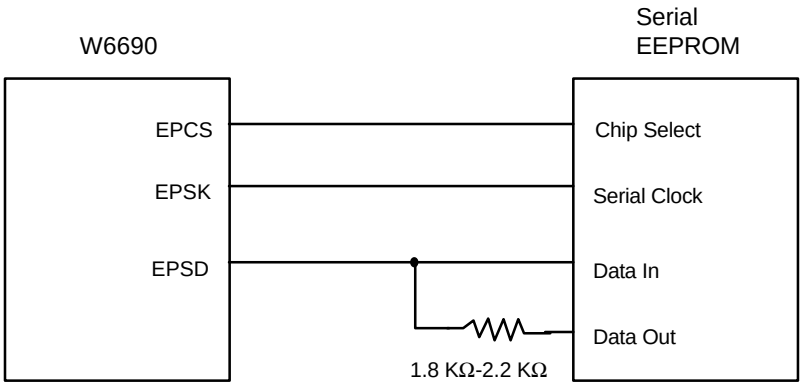


Figure 7.8 PNP ISA Serial EEPROM Connection Diagram

The W6690 provides two types of 8-bit micro-processor interfaces:

(1) Intel multiplexed address/data bus type with control signals CSIN*, IORC*, IOWC* and ALE

(2) Motorola type with control signals CSIN*, R/W*, DS*

The selection is made via MPSEL1-0 pins as follows:

MPSEL1	MPSEL0	FUNCTION
0	0	PNP ISA mode
0	1	ISA mode
1	0	Intel multiplexed micro-processor mode
1	1	Motorola micro-processor mode

7.8.2 Cascade Structure of Interrupt Sources

The W6690 uses cascade structure to record the causes of various interrupts. The interrupt structure is shown in Figure 7.9.

A read of the ISTA register clears all the interrupts except D_EXI, B1_EXI and B2_EXI bits. These three bits are cleared if their corresponding extended interrupt registers are cleard.

B1_EXI bit is cleared by reading the B1_EXIR register and B2_EXI bit is cleared by reading the B2_EXIR register. Reading of B1_EXIR or B2_EXIR register clears all the bits in it. The B1_EXIM and B2_EXIM registers mask the corresponding bits in the B1_EXIR and B2_EXIR registers.

To clear the D_EXI bit, all the bits in D_EXIR must first be cleared. A read of the D_EXIR register clears all the bits except the ISC bit. The ISC bit is cleared by a read of CIR and SQR registers.

An ISC interrupt may originate from

– a change in the received indication code (ICC bit in CIR register) or

– a change in the received S code (SCC bit in CIR register).

The ICC interrupt can not be disabled while the SCC interrupt can be disbled by clearing the SCIE bit in SQX register.

Bits SCC and ICC are cleared by a read of SQR and CIR.

D_EXIM register masks the corresponding bits in D_EXIR register. If the D_EXIM: ISC bit is set to one, it masks the ICC and SCC interrupts.

The ICC or SCC bit is set whenever a new code is loaded in CIR or SQR. But if the previous register content has not been read out in case of a code change, the new code will not be loaded. The code registers are buffered with a FIFO size of two. Thus if several consecutive code changes are detected, only the first and the last code is obtained at the first and second register read, respectively.

For Intel and Motorola modes, the interrupt request pin is level triggered with LOW active. It stays active until all the bits in ISTA register are cleared. If a new status bit is set while interrupt line is asserted, the interrupt request line makes no change. This may cause problems if W6690 is connected to edge triggered interrupt controllers (because the new status bit does not cause edge transition).

To solve this problem, the software can write FFH into the IMASK register and then write back the old value. As soon as all the mask bits are set, ISTA register will temporarily be cleared to zero and the interrupt request line goes inactive. When the old value is written in the mask register, interrupt request line will make an edge transition if there was a queued status bit.

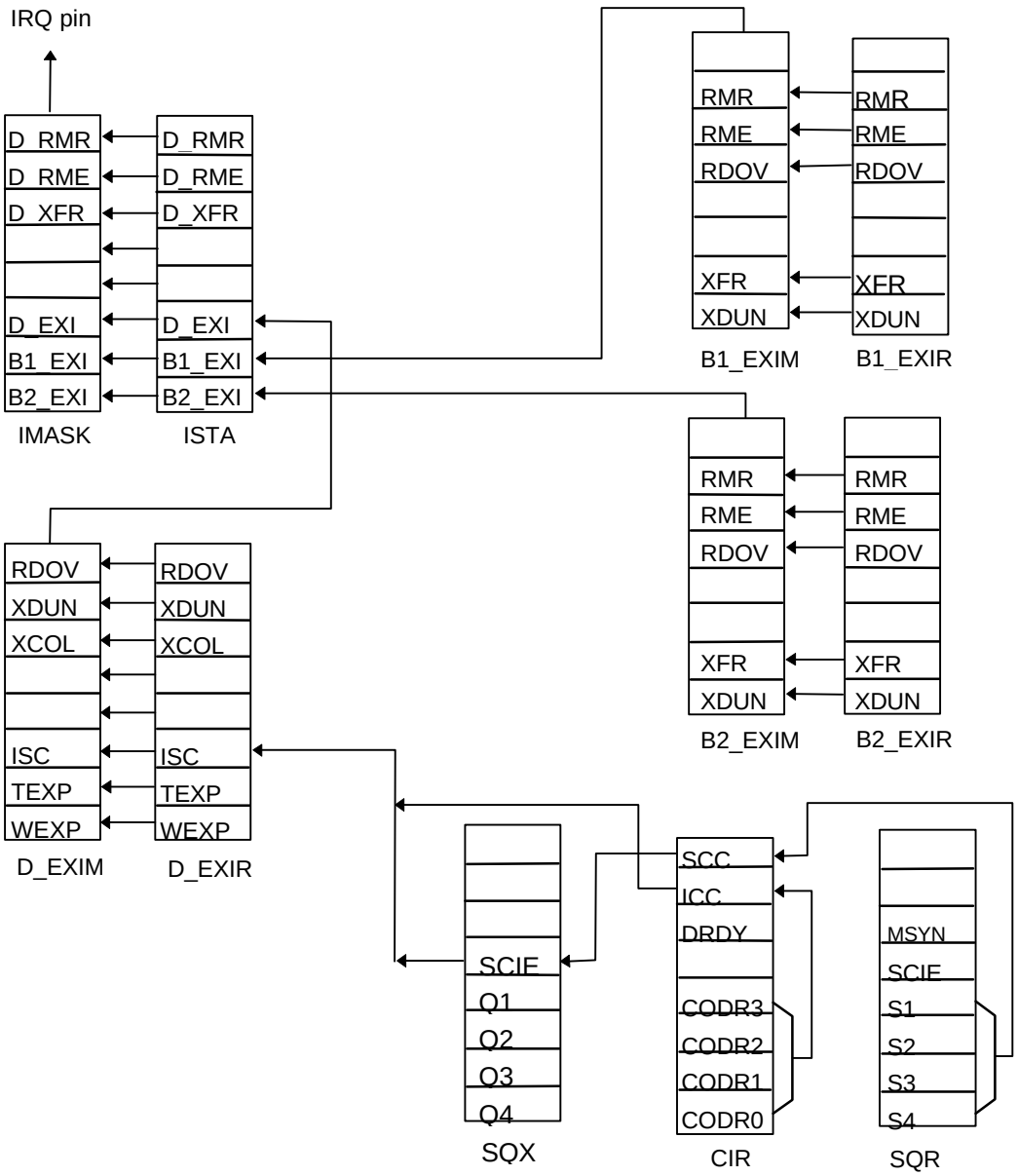


Figure 7.9 W6690 Interrupt Structure

8. REGISTER DESCRIPTIONS

Three 8-bit registers are used by the micro-processor to access the W6690's internal registers, excluding the PNP ISA control/status registers. The internal registers are accessed by first writing the address into "Device Address Index register", followed by a number of write and/or read operations. The "Device Write Data register" is the destination of write data, and the "Device Read Data register" is the destination of read data.

Table 8.1 Register address map: Device internal registers access control

ADDRESS PINS (A1A0)	ACCESS	REGISTER NAME	DESCRIPTION
00	W	DEV_ADR	Address index for device's registers
01	W	DEV_WR	Write data for device's registers
10	R	DEV_RD	Read data for device's registers

Table 8.2 Register summary: Device internal registers access control

ADDRESS PINS (A1A0)	R/W	NAME	7	6	5	4	3	2	1	0
00	W	DEV_ADR								
01	W	DEV_WR								
10	R	DEV_RD								

In sections 8.1–8.3, the term "Offset address" means the value that is programmed in the DEV_ADR register.

8.1 Chip Control and D_ch HDLC Controller

Table 8.3 Register address map: Chip Control and D channel HDLC

OFFSET	ACCESS	REGISTER NAME	DESCRIPTION
00	R	D_RFIFO	D channel receive FIFO
01	W	D_XFIFO	D channel transmit FIFO
02	W	D_CMDR	D channel command register
03	R/W	D_MODE	D channel mode control
04	R/W	D_TIMR	D channel timer control
05	R_clear	ISTA	Interrupt Status Register
06	R/W	IMASK	Interrupt Mask Register
07	R_clear	D_EXIR	D channel extended interrupt
08	R/W	D_EXIM	D channel extended interrupt mask

Table 8.3 Register address map: Chip Control and D channel HDLC, continued

OFFSET	ACCESS	REGISTER NAME	DESCRIPTION
09	R	D_STAR	D channel status register
0A	R	D_RSTA	D channel receive status
0B	R/W	D_SAM	D channel address mask 1
0C	R/W	D_SAP1	D channel individual SAPI 1
0D	R/W	D_SAP2	D channel individual SAPI 2
0E	R/W	D_TAM	D channel address mask 2
0F	R/W	D_TEI1	D channel individual TEI 1
10	R/W	D_TEI2	D channel individual TEI 2
11	R	D_RBCH	D channel receive frame byte count high
12	R	D_RBCL	D channel receive frame byte count low
13		Reserved	
14		Reserved	
15	R/W	D_CTL	D channel control register
16	R	CIR	Command/Indication receive
17	W	CIX	Command/Indication transmit
18	R	SQR	S/Q channel receive register
19	W	SQX	S/Q channel transmit register
1A	R/W	PCTL	PCM control register

Table 8.4 Register summary: Chip Control and D channel HDLC

OFFSET	R/W	NAME	7	6	5	4	3	2	1	0
02	W	D_CMDR	RACK	RRST		STT	XMS		XME	XRST
03	R/W	D_MODE	MMS	RACT		TMS	TEE	MFD	DLP	RLP
04	R/W	D_TIMR	CNT2	CNT1	CNT0	VAL4	VAL3	VAL2	VAL1	VAL0
05	R_clr	ISTA	D_RMR	D_RME	D_XFR			D_EXI	B1_EXI	B2_EXI
06	R/W	IMASK	D_RMR	D_RME	D_XFR			D_EXI	B1_EXI	B2_EXI
07	R_clr	D_EXIR	RDOV	XDUN	XCOL			ISC	TEXP	WEXP
08	R/W	D_EXIM	RDOV	XDUN	XCOL			ISC	TEXP	WEXP
09	R	D_STAR	XDOW		XBZ	DRDY				
0A	R	D_RSTA		RDOV	CRCE	RMB				
0B	R/W	D_SAM	SAM7	SAM6	SAM5	SAM4	SAM3	SAM2	SAM1	SAM0
0C	R/W	D_SAP1	SA17	SA16	SA15	SA14	SA13	SA12	SA11	SA10
0D	R/W	D_SAP2	SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20

Table 8.4 Register summary: Chip Control and D channel HDLC, continued

OFFSET	R/W	NAME	7	6	5	4	3	2	1	0
0E	R/W	D_TAM	TAM7	TAM6	TAM5	TAM4	TAM3	TAM2	TAM1	TAM0
0F	R/W	D_TEI1	TA17	TA16	TA15	TA14	TA13	TA12	TA11	TA10
10	R/W	D_TEI2	TA27	TA26	TA25	TA24	TA23	TA22	TA21	TA20
11	R	D_RBCH	VN1	VN0	LOV	RBC12	RBC11	RBC10	RBC9	RBC8
12	R	D_RBCL	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
13			Reserved							
14			Reserved							
15	R/W	D_CTL	WTT1	WTT2	SRST			TPS	OPC1	OPC0
16	R	CIR	QCC	ICC			CODR3	CODR2	CODR1	CODR0
17	W	CIX					CODX3	CODX2	CODX1	CODX0
18	R	SQR			MSYN	QCIE	Q1	Q2	Q3	Q4
19	W	SQX				QCIE	S1	S2	S3	S4
1A	R/W	PCTL								PXC

8.1.1 D_ch receive FIFO D_RFIFO Read Address 00H

The D_RFIFO has a length of 64 bytes.

After a D_RMR interrupt, exactly 32 bytes are available.

After a D_RME interrupt, the number of bytes available equals RBC4-0 bits in the D_RBCL register.

8.1.2 D_ch transmit FIFO D_XFIFO Write Address 01H

The D_XFIFO has a length of 64 bytes.

After an D_XFR interrupt, up to 32 bytes of data can be written into this FIFO for transmission. At the first time, up to 64 bytes of data can be written.

8.1.3 D_ch command register D_CMDR Write Address 02H

Value after reset: 00H

7	6	5	4	3	2	1	0
RACK	RRST		STT	XMS		XME	XRST

RACK Receive Acknowledge

After a D_RMR or D_RME interrupt, the processor must read out the data in D_RFIFO and then sets this bit to acknowledge the interrupt.

RRST Receiver Reset

Setting this bit resets the D_ch HDLC receiver and clears the D_RFIFO data.

STT Start Timer

The D_ch hardware timer is started when this bit is set to one. The timer may be stopped by a write of the D_TIMR register. Note that the timer must be in external mode.

XMS Transmit Message Start/Continue

Setting this bit will start or continue the transmission of a frame. The opening flag is automatically added by the HDLC controller.

XME Transmit Message End

Setting this bit indicates the end of frame transmission.. The D_ch HDLC controller automatically appends the CRC and the closing flag after the data transmission.

Note: If the frame ≤ 32 bytes, XME plus XMS commands must be issued at the same time.

XRST Transmitter Reset

Setting this bit resets the D_ch HDLC transmitter and clears the D_XFIFO. The transmitter will send inter frame time fill pattern (which is 1's) immediately. This command also results in a transmit FIFO ready condition.

8.1.4 D_ch Mode Register D_MODE Read/Write Address 03H

Value after reset: 00H

7	6	5	4	3	2	1	0
MMS	RACT		TMS	TEE	MFD	DLP	RLP

MMS Message Mode Setting

Determines the message transfer mode of the D_ch HDLC controller:

MMS	Mode	Address bytes	First byte address comparison with:	Second byte address comparison with:
0	Transparent mode	2	D_SAP1, D_SAP2, SAPG	D_TEI1, D_TEI2, TEIG

Notes:

1. D_SAP1, D_SAP2: two programmable address values for the first received address byte; SAPG = fixed value FC/FEH. D_TEI1, D_TEI2: two programmable address values for the second received address byte; TEIG = fixed value FFH.
2. The first byte address comparison can be masked by D_SAM register, and the second byte address comparison can be masked by D_TAM register. But the comparisons with SAPG and TEIG cannot be disabled.

MDS = 1 is used for internal test purpose only.

RACT Receiver Active

Setting this bit activates the D_ch HDLC receiver. This bit can be read. The receiver must be in active state in order to receive data.

TMS Timer Mode Setting

Sets the operating mode of the D_ch timer. In the external mode (TMS = 0), the timer is controlled by the processor. It is started by setting the STT bit in D_CMDR and is stopped by a write of the D_TIMR register. When the timer expires, a D_EXP interrupt is generated.

In the internal mode (TMS = 1), the timer is used for internal test purposes. It should not be selected for normal chip operation.

TEE Terminal Equipment Function Enable

The terminal equipment function is enabled when this bit is "1". The supported functions are:

– Watchdog timer, enabled when TEE = 1 and D_CTL: TPS = 1

– Exchange awake, enabled when TEE = 1 and D_CTL: TPS = 0

When the watchdog timer has been enabled, the micro-processor has to program the WTT1, 2 bits in a specified manner within 1024 mS to reset and restart the timer. Otherwise, the timer will expire in 1024 mS and a WEXP interrupt together with a 125 μS reset pulse on TRST pin is generated.

The exchange awake condition is initiated by C/I code change condition. A 16 mS reset pulse on TRST pin is generated.

Switching TPS bit will reset the watchdog timer.

The TEE bit is cleared only by a hardware reset.

MFD Multiframe Disable

This bit is used to enable or disable the multiframe structure on S/T interface :

0: Multiframe is enabled

1: Multiframe is disabled

DLP Digital Loopback

Setting this bit activates the digital loopback function. The transmitted digital 2B+D channels are looped to the received 2B+D channels. Note that after hardware reset, the internal clocks will turn off if the S bus is not connected or if there is no signal on the S bus. In this case, the C/I command ECK must be issued to enable loopback function.

RLP Remote Loopback

Setting this bit to "1" activates the remote loopback function. The received 2B channels from the S interface are looped to the transmitted 2B channels of S interface. The D channel is not looped in this loopback function.

8.1.5 D_ch Timer Register D_TIMR Read/Write Address 04H

Value after reset: FFH

7	6	5	4	3	2	1	0
CNT2	CNT1	CNT0	VAL4	VAL3	VAL2	VAL1	VAL0

CNT together with VAL determine the time period T2 after which a TEXP interrupt will be generated:

T2 = CNT * 2.048 s + T1 with T1 = (VAL +1) * 0.064 s

The timer is started by setting the STT bit in D_CMDR and will be stopped when a TEXP interrupt is generated or the D_TIMR register is written.

Note: If CNT is set to 7, a TEXP interrupt is generated periodically at every expiration of T1.

This register can be read only after the timer has been started. The read value indicates the timer's current count value. In case layer 1 is not activated, a C/I command "ECK" must be issued in addition to the STT command to start the timer.

8.1.6 Interrupt Status RegisterISTA Read-clear Address 05H

Value after reset: 00H

7	6	5	4	3	2	1	0
D_RMR	D_RME	D_XFR			D_EXI	B1_EXI	B2_EXI

D_RMR D_ch Receive Message Ready

A 32-byte data is available in the D_RFIFO. The frame is not complete yet.

D_RME D_ch Receive Message End

The last part of a frame with length > 32 bytes or a whole frame with length ≤ 32 bytes has been received. The whole frame length is obtained from D_RBCH + D_RBCL registers. The length of data in the D_RFIFO equals:

data length = RBC4-0 if RBC4-0 ≠ 0
data length = 32 if RBC4-0 = 0

D_XFR D_ch Transmit FIFO Ready

This bit indicates that the transmit FIFO is ready to accept data. Up to 32 bytes of data can be written into the D_XFIFO.

An D_XFR interrupt is generated in the following cases:

- after an XMS command, when ≥32 bytes of XFIFO is empty
- after an XMS together with an XME command is issued, when the whole frame has been transmitted
- after an XRST command
- after hardware reset

D_EXI D_ch Extended Interrupt

This bit indicates that at least one interrupt bit has been set in D_EXIR register.

B1_EXI B1_ch Extended Interrupt

This bit indicates that at least one interrupt bit has been set in B1_EXIR register.

B2_EXI B2_ch Extended Interrupt

This bit indicates that at least one interrupt bit has been set in B2_EXIR register.

Note: A read of the ISTA register clears all bits except D_EXI, B1_EXI and B2_EXI bits. D_EXI bit is cleared when all bits in D_EXIR register are cleared, B1_EXI bit is cleared by reading B1_EXI register and B2_EXI bit is cleared by reading B2_EXIR register.

8.1.7 Interrupt Mask Register IMASK R/W Address 06H

Value after reset: FFH

7	6	5	4	3	2	1	0
D_RMR	D_RME	D_XFR			D_EXI	B1_EXI	B2_EXI

Setting the bit to "1" masks the corresponding interrupt source in ISTA register. Masked interrupt status bits are read as zero. They are internally stored and pending until the mask bits are zero.

Setting the D_EXI, B1_EXI or B2_EXI bit to "1" masks all the interrupts in D_EXIR, B1_EXIR or B2_EXIR register, respectively.

8.1.8 D_ch Extended Interrupt Register D_EXIR Read Clear Address 07H

Value after reset: 00 H

7	6	5	4	3	2	1	0
RDOV	XDUN	XCOL			ISC	TEXP	WEXP

RDOV Receive Data Overflow

Frame overflow (too many short frames) or data overflow occurs in the receive FIFO. In data overflow, the incoming data will overwrite the data in the receive FIFO. If RDOV interrupt occurs, software has to reset the receiver and discard the data received.

XDUN Transmit Data Underrun

This interrupt indicates the D_XFIFO has run out of data. In this case, the W6690 will automatically reset the transmitter and send the inter frame time fill pattern (all 1's) on D channel. The microprocessor must wait until transmit FIFO ready (via XFR interrupt or XFA bit), re-write data, and issue XMS command to re-transmit the data.

XCOL Transmit Collision

This bit indicates a collision on the S-bus has been detected. A XRST command must be issued and software must wait until transmit FIFO ready (via XFR interrupt), re-write data, and issue XMS command to re-transmit the data.

ISC Indication or S Channel Change

A change in the layer 1 indication code or multiframe S channel has been detected. The actual value can be read from CIR or SQR registers.

TEXP D_ch Timer Expiration

Expiration occurs in the D_ch timer. The timer must be in external mode.

WEXP Watchdog Timer Expiration

Expiration occurs in the watch dog timer. A reset pulse with 125 µS pulse width is also generated on the TRST pin. See D_CTL register for watch dog timer control.

8.1.9 D_ch Extended Interrupt Mask Register D_EXIM Read/Write Address 08H

Value after reset: FFH

7	6	5	4	3	2	1	0
RDOV	XDUN	XCOL			ISC	TEXP	WEXP

Setting the bit to "1" masks the corresponding interrupt source in D_EXIR register. Masked interrupt status bits are read as zero. They are internally stored and pending until the mask bits are zero.

All the interrupts in D_EXIR will be masked if the IMASK:D_EXI bit is set to "1".

8.1.10 D_ch Status Register D_STAR Read Address 09H

Value after reset: 00H

7	6	5	4	3	2	1	0
XDOW		XBZ	DRDY				

XDOW Transmit Data Overwritten

At least one byte of data has been overwritten in the D_XFIFO. This bit is set by data overwritten condition and is cleared only by XRES command.

XBZ Transmitter Busy

This bit indicates the D_HDLC transmitter is busy. The XBZ bit is active from the transmission of opening flag to the transmission of closing flag.

DRDY D Channel Ready

This bit indicates the status of layer 1 D channel.

0: The layer 1 D channel is not ready. No transmission is allowed.

1: The layer 1 D channel is ready. Layer 2 can transmit data to layer 1.

8.1.11 D_ch Receive Status Register D_RSTA Read Address 0AH

Value after reset: 20H

7	6	5	4	3	2	1	0
	RDOV	CRCE	RMB				

RDOV Receive Data Overflow

A "1" indicates that the D_RFIFO is overflow. The incoming data will overwrite data in the receive FIFO. The data overflow condition will set both the status and interrupt bits. It is recommended that software must read the RDOV bit after reading data from D_RFIFO at RMR or RME interrupt. The software must abort the data and issue a RRST command to reset the receiver if RDOV = 1. The frame overflow condition will not set this bit.

CRCE CRC Error

This bit indicates the result of frame CRC check:

0: CRC correct

1: CRC error

RMB Receive Message Aborted

A "1" means that a sequence of seven 1's was received and the frame is aborted. Software must issue RRST command to reset the receiver.

Note: Normally D_RSTA register should be read by the micro-processor after a D_RME interrupt. The contents of D_RSTA are valid only after a D_RME interrupt and remain valid until the frame is acknowledged via a RACK bit.

8.1.12 D_ch SAPI Address Mask D_SAM Read/Write Address 0BH

Value after reset: 00H

7	6	5	4	3	2	1	0
SAM7	SAM6	SAM5	SAM4	SAM3	SAM2	SAM1	SAM0

This register masks(disables) the first byte address comparison of the incoming frame. If the mask bit is "1" the corresponding bit comparisons with D_SAP1, D_SAP2 are disabled. Comparison with SAPG is always performed.

Note: For the LAPD frame, the least significant two bits are the C/R bit and EA = 0 bit. It is suggested that the comparison with C/R bit be masked. EA = 0 for two octet address frame e.g LAPD, EA = 1 for one octet address frame.

8.1.13 D_ch SAPI1 Register D_SAP1 Read/Write Address 0CH

Value after reset: 00H

7	6	5	4	3	2	1	0
SA17	SA16	SA15	SA14	SA13	SA12	SA11	SA10

This register contains the first choice of the first byte address of received frame. For LAPD frame, SA17–SA12 is the SAPI value, SA11 is C/R bit and SA10 is zero.

8.1.14 D_ch SAPI2 Register D_SAP2 Read/Write Address 0DH

Value after reset: 00H

7	6	5	4	3	2	1	0
SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20

This register contains the second choice of the first byte address of received frame. For LAPD frame, SA27–SA22 is the SAPI value, SA21 is C/R bit and SA20 is zero.

8.1.15 D_ch TEI Address Mask D_TAM Read/Write Address 0EH

Value after reset: 00H

7	6	5	4	3	2	1	0
TAM7	TAM6	TAM5	TAM4	TAM3	TAM2	TAM1	TAM0

This register masks(disables) the second byte address comparison of the incoming frame. If the mask bit is "1" the corresponding bit comparisons with D_TEI1, D_TEI2 are disabled. Comparison with TEIG is always performed.

Note: For the LAPD frame, the least significant bit is the EA = 1 bit.

8.1.16 D_ch TEI1 Register D_TEI1 Read/Write Address 0FH

Value after reset: 00H

7	6	5	4	3	2	1	0
TA17	TA16	TA15	TA14	TA13	TA12	TA11	TA10

TA17–TA10

This register contains the first choice of the second byte address of received frame. For LAPD frame, TA17–TA11 is the TEI value, TA10 is EA = 1.

8.1.17 D_ch TEI2 Register D_TEI2 Read/Write Address 10H

Value after reset: 00H

7	6	5	4	3	2	1	0
TA27	TA26	TA25	TA24	TA23	TA22	TA21	TA20

TA27–TA20

This register contains the second choice of the second byte address of received frame. For LAPD frame, TA27–TA21 is the TEI value, TA20 is EA = 1.

8.1.18 D_ch Receive Frame Byte Count High D_RBCH Read Address 11H

Value after reset: 00H

7	6	5	4	3	2	1	0
VN1	VN0	LOV	RBC12	RBC11	RBC10	RBC9	RBC8

VN1–0 Chip Version Number

This is the chip version number. It is read as 00B.

LOV Length Overflow

A "1" in this bit indicates ≥ 4097 bytes are received and the frame is not yet complete. This bit is valid only after an D_RME interrupt and remains valid until the frame is acknowledge via the RACK command.

RBC12–8 Receive Byte Count

Four most significant bits of the total frame length. These bits are valid only after an D_RME interrupt and remain valid until the frame is acknowledge via the RACK command.

8.1.19 D_ch Receive Frame Byte Count Low D_RBCL Read Address 12H

Value after reset: 00H

7	6	5	4	3	2	1	0
RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0

RBC7–0 Receive Byte Count

Eight least significant bits of the total frame length. Bits RBC4-0 also indicate the length of the data currently available in D_RFIFO. These bits are valid only after an D_RME interrupt and remain valid until the frame is acknowledged via the RACK command.

8.1.20 D_ch Control Register D_CTL Read/Write Address 15H

Value after reset: 00H

7	6	5	4	3	2	1	0
WTT1	WTT2	SRST			TPS	OPS1	OPS0

WTT1, 2 Watchdog Timer Trigger 1, 2

When the watchdog timer has enabled (D_MODE: TEE = 1 and D_CTL:TPS = 1), the micro-processor has to program the WTT1, 2 bits in the following sequences within 1024 mS to reset and restart the timer. Otherwise, the timer will expire after 1024 mS and a WEXP interrupt together with a 125 µS reset pulse on TRST pin are generated:

SEQUENCE	WTT1	WTT2
1	1	0
2	0	1

Switching TPS bit from 0 to 1 or from 1 to 0 resets the watchdog timer.

SRST Software Reset

When this bit is set to "1", a software reset signal is activated. The effects of this reset signal are equivalent to the hardware reset pin RESET, except that it does not reset the PNP controller.

This bit is not auto-clear, the software must write "0" to this bit to exit from the reset mode.

Note: When SRST = 1, the chip is in reset state. Read or write to any of the registers is inhibited at this time. The SRST bit is write only.

TPS TRST Reset Pulse Select

This bit selects the source of reset pulse on TRST pin. It is valid only when the terminal equipment functions are enabled.

0: Exchange awake

A 16 mS reset pulse is generated when the a layer 1 indication code change has been detected.

1: Watchdog timer

A 125 μS reset pulse is generated as a result of the watchdog timer expiration.

Switching TPS bit from 0 to 1 or from 1 to 0 resets the watchdog timer.

OPS1–0 Output Phase Delay Compensation Select1–0

These two bits select the output phase delay compensation.

OPS1	OPS0	EFFECT
0	0	No output phase delay compensation
0	1	Output phase delay compensation 260 nS
1	0	Output phase delay compensation 520 nS
1	1	Output phase delay compensation 1040 nS

8.1.21 Command/Indication Receive Register CIR Read Address 16H

Value after reset: 0FH

7	6	5	4	3	2	1	0
SCC	ICC			CODR3	CODR2	CODR1	CODR0

SCC S Channel Change

A change in the received 4-bit S channel has been detected. The new code can be read from the SQR register. This bit is cleared by a read of the SQR register.

ICC Indication Code Change

A change in the received indication code has beendetected. The new code can be read from the CIR register. This bit is cleared by a read of the CIR register.

CODR3–0 Layer 1 Indication Code

Value of the received layer 1 indication code.

8.1.22 Command/Indication Transmit Register CIX Write Address 17H

Value after reset: 0FH

7	6	5	4	3	2	1	0
				CODX3	CODX2	CODX1	CODX0

CODX3–0 Layer 1 Command Code

Value of the command code transmitted from layer 2 to layer 1.

8.1.23 S/Q Channel Receive Register SQR Read Address 18H

Value after reset: 0FH

7	6	5	4	3	2	1	0
		MSYN	SCIE	S1	S2	S3	S4

MSYN Multiframe Synchronization

When this bit is "1", a multiframe synchronization is achived, i.e the the S/T receiver has synchronized to the received FA and M bit patterns.

SCIE S Channel Change Interrupt Enable

This bit reflects the bit written in the SQX register.

S1-4 Received S Bits

These are the S bits received in NT to TE direction in frames 1, 6, 11 and 16. S1 is in frame 1, S2 is in frame 6 etc.

8.1.24 S/Q Channel Transmit RegisterSQX Write Address 19H

Value after reset: 0FH

7	6	5	4	3	2	1	0
			SCIE	Q1	Q2	Q3	Q4

SCIE S Channel Change Interrupt Enable

This bit is used to enable/disable the generation of CIR:SCC status bit and interrupt.

0: Status bit and interrupt are disabled.

1: Status bit and interrupt are enabled.

Q1-4 Transmitted Q Bits

These are the transmitted Q channels in FA bit positions in frames 1, 6, 11 and 16. Q1 is in frame 1, Q2 is in frame 6 etc.

8.1.25 PCM Control Register PCTL Read/Write Address 1AH

Value after reset: 00H

7	6	5	4	3	2	1	0
							PXC

PXC PCM Cross-connect

This bit determines whether or not the PCM ports are cross-connected with the B channel ports. The setting of PXC is independent of the BSW1–0 bits.

PXC	CONNECTION
0	PCM1 ↔ B1, PCM2 ↔ B2
1	PCM1 ↔ B2, PCM2 ↔ B1

8.2. B1 HDLC controler

Table 8.5 Register address map: B1 channel HDLC

OFFSET	ACCESS	REGISTER NAME	DESCRIPTION
20	R	B1_RFIFO	B1 channel receive FIFO
21	W	B1_XFIFO	B1 channel transmit FIFO
22	W	B1_CMDR	B1 channel command register
23	R/W	B1_MODE	B1 channel mode control
24	R_clear	B1_EXIR	B1 channel extended interrupt
25	R/W	B1_EXIM	B1 channel extended interrupt mask
26	R	B1_STAR	B1 channel status register
27	R/W	B1_ADM1	B1 channel address mask 1
28	R/W	B1_ADM2	B1 channel address mask 2
29	R/W	B1_ADR1	B1 channel address 1
2A	R/W	B1_ADR2	B1 channel address 2
2B	R	B1_RBCL	B1 channel receive frame byte count low
2C	R	B1_RBCH	B1 channel receive frame byte count high

Table 8.6 Register summary: B1 channel HDLC

OFFSET	R/W	NAME	7	6	5	4	3	2	1	0
22	W	B1_CMDR	RACK	RRST	RACT			XMS	XME	XRST
23	R/W	B1_MODE	MMS	ITF	EPCM	BSW1	BSW0	SW56	FTS1	FTS0
24	R_clr	B1_EXIR		RMR	RME	RDOV			XFR	XDUN
25	R/W	B1_EXIM		RMR	RME	RDOV			XFR	XDUN
26	R	B1_STAR		RDOV	CRCE	RMB		XDOW		XBZ
27	R/W	B1_ADM1	MA17	MA16	MA15	MA14	MA13	MA12	MA11	MA10
28	R/W	B1_ADM2	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20
29	R/W	B1_ADR1	RA17	RA16	RA15	RA14	RA13	RA12	RA11	RA10
2A	R/W	B1_ADR2	RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20
2B	R	B1_RBCL	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
2C	R	B1_RBCH			LOV	RBC12	RBC11	RBC10	RBC9	RBC8

8.2.1 B1_ch receive FIFO B1_RFIFO Read Address 20H

The B1_RFIFO is a 64-byte depth FIFO memory with programmable threshold. The threshold value determines when to generate an interrupt.

When more than a threshold length of data has been received, a RMR interrupt is generated. After an RMR interrupt, 48 or 32 bytes can be read out, depending on the threshold setting.

In transparent mode, when the end of frame has been received, a RME interrupt is generated. After an RME interrupt, the number of bytes available is less than or equal to the threshold value.

8.2.2 B1_ch transmit FIFO B1_XFIFO Write Address 21H

The B1_XFIFO is a 64-byte depth FIFO with programmable threshold value. The threshold setting is the same as B1_RFIFO.

When the number of empty locations is equal to or greater than the threshold value, a XFR interrupt is generated. After a XFR interrupt, up to 48 or 32 bytes of data can be written into this FIFO for transmission.

8.2.3 B1_ch command register B1_CMDR Write Address 22H

Value after reset: 00H

7	6	5	4	3	2	1	0
RACK	RRST	RACT			XMS	XME	XRST

RACK Receive Message Acknowledge

After a RMR or RME interrupt, the micro-processor reads out the data in B1_RFIFO, it then sets this bit to explicitly acknowledge the interrupt.

RRST Receiver Reset

Setting this bit resets the B1_ch HDLC receiver.

RACT Receiver Active

The B1_ch HDLC receiver is active when this bit is set to "1". This bit is write only. The receiver must be in active state in order to receive data.

XMS Transmit Message Start/Continue

In transparent mode, setting this bit initiates the transparent transmission of B1_XFIFO data. The opening flag is automatically added to the message by the B1_ch HDLC controller. Zero bit insertion is performed on the data. This bit is also used in subsequent transmission of the frame.

In extended transparent mode, settint this bit activates the transmission of B1_XFIFO data. No flag, CRC or zero bit insertion is added on the data.

XME Transmit Message End

In transparent mode, setting this bit indicates the end of the whole frame transmission. The B1_ch HDLC controller transmits the data in FIFO and automatically appends the CRC and the closing flag sequence in transparent mode.

In extended transparent mode, setting this bit stops the B1_XFIFO data transmission.

XRST Transmitter Reset

Setting this bit resets the B1_ch HDLC transmitter and clears the B1_XFIFO. The transmitter will send inter frame time fill pattern on B channel. This command also results in a transmit FIFO ready condition.

8.2.4 B1_ch Mode Register B1_MODE Read/Write Address 23H

Value after reset: 00H

7	6	5	4	3	2	1	0
MMS	ITF	EPCM	BSW1	BSW0	SW56	FTS1	FTS0

MDS Message Mode Setting

Determines the message transfer modes of the B1_ch HDLC controller :

0: Transparent mode. In receive direction, address comparison is performed on each frame. The frames with matched address are stored in B1_RFIFO. Flag deletion, CRC check and zero bit deletion are performed. In transmit direction, the data is transmitted with flag insertion, zero bit insertion and CRC generation.

1: Extended transparent mode. In receive direction, all data are received and stored in the B1_RFIFO. In transmit direction, all data in the B1_XFIFO are transmitted without alteration.

ITF Inter-frame Time Fill

Defines the inter-frame time fill pattern in transparent mode.

0: Mark. The binary value "1" is transmitted.

1: Flag. This is a sequence of "01111110".

EPCM Enable PCM Transmit/Receive

0: Disable data transmit/ receive to/from PCM port. The frame synchronization clock is held LOW.

1: Enable data transmit/ receive to/from PCM port. The frame synchronization clock is active.

BSW1–0 B Channel Switching Select

These two bits determine the connection in B1 channel:

BSW1	BSW0	CONNECTION
0	0	layer 1 ↔HDLC
0	1	layer 1 ↔ PCM
1	0	HDLC ↔ PCM
1	1	layer 1 → PCM, PCM → HDLC

Note: The connection with micro-controller is through HDLC controller. When HDLC connects with layer 1, either transparent or extended transparent mode can be used. When connecting with PCM port, the EPCM bit must be set to enable PCM function.

SW56 Switch 56 Traffic

0: The data rate in B1 channel is 64 Kbps.

1: The data rate in B1 channel is 56 Kbps. The most significant bit in each octet is fixed at "1".

Note: In 56 Kbps mode, only transparent mode can be used.

FTS1–0 FIFO Threshold Select

These two bits determine the B1 channel receive and transmit FIFO's threshold setting. An interrupt is generated when the number of received data or the number of transmitted data reaches the threshold value.

FTS1	FTS0	THRESHOLD (BYTE)
0	0	32
0	1	Reserved
1	0	48
1	1	Not allowed

8.2.5 B1_ch Extended Interrupt Register B1_EXIR Read clear Address 24H

Value after reset: 00 H

7	6	5	4	3	2	1	0
	RMR	RME	RDOV			XFR	XDUN

RMR Receive Message Ready

At least a threshold lenth of data has been stored in the B1_RFIFO.

RME Receive Message End

Used in transparent mode only. The last block of a frame has been received. The frame length can be found in B1_RBCH + B1_RBCL registers. The number of data available in the B1_RFIFO equals frame lenth modulus threshold. The result of CRC check is indicated by B1_STAR: CRCE bit.

When the number of last block of a frame equals the threshold, only RME interrupt is generated.

RDOV Receive Data Overflow

Data overflow occurs in the receive FIFO. The incoming data will overwrite the data in the receive FIFO.

XFR Transmit FIFO Ready

This interrupt indicates that a threshold length of data can be written into the B1_XFIFO.

XDUN Transmit Data Underrun

This interrupt occurs when the B1_XFIFO has run out of data. In this case, the W6690 will automatically reset the transmitter and send the inter frame time fill pattern on B channel. The software must wait until transmit FIFO ready condition (via XFR interrupt or XFA bit), re-write data, and issue XMS command to re-transmit the data.

8.2.6 B1_ch Extended Interrupt Mask Register B1_EXIM Read/Write Address 25H

Value after reset: FFH

7	6	5	4	3	2	1	0
	RMR	RME	RDOV			XFR	XDUN

Setting the bit to "1" masks the corresponding interrupt source in B1_EXIR register. Masked interrupt status bits are read as zero when B1_EXIR register is read. They are internally stored and pending until the mask bits are zero.

All the interrupts in B1_EXIR will be masked if the IMASK: B1_EXI bit is set to "1".

8.2.7 B1_ch Status Register B1_STAR Read Address 26H

Value after reset: 20H

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	RDOV	CRCE	RMB		XDOW		XBZ

RDOV Receive Data Overflow

A "1" indicates that the D_RFIFO is overflow. The incoming data will overwrite data in the receive FIFO. The overflow condition will set both the status and interrupt bits. It is recommended that software must read the RDOV bit after reading data from D_RFIFO at RMR or RME interrupt. The software must abort the data and issue a RRST command to reset the receiver if RDOV = 1.

CRCE CRC Error

Used in transparent mode only. This bit indicates the result of frame CRC check:

0: CRC correct

1: CRC incorrect

RMB Receive Message Aborted

Used in transparent mode only. A "1" means that a sequence of seven 1's was received and the frame is aborted by the B1_HDLC receiver. Software must issue RRST command to reset the receiver.

Note: Bits CRCE and RMB are valid only after a RME interrupt and remain valid until the frame is acknowledged via RACK command

XDOW Transmit Data Overwritten

At least one byte of data has been overwritten in the B1_XFIFO. This bit is cleared only by XRST command.

XBZ Transmitter Busy

The B1_HDLC transmitter is busy when XBZ is read as "1". This bit may be polled. The XBZ bit is active when an XMS command is issued and the message has not been completely transmitted.

8.2.8 B1_ch Address Mask Register 1 B1_ADM1 Read/Write Address 27H

Value after reset: 00H

7	6	5	4	3	2	1	0
MA17	MA16	MA15	MA14	MA13	MA12	MA11	MA10

MA17–10 Address Mask Bits

Used in transparent mode only. These bits mask the first byte address comparisons. If the mask bit is "1", the corresponding bit comparison with B1_ADR1 is disabled.

0: Unmask comparison

1: Mask comparison

8.2.9 B1_ch Address Mask Register 2 B1_ADM2 Read/Write Address 28H

Value after reset: 00H

7	6	5	4	3	2	1	0
MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20

MA27–20 Address Mask Bits

Used in transparent mode only. These bits mask the second byte address comparisons. If the mask bit is "1", the corresponding bit comparison with B1_ADR2 is disabled.

0: Unmask comparison

1: Mask comparison

8.2.10 B1_ch Address Register 1 B1_ADR1 Read/Write Address 29H

Value after reset: 00H

7	6	5	4	3	2	1	0
RA17	RA16	RA15	RA14	RA13	RA12	RA11	RA10

RA17-10 Address Bits

Used in transparent mode only. These bits are used for the first byte address comparisons.

8.2.11 B1_ch Address Register 2 B1_ADR2 Read/Write Address 2AH

Value after reset: 00H

7	6	5	4	3	2	1	0
RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20

RA27–20 Address Bits

Used in transparent mode only. These bits are used for the second byte address comparisons.

8.2.12 B1_ch Receive Frame Byte Count Low B1_RBCL Read Address 2BH

Value after reset: 00H

7	6	5	4	3	2	1	0
RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0

RBC7–0 Receive Byte Count

Used in transparent mode only. Eight least significant bits of the total number of bytes in a received frame. These bits are valid only after a RME interrupt and remain valid until the frame is acknowledge via the RACK bit.

8.2.13 B1_ch Receive Frame Byte Count High B1_RBCH Read Address 2CH

Value after reset: 00H

7	6	5	4	3	2	1	0
		LOV	RBC12	RBC11	RBC10	RBC9	RBC8

LOV Message Length Overflow

Used in transparent mode only. A "1" in this bit indicates a received message ≥ 4097 bytes. This bit is valid only after RME interrupt and is cleared by the RACK command.

RBC12–8 Receive Byte Count

Used in transparent mode only. Five most significant bits of the total number of bytes in a received frame. These bits are valid only after a RME interrupt and remain valid until the frame is acknowledge via the RACK bit.

Note: The frame length equals RBC12-0. This length is between 1 to 4096. After a RME interrupt, the number of data available in B1_RFIFO is frame length modulus threshold.

remainder = RBC12-0 MOD threshold

no. of available data = remainder if remainder ≠ 0 or

no. of available data = threshold if remainder = 0

The remainder equals RBC4–0 if threshold is 32.

8.3. B2 HDLC controller

Table 8.7 Register address map: B2 channel HDLC

OFFSET	ACCESS	REGISTER NAME	DESCRIPTION
30	R	B2_RFIFO	B2 channel receive FIFO
31	W	B2_XFIFO	B2 channel transmit FIFO
32	W	B2_CMDR	B2 channel command register
33	R/W	B2_MODE	B2 channel mode control
34	R_clear	B2_EXIR	B2 channel extended interrupt

Table 8.7 Register address map: B2 channel HDLC, continued

OFFSET	ACCESS	REGISTER NAME	DESCRIPTION
35	R/W	B2_EXIM	B2 channel extended interrupt mask
36	R	B2_STAR	B2 channel status register
37	R/W	B2_ADM1	B2 channel address mask 1
38	R/W	B2_ADM2	B2 channel address mask 2
39	R/W	B2_ADR1	B2 channel address 1
3A	R/W	B2_ADR2	B2 channel address 2
3B	R	B2_RBCL	B2 channel receive frame byte count low
3C	R	B2_RBCH	B2 channel receive frame byte count high

Table 8.8 Register summary: B2 channel HDLC

OFFSET	R/W	NAME	7	6	5	4	3	2	1	0
32	W	B2_CMDR	RACK	RRST	RACT			XMS	XME	XRST
33	R/W	B2_MODE	MMS	ITF	EPCM	BSW1	BSW0	SW56	FTS1	FTS0
34	R_clr	B2_EXIR		RMR	RME	RDOV			XFR	XDUN
35	R/W	B2_EXIM		RMR	RME	RDOV			XFR	XDUN
36	R	B2_STAR		RDOV	CRCE	RMB		XDOW		XBZ
37	R/W	B2_ADM1	MA17	MA16	MA15	MA14	MA13	MA12	MA11	MA10
38	R/W	B2_ADM2	MA27	MA26	MA25	MA24	MA23	MA22	MA21	MA20
39	R/W	B2_ADR1	RA17	RA16	RA15	RA14	RA13	RA12	RA11	RA10
3A	R/W	B2_ADR2	RA27	RA26	RA25	RA24	RA23	RA22	RA21	RA20
3B	R	B2_RBCL	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
3C	R	B2_RBCH			LOV	RBC12	RBC11	RBC10	RBC9	RBC8

The B2 channel HDLC register's definitions and functions are the same as those of B1 channel HDLC. Please refer to section 9.2 for a detailed description.

8.4. PNP ISA

Three 8-bit registers are used by the micro-processor to access the PNP registers.

Table 8.9 Register address map: PNP auto-configuration ports

ISA PORT	ACCESS	REGISTER NAME	DESCRIPTION
0279H	W	PNP_ADR	Address index for PNP registers
0A79H	W	PNP_WR	Write data for PNP register
0203H–03FFH	R	PNP_RD	Read data for PNP register

Table 8.10 Register summary: PNP auto-configuration ports

ISA PORT	R/W	NAME	7	6	5	4	3	2	1	0
0279H	W	PNP_ADR	PNP_address							
0A79	W	PNP_WR	write_data							
0203H–03FFH	R	PNP_RD	read_data							

Table 8.11 Register address map: PNP control and configuration registers

In the following tables, the "index" is the value that is programmed in PNP_ADR register.

INDEX (HEX)	ACCESS	REGISTER NAME	DESCRIPTION
00	W	SET_RD	Set read_data port
01	R	SER_ISO	Serial isolation
02	W	CFG_CTL	Configuration control
03	W	WAKE	Wake[CSN]
04	R	R_DATA	Resource data
05	R	STATUS	Status
06	R/W	CSN	Card Select Number
07	R	LDN	Logical device number
30	R/W	ACT	Activate
31	R/W	IO_CHK	I/O range check
60	R/W	IO_H	I/O port baseaddress [15:8]
61	R/W	IO_L	I/O port base address [7:0]
70	R/W	IRQ_N	Interrupt request level select
71	R	IRQ_T	Interrupt request type

Table 8.12 Register summary: PNP control and configuration registers

INDEX	R/W	NAME	7	6	5	4	3	2	1	0
00	W	SET_RD	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2
01	R	SER_ISO	X	X	X	X	X	X	X	X
02	W	CFG_CTL	X	X	X	X	X	CTL2	CTL1	CTL0
03	W	WAKE	M7	M6	M5	M4	M3	M2	M1	M0
04	R	R_DATA	RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0
05	R	STATUS	X	X	X	X	X	X	X	RDY
06	R/W	CSN	N7	N6	N5	N4	N3	N2	N1	N0
07	R	LDN	0	0	0	0	0	0	0	0

Table 8.12 Register summary: PNP control and configuration registers, continued

INDEX	R/W	NAME	7	6	5	4	3	2	1	0
30	R/W	ACT	0	0	0	0	0	0	0	ACT
31	R/W	IO_CHK	0	0	0	0	0	0	ENA	TYPE
60	R/W	IO_H	IA15	IA14	IA13	IA12	IA11	IA10	IA9	IA8
61	R/W	IO_L	IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0
70	R/W	IRQ_N	X	X	X	X	IRN3	IRN2	IRN1	IRN0
71	R/W	IRQ_T	X	X	X	X	X	X	HIGH	LEV

8.4.1 PNP Address Index Register PNP_ADR Write Address 0279H

Value after reset: Undefined

7	6	5	4	3	2	1	0

Bit 7–0 Address Index

This register contains the address index for the desired PNP registers. The PNP registers are accessed by first writing the address into this register, followed by a number of write and/ or read operations. This register is also the write destination of initiation key.

This register is fixed at ISA port 0279H.

8.4.2 PNP Write Data Register PNP_WR Write Address 0A79H

Value after reset: Undefined

7	6	5	4	3	2	1	0

Bit 7–0 Write Data

This register contains the write data for the register specified by the PNP_ADR register.

This register is fixed at ISP port 0A79H.

8.4.3 PNP Read Data Register PNP_RD Read Address 0203H-03FFH

Value after reset: Undefined

7	6	5	4	3	2	1	0

Bit 7–0 Read Data

This register contains the read data from the register specified by the PNP_ADR register.

The location of this register is relocatable at 0203H–03FFH, which is set by the SET_RD register.

8.4.4 Set Read Data Port SET_RD Write Address 00H

Value after reset: Undefined

7	6	5	4	3	2	1	0
RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2

RA9–2 Read_data Port Address

This register is used to set the ISA port address of PNP_RD register. Bits 7–0 become ISA address bits 9–2. Reads from this register are ignored.

8.4.5 Serial Isolation SER_ISO Read Address 01H

Value after reset: Undefined

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Bit 7–0 Don't care

This register is read only. A read to this register causes a PNP card in the isolation state to compare one bit of the board's ID.

8.4.6 Configuration Control CFG_CTL Write Address 02H

Value after reset: Undefined

7	6	5	4	3	2	1	0
X	X	X	X	X	CTL2	CTL1	CTL0

Bit 7–3 Ignore

These bits are not used.

CTL2 Control Bit 2

Writing a "1" to this bit causes the card to reset its CSN to zero.

CTL1 Control Bit 1

Writing a "1" to this bit causes the card to enter the "wait-for-key" state, but the card's CSN is preserved and the logical device configurations are not affected.

CTL0 Control Bit 0

Writing a "1" to this bit resets the logical device's configuration registers to their power-up values, but the card's CSN is unaffected.

This register is write only. The three control bits are automatically reset to zero by hardware after the commands execute.

8.4.7 Wake[CSN] WAKE Write Address 03H

Value after reset: Undefined

7	6	5	4	3	2	1	0
M7	M6	M5	M4	M3	M2	M1	M0

M 7–0

This register is write only. A write to this register will cause all cards that have a CSN that matches the M7–0 to go to change from the sleep state to either the isolation state if M7–0 is zero or the configuration state if M7–0 is not zero. In addition, the pointer to the "Serial identifier" is reset.

8.4.8 Resource Data R_DATA Read Address 04H

Value after reset: Undefined

7	6	5	4	3	2	1	0
RSD7	RSD6	RSD5	RSD4	RSD3	RSD2	RSD1	RSD0

RSD7–0 Resource Data

This register is read only. A read from this register reads the next byte of resource data. The STATUS register must be polled until bit 0 is set before this register may be read.

8.4.9 Status Register STATUS Read Address 05H

Value after reset: Undefined

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	RDY

Bit 7–1 Ignore

These bits are not used.

RDY Ready

When this bit is set, it is okay to read the next data byte from the R_DATA register.

8.4.10 Card Select Number CSN Read/Write Address 06H

Value after reset: 0

7	6	5	4	3	2	1	0
N7	N6	N5	N4	N3	N2	N1	N0

N7–0 Card Select Number

N7–0 is the card's CSN, which is uniquely assigned to this card after the serial isolation process so that each card may be individually selected during a Wake[CSN] command.

8.4.11 Logical Device Number LDN Read Address 07H

Value after reset: 0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

This register has a read-only value of 0, since the card has only one logical device.

8.4.12 Activate ACT Read/Write Address 30H

Value after reset: Undefined

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ACT

ACT Activate

Each logical device has one activate register. The logical device is activated when the ACT bit is set. Bit 7–1 are reserved and must return zero on reads. Before a logical device is activated, I/O range check must be disabled.

8.4.13 I/O Range Check IO_CHK Read/Write Address 31H

Value after reset :Undefined

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ENA	TYPE

This register is used to perform a conflict check on the I/O port range programmed for use by the logical device. Bits 7–2 are reserved and must return zero on read.

ENA Enable I/O Range Check

If set, I/O range check is enabled. I/O range check is valid only when the logical device is deactivated.

TYPE I/O Range Check Drive Type

This bit determines the drive type in response to the I/O read of the logical device's assigned I/O range when I/O range check is in operation.

0: Drive AAH.

1: Drive 55H.

8.4.14 I/O Port Base Address [15:8] IO_H Read/Write Address 60H

Value after reset: Undefined

7	6	5	4	3	2	1	0
IA15	IA14	IA13	IA12	IA11	IA10	IA9	IA8

This register indicates the selected I/O upper limit address bits 15–8 for I/O descriptor 0. When the device is activated, if there is an address match to IO_L and an address match to this register, a chip select signal is generated.

IA15–10 ISA Address 15–10

These bits are not supported since the logical device uses 10-bit address decoding.

IA9–8 ISA Address 9–8

These two bits are the ISA address bits 9–8.

8.4.15 I/O Port Base Address [7:0] IO_L Read/Write Address 61H

Value after reset: Undefined

7	6	5	4	3	2	1	0
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0

This register indicates the selected I/O lower limit address bits 7–0 for I/O descriptor 0. When the device is activated, if there is an address match to IO_H register and an address match to this register, a chip select is generated.

IA 7–2 ISA Address 7–2

These bits are the ISA address bits 7–2.

IA 1–0 ISA Address 1–0

These bits are not supported since the logical device needs four ISA ports. They are read as zeros.

8.4.16 Interrup Request Level Select IRQ_N Read/Write Address 70H

Value after reset :Undefined

7	6	5	4	3	2	1	0
X	X	X	X	IRN3	IRN2	IRN1	IRN0

Bit 7–4 Ignore

IRN3–0 Interrupt Level Number

These bits select the interrupt level number. One selects IRQ1, fifteen selects IRQ15. Zero is not a valid interrupt selection and represents no interrupt selection.

8.4.17 Interrupt Request Type IRQ_T Read Address 71H

Value after reset: 02H

7	6	5	4	3	2	1	0
X	X	X	X	X	X	HIGH	LEV

Bit 7–2 Don't care

HIGH Interrupt High Active

0: The interrupt is LOW active.

1: The interrupt is HIGH active.

LEV Interrupt Level Triggered

0: The interrupt is edge triggered.

1: The interrupt is level triggered.

Notes:

1. This register is read only. Only the edge triggered, HIGH active type is implemented.
2. An edge triggered, HIGH active interrupt must be programmed for ISA compatibility. This means that a valid interrupt generates a LOW to HIGH transition on the interrupt request line.

Remarks about Plug and Play ISA Specification:

According to "Plug and Play ISA Specification", the following requirements must be obeyed :

1. Any unimplemented memory configuration registers must return "zero" on read.
2. Any unimplemented I/O configuration registers must return "zero" on read.
3. Any unimplemented interrupt configuration registers must return "zero" on read.
4. Any unimplemented DMA configuration registers must return "four" on read.

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Rating

PARAMETER	SYMBOL	LIMIT VALUES	UNIT
Voltage on Any Pin with Respect to Ground	V_S	-0.4 to V_{DD} +0.4	V
Ambient Temperature Under Bias	T_A	0 to 70	°C
Maximum Voltage on V_{DD}	V_{DD}	6	V

9.2 Power Supply

The power supply is 5V ±5 %.

9.3 DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5V ±5 %, V_{SSA} = 0V, V_{SSD} = 0V

PARAMETER	SYM.	MIN.	MAX.	UNIT	TEST CONDITIONS	REMARKS
Low Input Voltage	V_{IL}	-0.4	0.8	V		
High Input Voltage	V_{IH}	2.0	V_{DD} +0.4	V		
Low Output Voltage	V_{OL}		0.4	V	I_{OL} = 12 mA	D0–D7 in PNP ISA or ISA modes
High Output Voltage	V_{OH}	2.4		V		
Power Supply Current (power down)	I_{CC}		1.5	mA	V_{DD} = 5V, Inputs at V_{DD}/V_{SS}, No output loads except at SX1, 2 (50 Ω load)	
Power Supply Current (operational)	I_{CC}		17	mA	V_{DD} = 5V, Inputs at V_{DD}/V_{SS}, No output loads except at SX1, 2 (50 Ω load)	
Input Leakage Current	I_{LI}		10	µA	0V < V_{IN} < V_{DD} to 0V	All pins except SX1, 2, SR1,2
Output Leakage Current	I_{LO}		10	µA	0V < V_{OUT} < V_{DD} to 0V	All pins except SX1, 2, SR1, 2
Absolute Value of Output Pulse Amplitude (V_{SX2}–V_{SX1})	V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω R_L = 400 Ω	SX1, 2
Transmitter Output Current	I_X	7.5	13.4	mA	R_L = 5.6 Ω	SX1, 2
Transmitter Output Impedence	R_X	30 23		kΩ Ω	Inactive or during binary one During binary zero (R_L = 50 Ω)	SX1, 2

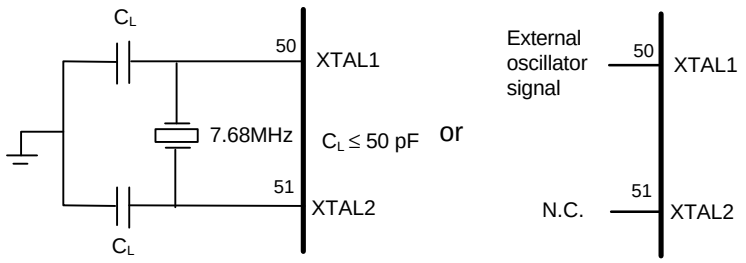
Note: Due to the transformer, the load resistance seen by the circuit is four times R_L.

Capacitances

T_A = 25 °C, V_{DD} = 5 V ±5%, V_{SSA} = 0V, V_{SSD} = 0V, fc = 1 MHz, unmeasured pins grounded.

PARAMETER	SYM.	MIN.	MAX.	UNIT	REMARKS
Input Capacitance	C_{IN}		7	pF	All pins except SR1, 2
I/O pin Capacitance	C_{IO}		7	pF	All pins except SR1, 2
Output Capacitance Against V_{SSA}	C_{OUT}		10	pF	SX1, 2
Input Capacitance	C_{IN}		7	pF	SR1, 2
Load Capacitance	C_L		50	pF	XTAL1, 2

Recommended oscillator circuits



Crystal specifications

PARAMETER	SYMBOL	VALUES	UNIT
Frequency	f	7.680	MHz
Frequency Calibration Tolerance		Max. 100	ppm
Load Capacitance	C_L	Max. 50	pF
Oscillator Mode		Fundamental	

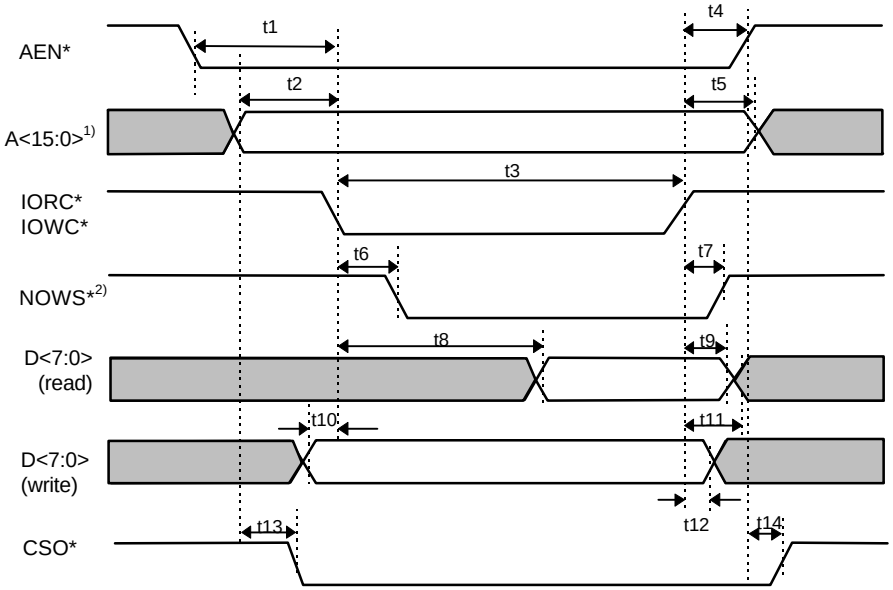
Note: The load capacitance C_L depends on the crystal specification. The typical values are 33 to 47 pF.

External ocsillator input (XTAL1) clock characteristics

PARAMETER	MIN.	MAX.
Duty Cycle	1:2	2:1

9.4 Switching Characteristics

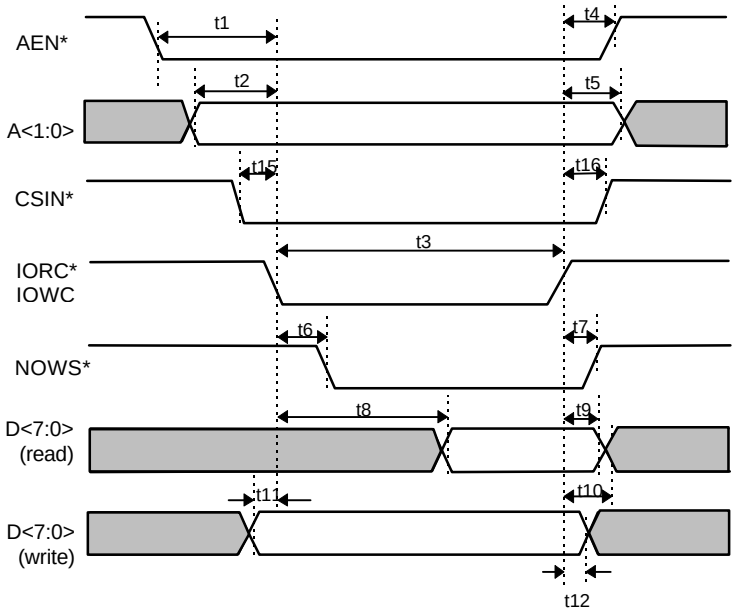
PNP ISA mode bus timing



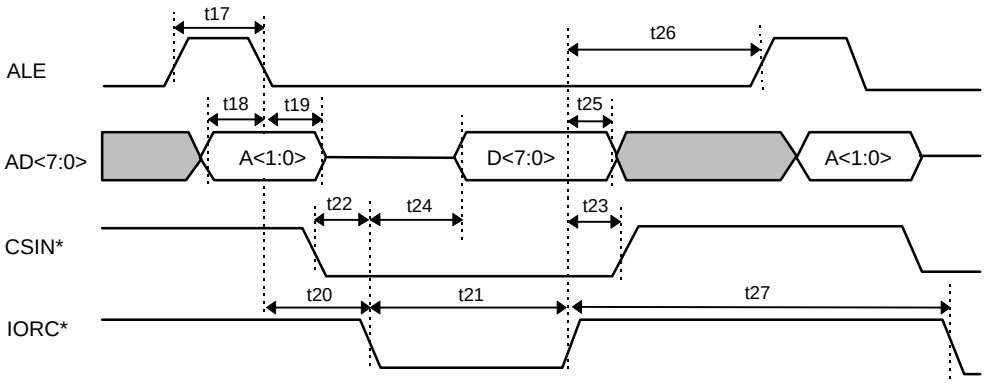
Notes:

1. When doing plug and play operation, A[11:0] are used, otherwise A[15:0] are used.
2. When doing plug and play operation, NOWS* is not asserted. In other cases, NOWS* is asserted which causes a 3 clock cycle I/O access.

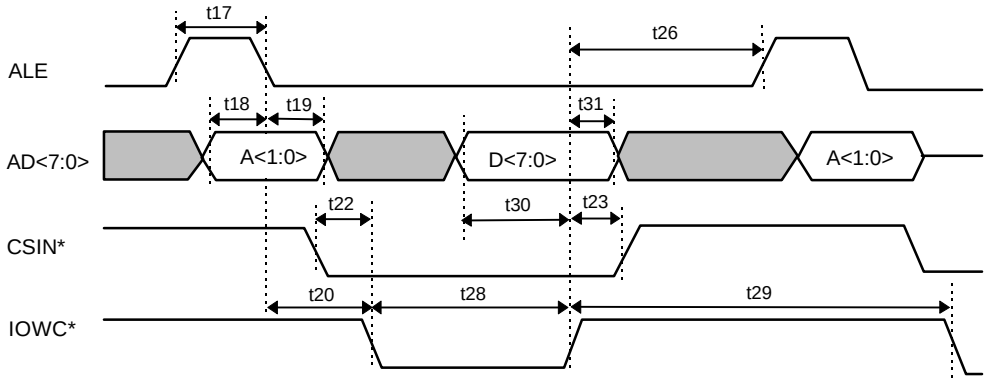
ISA mode bus timing



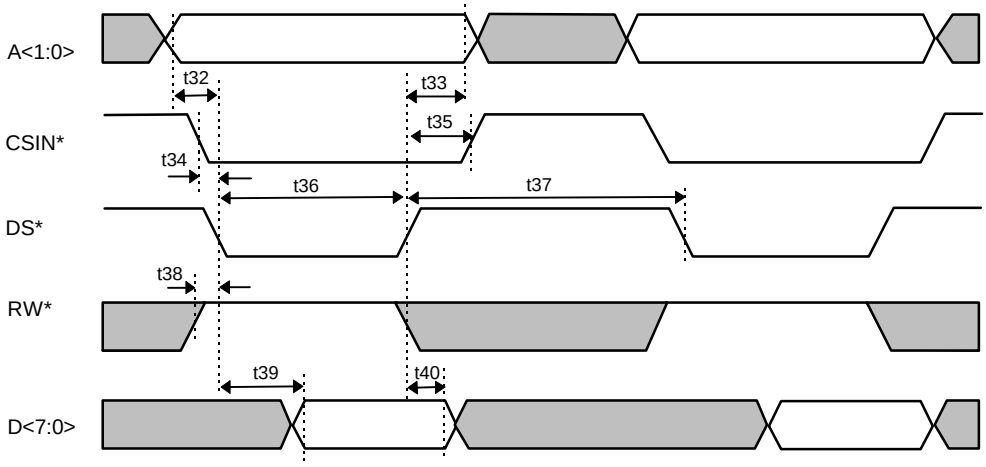
Intel mode read cycle timing



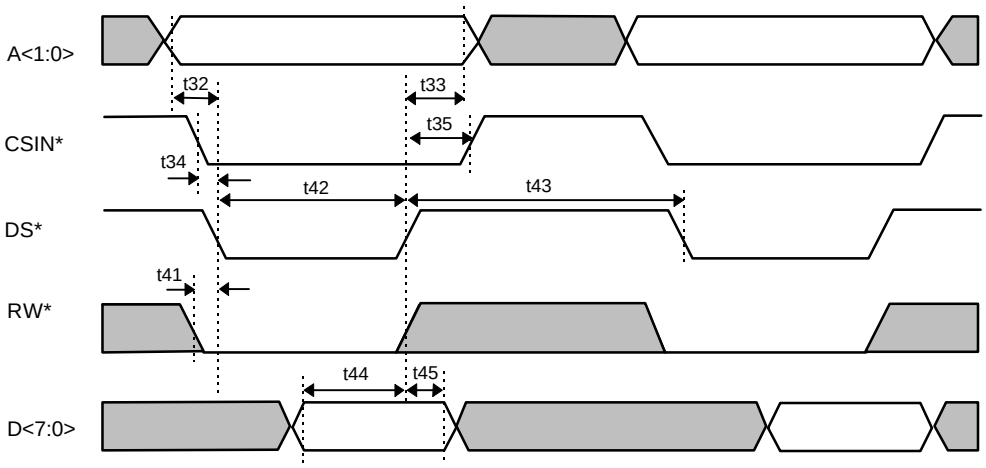
Intel mode write cycle timing



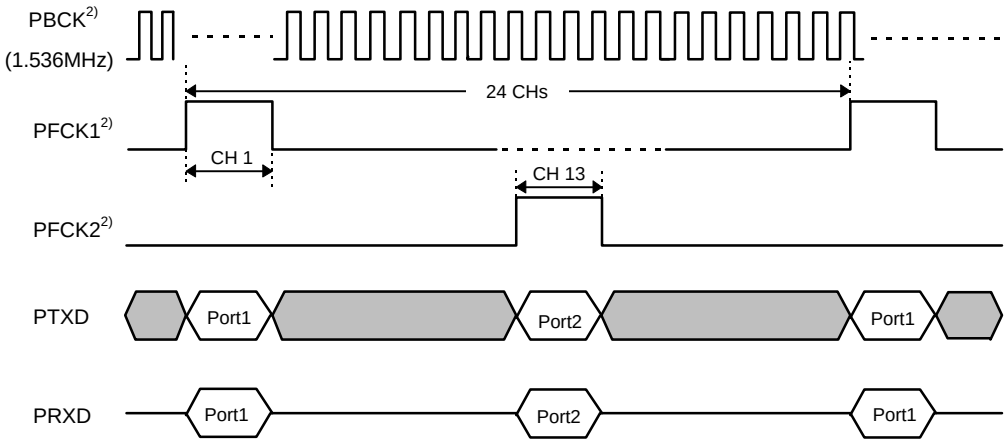
Motorola mode read cycle timing



Motorola mode write cycle timing



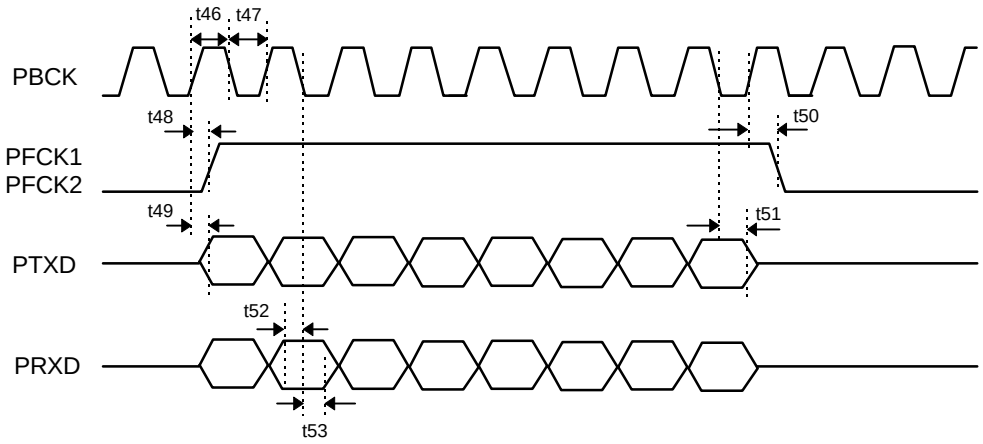
PCM interface timing[1)]



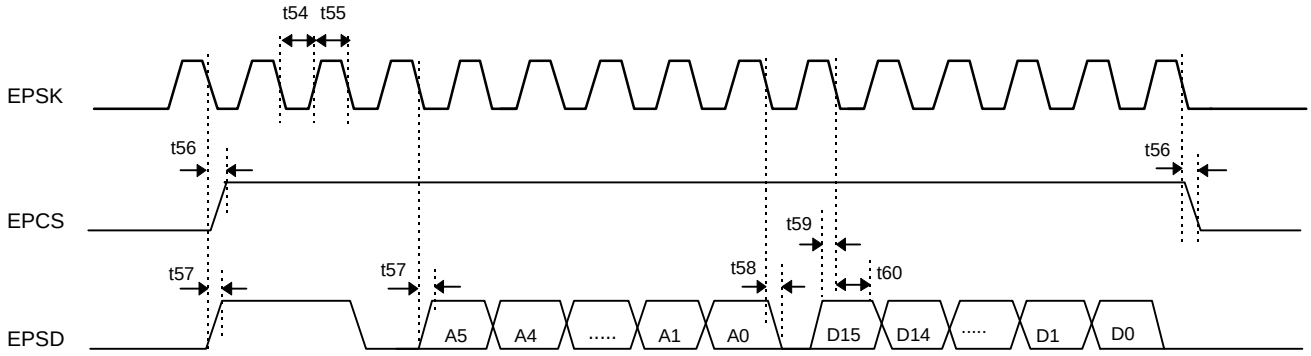
Notes

1. These drawings are not to scale.
2. The frequency of PBCK is 1536 KHz which includes 24 channels of 64 Kbps data. The PFCK1 and PFCK2 are located at channel 1 and channel 13, each with a 8 x PBCK duration.

Detailed PCM timing



EEPROM timing



PARAMETER	PARAMETER DESCRIPTIONS	MIN.	MAX.	REMARKS
t1	AEN* valid before IORC*, IOWC* asserted	100		Unit: nS
t2	A<1:0> valid before IORC*, IOWC* asserted	88		
t3	IORC*, IOWC* asserted before IORC*, IOWC* negated			
t3a	I/O access with 3 clocks	166		
t3b	I/O access with 6 clocks	530		
t3c	I/O access with 7 clocks	650		
t4	IORC*, IOWC* negated before AEN* invalid	30		
t5	IORC*, IOWC* negated before A<1:0> invalid	32		

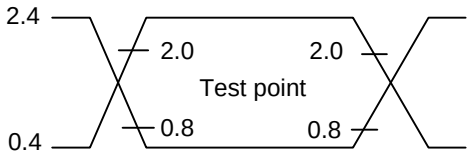
PARAMETER	PARAMETER DESCRIPTIONS	MIN.	MAX.	REMARKS
t6	NOWS* asserted after IORC*, IOWC* valid		20	
t7	NOWS* deasserted after IORC*, IOWC* invalid		20	
t8	IORC* asserted to read data valid		50	
t9	IORC* negated to read data invalid	0		
t10	IORC* negated to data bus float		30	
t11	Write data valid before IOWC* asserted	0		
t12	IOWC* negated to write data invalid	0		
t13	A<15:0> valid to CSO* assserted		20	
t14	A<15:0> invalid to CSO* deasserted		20	
t15	CSIN* valid before IORC*, IOWC* asserted	10		
t16	CSIN* invalid after IORC*, IOWC* deasserted	0		
t17	ALE pulse width	50		
t18	Address setup time to ALE	15		
t19	Address hold time from ALE	10		
t20	Address setup time to IORC*, IOWC*	0		
t21	IORC* pulse width	110		
t22	CSIN* setup time to IORC*, IOWC*	0		
t23	CSIN* hold time from IORC*, IOWC*	0		
t24	Data output delay from IORC*		50	
t25	Data float from IORC*		25	
t26	ALE guard time	15		
t27	IORC* recovery time	70		
t28	IOWC* pulse width	60		
t29	IOWC* recovery time	70		
t30	Data setup time to IOWC*	35		
t31	Data hold time from IOWC*	10		
t32	Address setup time to DS*	25		
t33	Address hold time from DS*	10		
t34	CSIN* setup time to DS*	10		
t35	CSIN* hold time from DS*	10		
t36	DS* read pulse width	110		
t37	DS* read recovery time	70		
t38	RW* setup time to DS* read	0		

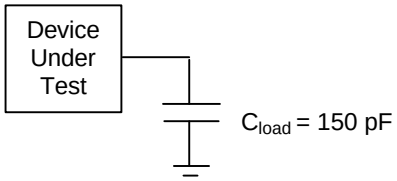
PARAMETER	PARAMETER DESCRIPTIONS	MIN.	MAX.	REMARKS
t39	Data output delay from DS*		110	
t40	Data hold time from DS*		25	
t41	RW* setup time to DS* write	0		
t42	DS* write pulse width	60		
t43	DS* write recovery time	70		
t44	Write data setup time to DS*	35		
t45	Write data hold time from DS*	10		
t46	PBCK pulse high	260		
t47	PBCK pulse low	260		
t48	Frame clock asserted from PBCK		20	
t49	PTXD data delay from PBCK		20	
t50	Frame clock deasserted from PBCK		20	
t51	PTXD hold time from PBCK	10		
t52	PRXD setup time to PBCK	20		
t53	PRXD hold time from PBCK	10		
t54	EPSK low	2500		
t55	EPSK high	2500		
t56	EPCS output delay		30	
t57	EPSD output delay		30	
t58	EPSD tri-state delay		30	
t59	EPSD input setup time	30		
t60	EPSD input hold time	30		

9.5 AC Timing Test Conditions

T_A = 0 to 70 °C, V_{DD} = 5 V ±5 %

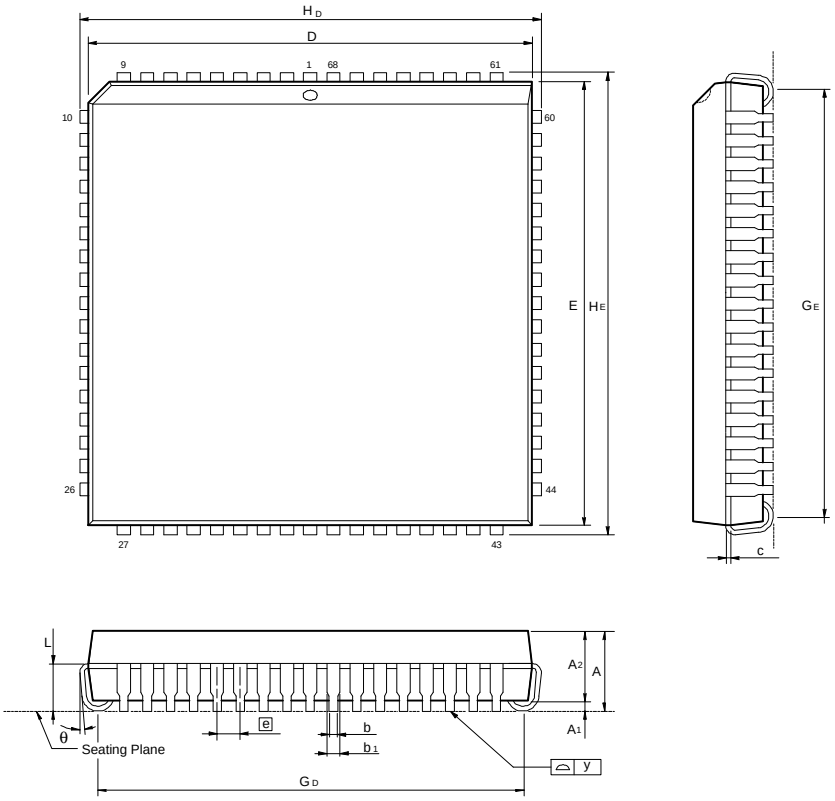
Inputs are driven to 2.4V for logical 1 and 0.4V for logical 0. Measurements are made at 2.0V for logical 1 and 0.8V for logical 0. The AC testing input/output waveforms are shown below:





10. PACKAGE DIMENSIONS

10.1 68-pin PLCC

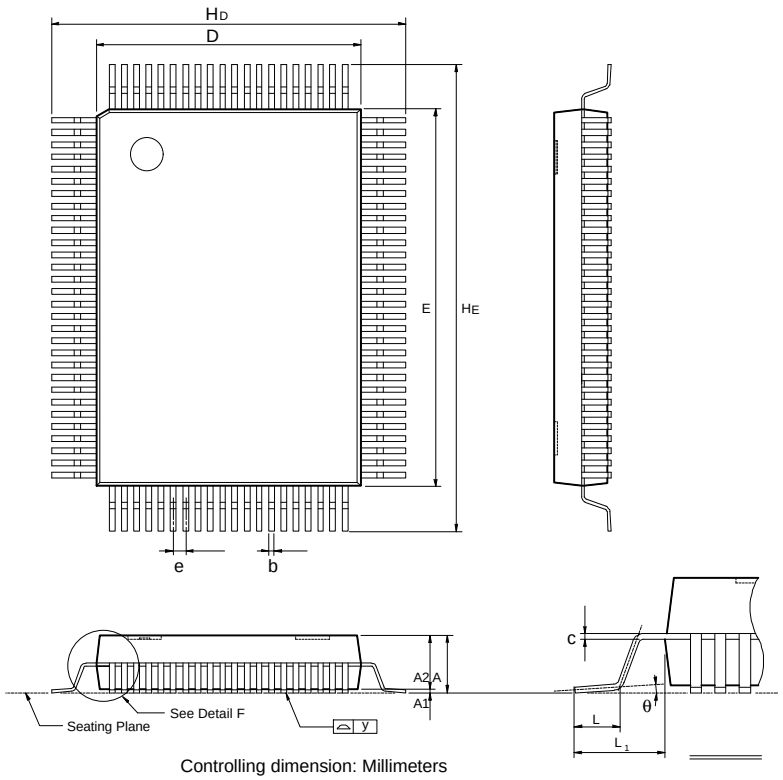


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.143	0.148	0.153	3.63	3.76	3.89
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.949	0.954	0.959	24.10	24.23	24.36
E	0.949	0.954	0.959	24.10	24.23	24.36
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.895	0.915	0.935	22.73	23.24	23.75
G_E	0.895	0.915	0.935	22.73	23.24	23.75
H_D	0.980	0.990	1.000	24.90	25.15	25.40
H_E	0.980	0.990	1.000	24.90	25.15	25.40
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10
θ	0	—	10	0	—	10

10. Package Dimensions, continued

10.2 100-pin QFP

(14 × 20 × 1.4 mm footprint 2.0 mm)



Controlling dimension: Millimeters

Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1035	1.40	1.45
b	0.009	0.013	0.015	0.22	0.32	0.38
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.626	0.630	0.634	15.90	16.00	16.10
H_E	0.862	0.866	0.870	21.90	22.00	22.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1		0.039			1.00	
y	—	—	0.003	—	—	0.08
θ	0°	—	7 °	0°	—	7 °

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