ES1688 *Audio*Drive®

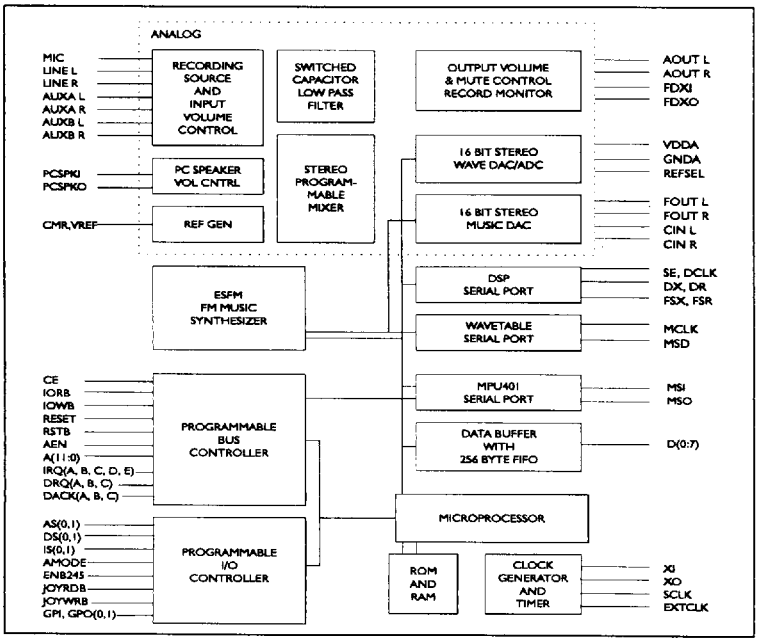
DESCRIPTION

The ES1688 *Audio*Drive® is a single, mixed-signal chip for adding 16-bit stereo audio and 20-voice FM music synthesis to personal computers. The ES1688*Audio*Drive can record, compress, and playback voice, sound and music with built-in 6 channel mixer controls. It consists of an embedded microcontroller, 20 voice high-quality ESFM™ music synthesizer, 16-bit stereo wave A/D and D/A, 16-bit stereo music D/A, MPU401 UART mode serial port, two serial port interfaces to external DSP and external wavetable music synthesizer, DMA control logic with FIFO, and ISA bus interface logic. The AudioDrive® ESFM™ music synthesizer is backward-compatible to the OPL™3 and has enhanced capabilities for superior sound quality with ESFM™ music synthesis. A serial port interface to an external DSP allows the DSP to control the ES1688 full-duplex analog resources for audio effects, compression/decompression, or telephony applications. The MPU401 serial port can be used to interface the host to an external wavetable synthesizer. The ES1688 music D/A can be utilized by an external wavetable synthesizer by using a third ES1688 serial port. The PC speaker volume can be modified by software. Two software address selection modes allow for motherboard plug-and-play configuration. Advanced power management features include suspend/resume from disk or host independent self-timed power down and auto-wakeup. It has three stereo inputs (typically LINE, CD-ROM, and TV) and a mono input for a microphone.

ESFM™ music synthesis provides high-fidelity music and greater realism for every instrument. ESFM™ produces deeper instrument timbre, with layering capabilities for chorusing.

The ES1688 is socket compatible to the ES688 and is available in an industry standard 100-pin PQFP package.

BLOCK DIAGRAM



FEATURES

- Single, mixed-signal, 16-bit stereo VLSI chip
- Record, compress, and playback voice, sound and music
- High-quality 20 voice, ESFM™ FM music synthesizer, patents pending
- 6 channel mixer with stereo inputs for line-in, CD-ROM, TV, and a mono input for microphone
- Mixer controlled record and playback with progammable logarithmic volume controls
- Programmable sample rate from 4 KHz to 44.1 KHz for record and playback
- MPU401 (UART mode), Sound Blaster MIDI interface for wavetable synthesizers and MIDI devices
- Serial Port interface to external DSP optionally controls full-duplex analog operation
- Separate wavetable serial port interface for access to the music DAC
- PC speaker I/O with volume control
- Software address mapping, and DMA and IRQ selections for motherboard plug-and-play
- Programmed I/O and DMA data transfers including demand transfer DMA
- Address decode for joystick
- Advanced power management with self-timed power-down, auto-wakeup, and suspend/resume to and from disk
- Patented ESPCM™ compression
- Supports 3.3 volt or 5.0 volt operation
- Supports Microsoft® Windows™, Windows NT™, Windows for Work Groups, Windows 95 and Windows Sound System
- Supports IBM OS/2®
- Supports PC games and applications for Sound Blaster™ and Sound Blaster Pro™ modes
- Supports FM music synthesis in OPL™ 3 mode

APPLICATIONS

- PC Audio
- Business Audio
- Multimedia PC
- PC Games
- Music Synthesis

IMPLEMENTATION PLATFORMS

- Desktop Systems
- Notebooks
- Motherboards
- Sound Cards
- Multifunction Cards
- Voice/Fax/Modem Cards

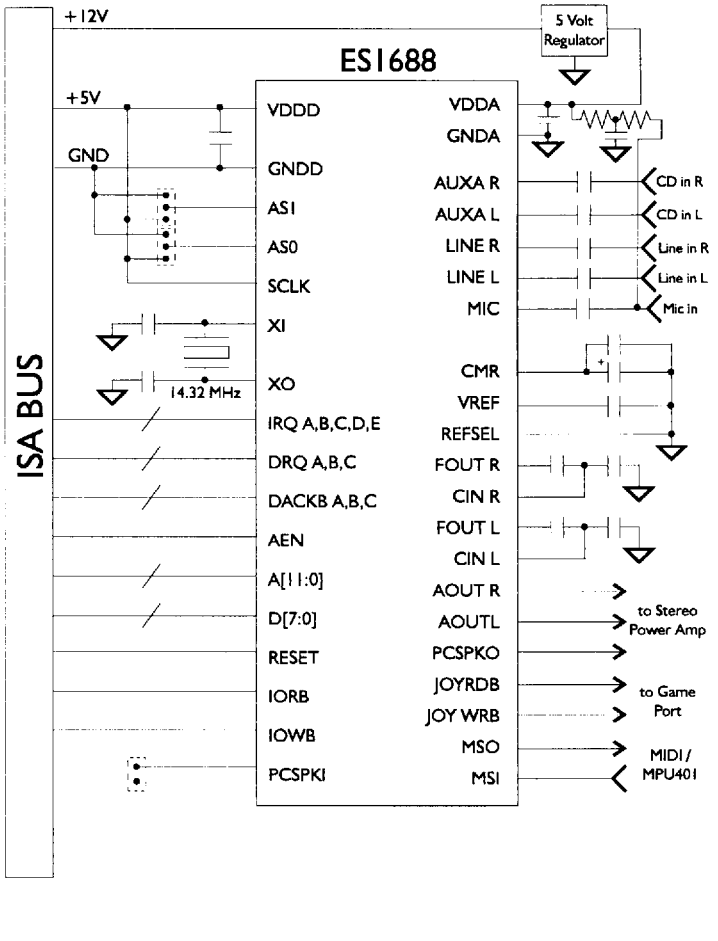
DIGITAL PIN DESCRIPTION

VDDD	I	Digital Supply Voltage (3.0V to 5.5V)
GNDD	I	Digital Ground
JOYWRB	O	Active low decode for joystick, write to port 201H.
JOYRDB	O	Active low decode for joystick, read from port 201H.
GPO0	O	Output that is set low by external reset and thereafter controlled by bit 0 of port 2x7H. Available to system software for power management or other applications.
GPO1	O	Output that is set high by external reset and thereafter controlled by bit 1 of port 2x7H. Available to system software for power management or other applications.
MSI	I	MIDI serial input from Sound Blaster MIDI and MPU401 Interface. Schmitt trigger input with internal pull-up resistor.
MSO	O	MIDI serial output to Sound Blaster MIDI and MPU401 interface.
GPI	I	Reserved General Purpose Input with internal pull-down. Currently no function is assigned to this pin and any connection is acceptable.
RESET	I	Active high reset from ISA bus.
RSTB	O	Inverted RESET output.
SCLK	I	Clock selection input: 0: Clock from EXTCLK input 1: Clock from crystal connected to pins XI and XO
EXTCLK	I	14.32 MHz clock input from ISA bus. Duty cycle must be 40%-60%. No connection if SCLK=1
XO	O	Optional crystal output.
XI	I	Optional crystal input. No connection if SCLK=0.
CE	I	Input with internal pullup. Active high chip enable. When low, all IRQ outputs and DRQ outputs become high impedance, and AEN is forced high internally, thereby disabling the I/O activity to/from the ES1688. Outputs JOYRDB, and JOYWRB become inactive high. Leave unconnected or connected to VDD for normal operation.
IORB	I	Active low read strobe from ISA bus.
IOWB	I	Active low write strobe from ISA bus.
A0-A9	I	Address inputs from ISA bus.
A10-A11	I	Active inputs from ISA bus. The ES1688 requires these pins to be low for all address decodes. These pins have an internal pulldown device enabled when input signal AMODE=0. In case they can float (ES688 compatible designs).
AEN	I	Active low address enable from ISA bus
D0-D7	I/O	Bi-directional data bus. These pins have weak pullup devices to prevent these inputs from floating when not driven.
ENB245	O	Active low output when ES1688 is being read or written to. Intended to be connected to the enable control of an external 74LS245.
DS0, DS1	I	Inputs with internal pull-down devices. These inputs select the DMA channel selected after external reset: DS1 DS0 DRQx/DACKBx Recommended ISA DRQ/DACK 0 0 No DRQ or DACK ------ 0 1 DRQA, DACKBA DRQ0/-DACK0 1 0 DRQB, DACKBB DRQ1/-DACK1 1 1 DRQC, DACKBC DRQ3/-DACK3 DS1=0 and DS0=0 is a special case: no DMA request or interrupt request pin is selected after external reset. Software configuration of interrupt and DMA channels are required.
IS0, IS1	I	Inputs with internal pull-down devices. These inputs select the default interrupt request pin selected after external reset (unless DS1=0 and DS0=0) IS1 IS0 IRQX Recommended ISA IRQ 0 0 IRQA IRQ9 0 1 IRQB IRQ5 1 0 IRQC IRQ7 1 1 IRQD IRQ10
AMODE	I	Input pin with internal pin pull-down device. If this pin is low, then AS0 and AS1 act as in the ES688, namely, they directly select the base address of the ES1688 I/O address bank. If this pin is high, then AS0 and AS1 can be configured to select one of two software address selection techniques.
AS0, AS1	I	Inputs with internal pull-down devices. Along with AMODE, these inputs select the I/O address bank or the software address selection technique. They should be jumpered to VDDD or GNDD: AMODE AS1 AS0 Function 0 0 0 220 base address 0 0 1 230 base address 0 1 0 240 base address 0 1 1 250 base address 1 0 0 220 base address 1 0 1 Read-Sequence-Key address selection 1 1 0 240 base address 1 1 1 System-Control-Register address selection Because the pulldown devices on these pins are weak, in a high noise environment there might be glitching on a floating trace running to an open option switch. In such a case either use an external pulldown resistor or a shorting block that goes to either VDDD or GNDD. Note: when AMODE=0, address inputs A10 and A11 have internal pull-down devices. When AMODE=1, they do not.
IRQ A,B,C,D	O	Active high interrupt request to ISA bus. Unselected IRQ outputs are high impedance. IRQs are selected after external reset based on the settings of input IS1 and IS0 and can be reprogrammed thereafter.
IRQE	O	Active high interrupt request to ISA bus. Reserved for MPU401 use.
DRQ A,B,C	O	Active high DMA request to ISA bus. Unselected DRQ outputs are high impedance. When DMA is not active, the selected DRQ output has a pulldown device that holds the DRQ line inactive unless another device shares the same DRQ line can source enough current to make the DRQ line active. DRQs are selected after external reset based on the settings of inputs DS1 abd DS0, and can be reprogrammed thereafter.
DACKB A,B,C	I	Active low DMA acknowledge inputs from ISA bus
PCSPKI	I	Normally low digital PC speaker signal input. This signal is converted to an analog signal with volume control and appears on analog output PCSPKO.
FSR	I	Input with internal pull-down. Frame Sync for Receive data from external DSP. Programmable for active high or active low.
FSX	I	Input with internal pull-down. Frame Sync for Transmit request from external DSP. Programmable for active high or active low.
DCLK	I	Input with internal pull-down. Serial data clock from external DSP. Typically 2.048 MHz.
DR	I	Input with internal pull-down. Data receive pin from external DSP.
DX	O	Tri-state output. Data Transmit to external DSP. High impedence when not transmitting.
MSD	I	Input with internal pull-down. Music Serial Data from external ES689 Wavetable Music Synthesizer.
MCLK	I	Input with internal pull-down. Music Serial Clock from external ES689 Wavetable Music synthesizer.
SE	I	Input with internal pull-down. Active high to enable serial mode, i.e., enables an external DSP to control analog resources of the ES1688 through the DSP serial interface.

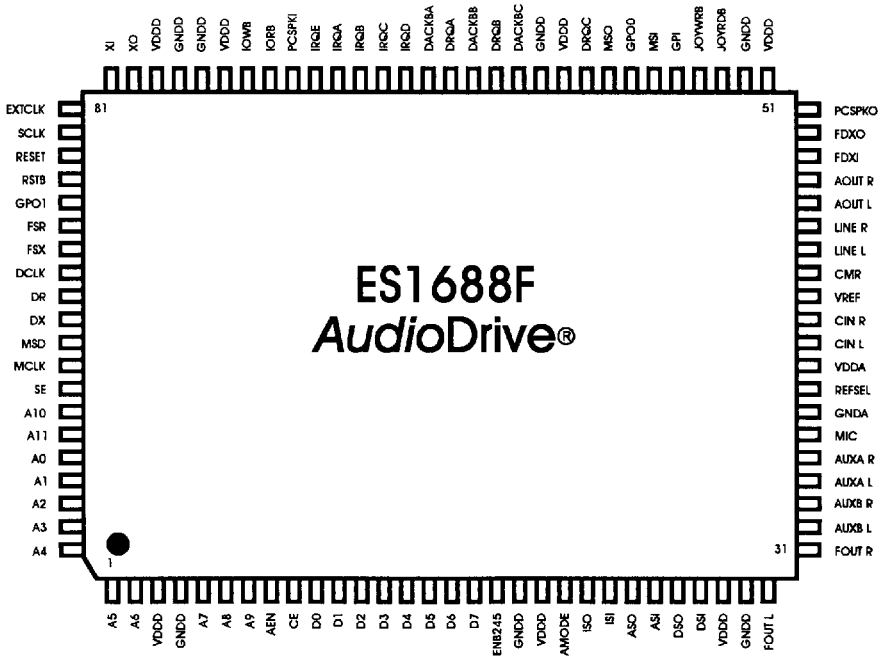
ANALOG PIN DESCRIPTION

VDDA	I	Analog supply voltage (4.5V to 5.5V). Should be greater than or equal to VDDD-0.3V.
GNDA	I	Analog Ground.
MIC	I	Microphone input. MIC has an internal pullup resistor to CMR
LINE L,R	I	Line input left, right. LINE L,R have internal pullup resistors to CMR.
AUXA L,R	I	Auxiliary input left, right. AUXA L,R have internal pullup resistors to CMR. Normally intended for connection to an internal or external CD or CD-ROM analog output.
AUXB L,R	I	Auxiliary input left, right. AUXB L,R have internal pullup resistors to CMR. Normally intended for connection to an external music synthesizer or other line level music source.
FOUT L,R	O	Filter outputs left, right. A.C. coupled externally to CIN L,R in order to remove DC offsets. These outputs have internal series resistors of about 5K ohms. Capacitors to analog ground on these pins can be used to create a lowpass filter pole that removes switching noise introduced by the switched-capacitor filters.
CIN L,R	I	Capacitive coupled inputs left, right. These inputs have internal pullup resistors to CMR of approximately 50K ohms.
VREF	O	Reference generator resistor divider output. Should be bypassed to analog ground with 0.1 uf capacitor.
CMR	O	Buffered reference output. Should be bypassed to analog ground with a 47 uf electrolytic capacitor with a 0.1 uf capacitor in parallel.
AOUT L,R	O	Line level stereo outputs, left, right
REFSEL	I	Option input: Analog GND: normal operation Anlog VDD: reserved
PCSPKO	O	Analog output of PCSPKI with volume control.
FDXO	O	Normally connected to CMR via an internal resistor. Can be programmed to connect internal to FOUT R pin during DSP serial mode.
FDXI	I	Input with internal pullup to CMR. Alternate input to left channel filter stage in DSP serial mode.

TYPICAL CIRCUIT DIAGRAM



PINOUT



ANALOG CHARACTERISTICS

Parameter	Pins	Min	Typ	Max	Unit (conditions)
Reference Voltage	CMR, VREF		2.25		Volts (VDDA =5.0V)
Input Impedance	LINE L/R, AUXA L/R, AUXB L/R, MIC	30K		100K	Ohms
	CIN L/R	35K	50K	65K	Ohms
Output Impedance	FOUT L/R	3.5K	5K	6.5K	Ohms
	AOUT L/R max load for full-scale output range		5K		Ohms
Input Voltage Range	MIC	10		125	mVp-p
	LINE L/R, AUXA L/R, AUXB L/R	0.5		VDDA-0.5	Volts
Output Voltage Range	AOUT L/R full-scale output range	0.5		VDDA-1.0	Volts
Gain	Mic preamp		26		dB
I/O Range	Input Volume Range	0		22.5	dB
	Output Volume Range	-46.5		+10	dB

DIGITAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Conditions
VIH1	Input High Voltage: All Except GPI1	2.0		V	VDDD=min
VIH2	Input High Voltage: GPI1	3.0		V	VDDD=min
VIL	Input Low Voltage		0.8	V	VDDD=max
VOL1	Output Low Voltage, All except D[7:0], DRQx, IRQx		0.4	V	IOL=4mA, VDDD=min
VOH1	Output High Voltage, All except D[7:0], DRQx, IRQx	2.4		V	IOH=-3mA, VDDD=max
VOL2	Output Low Voltage, D[7:0], DRQx, IRQx		0.4	V	IOL=16mA, VDDD=min
VOH2	Output High Voltage, D[7:0], DRQx, IRQx	2.4		V	IOH=-12mA, VDDD=max
VOL3	Output Low Voltage, Select DRQx when DMA inactive		0.4	V	IOL=0.8mA
ICC1	VDDD active		60	mA	VDDD=max osc. rate at 14.32 MHz
ICC2	VDDA active		40	mA	VDDA=max

MAXIMUM RATINGS

Ratings	Symbol	Value	Units
Analog Supply Voltage	VDDA	-0.3 to 7.0	V
Digital Supply Voltage	VDDD	-0.3 to 7.0	V
Input Voltage	VIN	-0.3 to 7.0	V
Operating Temperature Range	TA	0 to 70	Deg C
Storage Temperature Range	TSTG	-50 to 125	Deg C

SERVICE & SUPPORT

- Bundled Drivers:
  - Microsoft Windows
  - Microsoft Windows NT
  - Microsoft Windows Sound System
  - IBM® OS/2®
- Evaluation Kit
- Manufacturing Kit
- Bundled Audio Application Software
- Reference Design

BUNDLED SOFTWARE

- Audio Recorder
- Audio Reminder
- Audio Clip Library
- Chime
- Mixer
- Stopwatch
- Talking Calculator
- Talking Clock
- Timer

AudioDrive®

ESS Technology, Inc.
46107 Landing Parkway
Fremont, CA 94538
TEL: (510) 226-1088
FAX: (510)226-8868