Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

ATM UTOPIA Slave Core V2.0

Features

- UTOPIA Level 1/Level 2 with parity generation/checking. In Level 2, all multi-PHY modes are supported:
  — 1 RxClav/1 TxClav
  — Direct status
  — Multiplexed status polling
- 8-/16-bit bus width
- Programmable cell length
- 25/33/50 MHz operation
- Meets all UTOPIA setup and clock-to-output specifications
- FIFO control/monitoring with the following options:
  — Internal 128 × 9/64 × 17 *ORCA*® FIFOs (scalable)
- Flexible control inputs with options for the following:
  — Internal/external hardwiring
  — Access via a parallel or serial microprocessor interface
- Supports the *ORCA* Series 2 and Series 3 families of FPGAs

Standards Compliance

- ATM forum UTOPIA Level 1 version 2.1
- ATM forum UTOPIA Level 2 version 1.0

Benefits

- Faster development for improved time-to-market with ATM functions
- Lower development cost through design reuse
- *VHDL** source code for easy design integration
- *ORCA*-specific optimization, tailor-made for high performance
- Ample design flexibility using built-in interface and function options
- Verified functionality and standards compliance

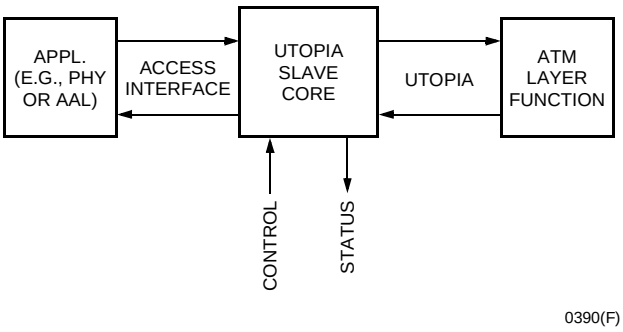

Figure 1. ATM UTOPIA Slave Core Application

Description

The ATM UTOPIA Slave Core from *Modelware*† implements, in modular VHDL, the ATM forum's UTOPIA Level 1 and Level 2 specifications.

The core interfaces to the application (e.g., ATM physical or adaptation layer) via a generic FIFO-like access interface and to the ATM layer via a UTOPIA Level 1 or Level 2 interface (Figure 1). The core uses internal FIFOs for cell buffering and timing transfer between the application and the ATM layer.

The core (using 18-bit internal FIFOs) operates at 50 MHz in an OR2T15A-6 or an OR3T55-7 *ORCA* FPGA.

* *VHDL* is a registered trademark of Gateway Design Automation Corporation.
† *Modelware* is a registered trademark of Modelware, Inc.

Design Package

The ATM UTOPIA slave core package contains:

- *VHDL* source code
- *VHDL* testbench
- Scripts and data files for simulation (behavioral and gate-level), synthesis, and FPGA layout
- Detailed documentation:
  — Reference guide: features, architecture, interfaces, and operation
  — User's guide: simulation, synthesis, and FPGA layout procedures

Required Tools

- MTI V-system for simulation
- *Exemplar LeonardoSpectrum** for synthesis
- Lucent Technologies *ORCA* Foundry for FPGA layout

* *Exemplar* and *LeonardoSpectrum* are trademarks of Exemplar Logic, Inc.

Additional Resources

- ORCA *ATM Physical Layer CSC Application Note* (AP97-050FPGA available from Lucent Technologies)
- ORCA *OR2CxxA and OR2TxxA Series Field Programmable Gate Arrays* Data Sheet (DS98-022), January 1998
- ORCA *OR3CxxA and OR3TxxA Series Field Programmable Gate Arrays* Data Sheet (DS98-163-1), August 1998
- *Asynchronous Transfer Mode: ATM Architecture and Implementation*, Martin et al., Prentice Hall 1996

Ordering Information

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