

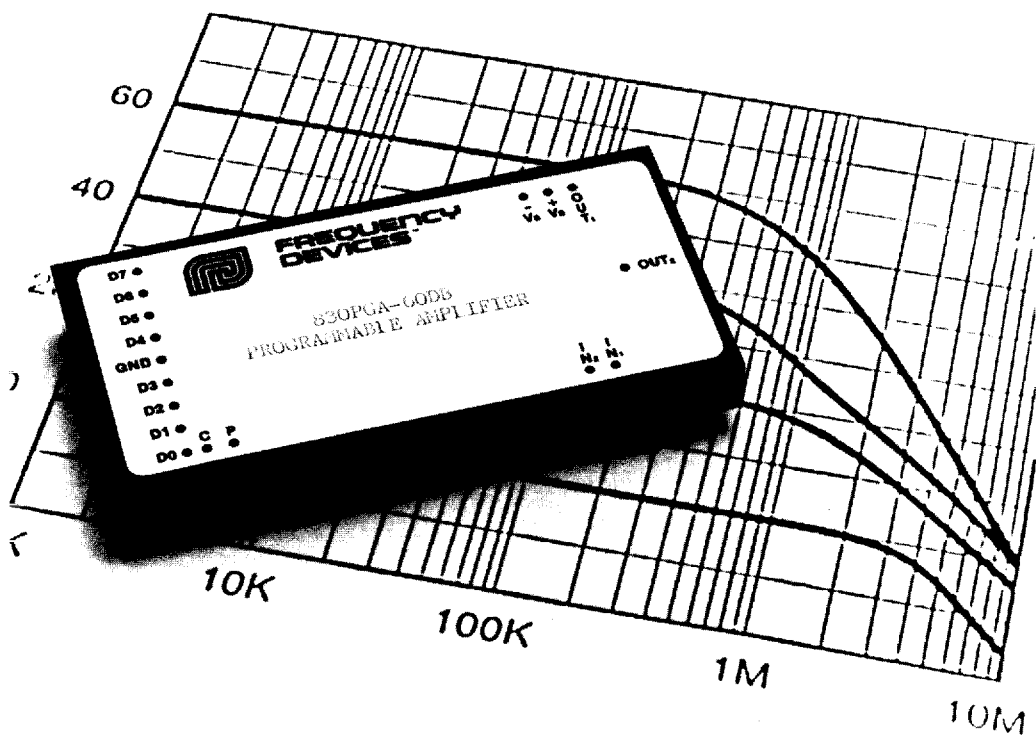


FREQUENCY
DEVICES™

DS - 00830 - 00

830PGA Series

Programmable Gain Amplifiers





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FEATURES

- Adjustable Gain Selection up to 60 dB (1000X) in 0.5, 1.0, or 2.0 dB steps
- Digital Gain Selection (8 bit word) via Industry - Standard CMOS Interface Logic
- Differential Input
- Internally Latched Control Lines
- >100 kHz Full Power Bandwidth
- Plug-In Ready-to-Use

APPLICATIONS

- Data Acquisition
- Test Equipment
- Remote Instrumentation Systems
- Ground Loop Elimination in Remote measurements
- System Dynamic Range and Resolution Improvements
- Telemetry
- Process Control
- Medical, Scientific & Engineering Research
- Digitally controlled autoranging system

General Description

The 830PGA Series programmable amplifiers are digitally controlled gain modules that were designed for conditioning DC-Coupled Wideband Signals in automated systems.

The 830 PGA Series of amplifiers are programmable from:

- 0 dB to 60 dB in 2 dB steps
- or 0 dB to 40 dB in 1 dB steps
- or 0 dB to 20 dB in 0.5 dB steps

and feature a full power bandwidth in excess of 100 kHz.

The gain selection is accomplished with an 8-bit word which can be internally latched for easy microprocessor interfacing, or be simply controlled manually from an 8-bit DIP switch.

Other performance features includes differential input, tight gain and phase matching, and low noise and distortion, making this plug-in ready - to - use amplifier ideal for many signal conditioning applications.

These units contain 8-bit CMOS clocked "D" latches which can be digitally configured to operate in any of three modes:

- a) Transfer frequency control input data into the latches on the STROBE (or CLOCK) rising edge.
- b) As above, but on the STROBE falling edge.
- c) Continuously follow the frequency tuning input data, in a non-latching transparent mode.



Analog Input Characteristics

| | |
|-----------------------------|---|
| Configuration | DC Coupled Differential Input AC Coupled Available |
| Impedance | 1 Meg Ω 47 pF |
| Bias Current | 1 μ A Max. |
| Offset Current | 10 nA Max. |
| Voltage Range | ± 10 V _{PEAK} |
| Maximum Safe Voltage | ± 120 V _{PEAK} |
| Common Mode Rejection Ratio | Typ. 80 dB at 1 kHz Min. 60 dB from 10 Hz to 100 kHz |
| Noise (Referred to input) | 90 μ V _{RMS} (@ 4 MHz Bandwidth) 20 μ V _{RMS} (@ 100 kHz Bandwidth) typ 110 dB down from 7 V _{RMS} |

Analog Output Characteristics

| | |
|--------------------------------------|---|
| Configuration | Single Ended DC Coupled |
| Impedance | <1 Ω |
| Current | ± 10 mA Max. (for linear operation) |
| Initial Offset @ G = 0 dB (@ 25 °C) | < 2 mV Typ. 10 mV Max. |
| Initial Offset @ G = 60 dB (@ 25 °C) | ± 30 mV Typ. ± 80 mV Max. |
| Offset vs. Temp. @ G = 0 dB (RTI) | 50 μ V/°C Typ. 100 μ V/°C Max. |
| Offset vs. Temp. @ G = 60 dB (RTI) | 20 μ V/°C Typ. 40 μ V/°C Max. |



General Analog Characteristics

| | |
|---|----------------------------------|
| Gain | 0 to 60 dB in 2 dB Steps |
| Gain Tolerance | ± 0.02 dB |
| Gain Match (Channel to Channel @ 0 dB) | 0.04 dB from 1 Hz to 100 kHz |
| Gain vs. Temp. @ G = 0 dB | 0.001 dB/°C (0.01 %/°C) |
| Gain vs. Temp. @ G = 60 dB | 0.005 dB/°C (0.05 %/°C) |
| Phase Match (Channel to Channel @ 0 dB) | 0.5° from 1 Hz to 100 kHz |
| Distortion | 0.003% @ 1 kHz 0.02% @ 90 kHz |
| Full Power Bandwidth | 100 kHz |

Power Requirements

| | |
|-------------------|--|
| Rated Voltage | ± 15 Vdc |
| Operating Range | ± 12 Vdc to ± 18 Vdc |
| Max. Safe Voltage | ± 18 Vdc |
| Quiescent Current | ± 38 mA ± 4 mA (7 V _{RMS} In, Output open) |

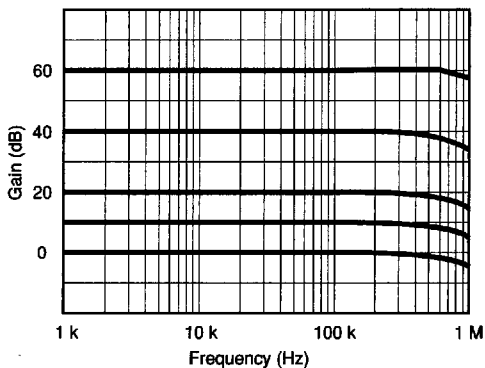
Environmental

| | |
|-----------------------|--------------------------------------|
| Operating Temperature | -25 °C to +85 °C |
| Storage Temperature | -40 °C to +85 °C |
| Altitude | 10,000 Feet |
| Relative Humidity | 0 % to 95 % @ 60 °C (non-condensing) |

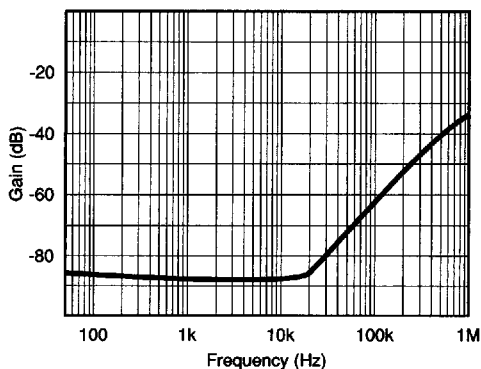


830PGA Series Typical Performance Curves

Frequency Response

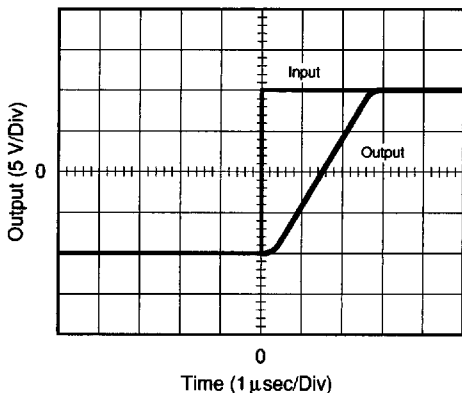


Common Mode Rejection Ratio



Step Response

(Slew Rate $V/T = 10$ to 20 V/ μ s)

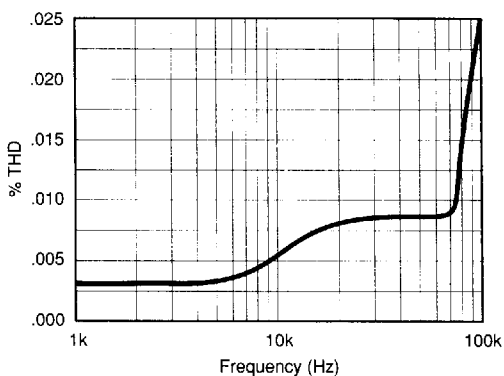


(Slew Rate Increases with Programmed Gain)



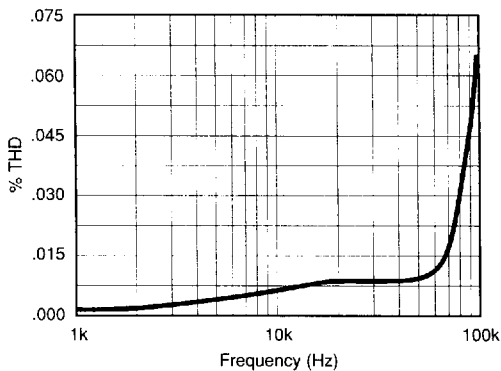
Total Harmonic Distortion

$V_{OUT} = 3.5 \text{ V RMS}$ (Gain = 0 dB)



Total Harmonic Distortion

$V_{OUT} = 6.5 \text{ V RMS}$ (Gain = 0 dB)





DATA LATCH CHARACTERISTICS

Data Control Lines

| | |
|-----------|---|
| Functions | Latch Strobe (C) Transition Polarity (P) |
|-----------|---|

Data Control Modes

| | | |
|----------------------|---------------------------------|------------------------------|
| Mode 1 (Latch) | P = 0; C = 0 → 1 | gain latched on rising edge |
| Mode 2 (Latch) | P = 1; C = 1 → 0 | gain latched on falling edge |
| Mode 3 (Transparent) | P = 0; C = 0 or P = 1; C = 1 | gain follows input |

INPUT DATA LEVELS (CMOS LOGIC)

| Input Voltage (V _S = 15V) | Min. | Max. |
|--------------------------------------|------|------|
| Low Level In | 0 V | 4 V |
| High Level In | 11 V | 15 V |

Input Current

| | | |
|---------------|----------------------------|--------|
| High Level In | - 10 ⁻⁵ μA Typ. | - 1 μA |
| Low Level In | + 10 ⁻⁵ μA Typ. | + 1 μA |

| | | |
|--------------------------|------|--------|
| Input Capacitance | 5 pF | 7.5 pF |
|--------------------------|------|--------|

Latch Response

| | | |
|-------------------------------|-------|---|
| Data Set Up Time ¹ | 25 ns | — |
| Data Hold Time ² | 50 ns | — |
| Strobe Pulse Width | 80 ns | |

PROGRAMMING WEIGHTS (Gain dB)

| Model | LSB | | | | | | | MSB | |
|--------------|-----|-----|-----|-----|-----|-----|-----|-----|--------|
| | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | Steps |
| 830 PGA - 60 | 2 | 4 | 6 | 8 | 10 | 10 | 20 | 20 | 2 dB |
| 830 PGA - 40 | 1 | 2 | 3 | 4 | 5 | 5 | 10 | 20 | 1 dB |
| 830 PGA - 20 | 0.5 | 1.0 | 1.5 | 2.0 | 2.5 | 2.5 | 5.0 | 5.0 | 0.5 dB |

Notes

1. The time data must be present before occurrence of the strobe edge.
2. The time data must be present after occurrence of the strobe edge.



INPUT DATA FORMAT

Gain Select Bits

Positive Logic

Logic "1" = +Vs

Logic "0" = Gnd

Logic threshold typ. = 0.45 Vs

Bit Weighting

D0 = LSB

Least Significant Bit

(Binary-Coded)

D7 = MSB

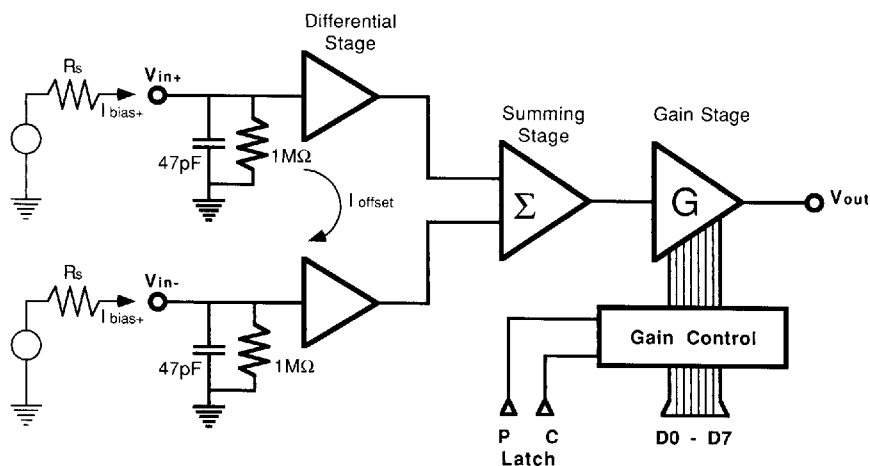
Most Significant Bit

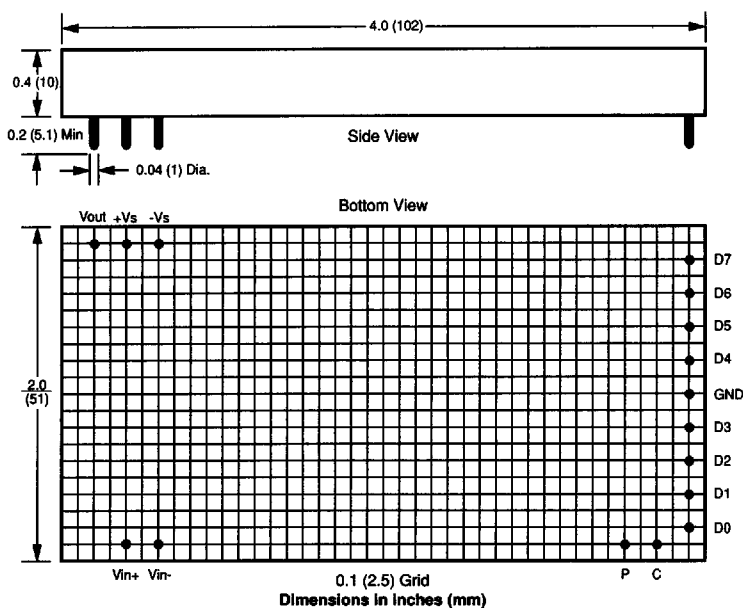
Gain Range

1000:1

Programmed Weighted

Functional Schematic





Pin Designation

Vin+ Input Signal Positive
 Vin- Input Signal Negative
 Vout Output Signal
 "P" Transition Polarity Bit
 "C" Gain Strobe Bit
 + Vs Supply Voltage, Positive
 - Vs Supply Voltage, Negative
 Gnd Power and Signal Return

D₀ Gain Bit 0 (LSB)
 D₁ Gain Bit 1
 D₂ Gain Bit 2
 D₃ Gain Bit 3
 D₄ Gain Bit 4
 D₅ Gain Bit 5
 D₆ Gain Bit 6
 D₇ Gain Bit 7 (MSB)

Grounding

To achieve specified precision, all analog and digital grounds are connected internal to the filter. Should this cause a problem, all digital inputs (C, P, and D0 - D7) can be optically isolated.



Standard Models

| Model Number | Max. Gain (dB) | Gain Step (dB) |
|-----------------|-------------------|-------------------|
| 830PGA-60 | 60 | 2.0 |
| 830PGA-40 | 40 | 1.0 |
| 830PGA-20 | 20 | 0.5 |

Input and Output Options

Suffix Added to Model Number

/AC

/SN

/DF

Description

AC Coupled Input and Output

Single Ended Input

Differential Output

Custom Features

For custom models, please contact our sales office.