VITESSE

SimpliPHY™ GigaBit Ethernet PHY Series

VSC8201 Design Considerations for Wake-on-LAN Compliance

Application Note

Introduction

This application note describes how the VSC8201 single port Gigabit Ethernet PHY should be used to design a WAKE-on LAN compliant PCM based network adapter.

It is assumed that the reader is familiar with the PCI terminology used in this document.

WAKE-on-LAN (WOL) is a protocol used to wake up a PC remotely, i.e to put the system into a fully powered state (S0, working) from a lower power state.

A WOL compliant PCI Gigabit NIC card must be capable of operating under the voltage and current constraints of the D3 (lowest power) power state.

The PCI bus has two power sources namely Vcc (Main) and Vcc (Aux). In the D3 power state, only the Vcc (Aux) is on and the system/device is said to be in 'sleep' mode. In this state the device should draw no more than 375mA of current and should be capable of detecting wake up events.

The following wake-up events must be supported by a WOL compliant GNIC:

- Detection of a change in network link state - The MAC detects this by polling the MII registers of the Ethernet PHY.
- Receipt of a network wake-up frame (required).
- Receipt of a Magic packet (optional).

The major components of a GNIC are the Ethernet MAC and the Ethernet PHY. Of these two, the main source of power consumption is normally the PHY. In 1000BASE-T mode, the current drawn by all industry standard PHYs is more than 375mA; and therefore, to make the network adapter operate under the D3 state, it is imperative that the PHY does not link up in 1000BASE-T when in the 'sleep'/D3 power state.

In order to meet the above mentioned requirements under all conditions, some changes need to be made to the PHY hardware configuration, and the GNIC software driver. These are described in the following sections.

Design Considerations

Theory

The VSC8201 has the following active high hardware control pins that define the link-up capability of the PHY after RESET# deassertion:

- MODE10   - default on-chip pull-up.
- MODE100   - default on-chip pull-up.
- MODE1000   - default on-chip pull-up.
- FRC_DPLX   - default on-chip pull-up.
- ANEG_DIS   - default on-chip pull-down.

If all the pins are kept as no-connects on the board, then by default the VSC8201 always auto-negotiates during the link-up process and advertises 10/100/1000BASE-T Half/Full duplex capabilities.

This configuration is acceptable for a GNIC that is not WOL compliant, i.e. it does not have to support operation in the D3 power state. But for a WOL compliant GNIC, the VSC8201 must have an external pulldown on the MODE1000 pin so that by default the VSC8201 advertises only 10/100BASE-T Half/Full duplex capabilities. This eliminates the possibility of a link up in 1000BASE-T mode and enables operation in D3 power state.

Once the VSC8201 is under software driver control, the driver can write to MII registers and enable 1000BASE-T operation.

The GNIC can go into D3 sleep mode in the following ways:

- ACPI shutdown - In this case the driver configures the VSC8201 into 10/100BASE-T operating mode by writing to the MII registers of the VSC8201 before the Vcc (Main) supply goes off.

- Abnormal shutdown - In this case the main power Vcc (Main) is lost suddenly and driver does not configure the VSC8201 in 10/100BASE-T operating mode by writing to the MII registers of the VSC8201. It is assumed that on sudden loss of Vcc (Main) the MAC will reset the VSC8201 by driving a pulse on the RESET# pin of the VSC8201. Upon deassertion of RESET# the VSC8201 re-reads the hardware configuration pins, which should be set as shown in figure 1 below.

VSC8201 Hardware Configuration

The MODE1000 pin must be pulled down on the board so that 1000BASE-T capability is not advertised by default during auto-negotiation.
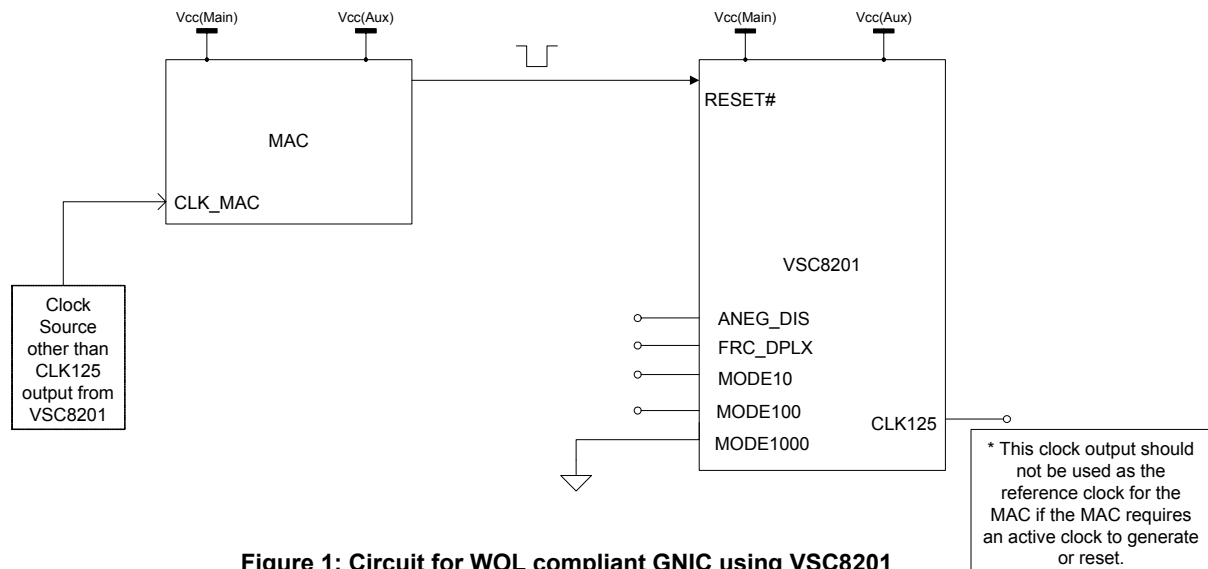

Figure 1: Circuit for WOL compliant GNIC using VSC8201

VSC8201 Software Configuration

By default the VSC8201's advertisement capabilities are defined by the hardware control pins. In order to change the default advertisement capabilities of the VSC8201 by writing to the MII registers, the control must be transferred from the hardware pins to the MII registers.

Once the driver is loaded it must set MII Register 28.2 (MODE/Duplex pin priority select) of the VSC8201. After this the GNIC driver can override the default settings of the auto-negotiation advertisement by writing to MII registers 4 and 9 of the VSC8201.

Constraints

The VSC8201 outputs a 125MHz clock for use by the MAC or an external device on the board if needed. This clock is enabled only when the RESET# pin of the VSC8201 is deasserted.
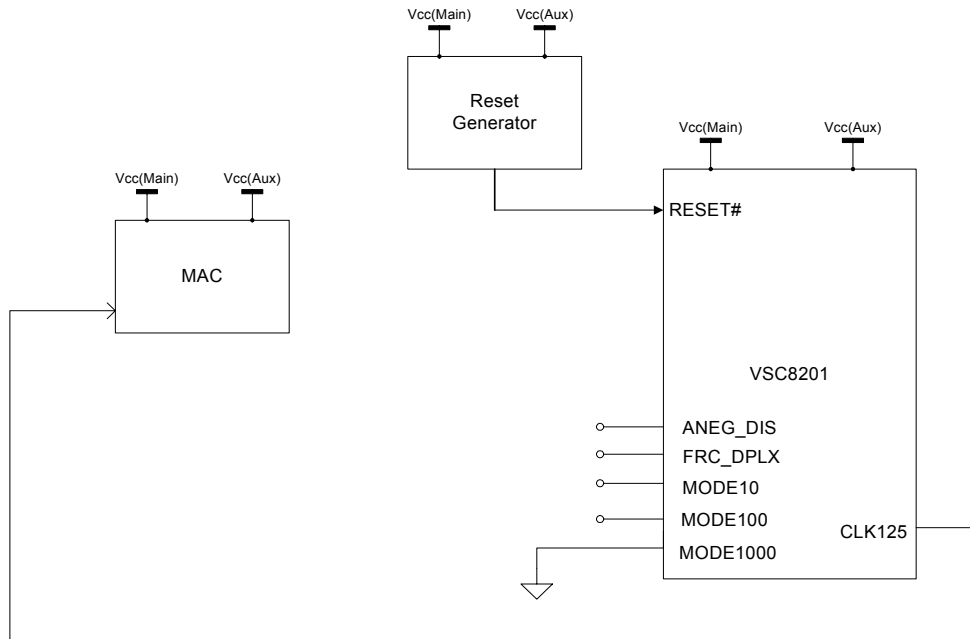
VSC8201 is compliant with WOL power requirements in 10/100BASE-T operating mode with the CLK125 output enabled.

Since the VSC8201 requires a reset (which is generated by the MAC) after abnormal shutdown to reconfigure the VSC8201 to advertise only 10/100BASE-T operating speeds, it may not be possible to supply the MAC with 125Mhz clock generated by the VSC8201 and still be WOL compliant under all operating conditions.

If the MAC requires that the clock be active in order to generate a reset pulse during abnormal shutdown, then the 125MHz clock from the VSC8201 should not be used.

The 125MHz clock can be used as a reference clock for the MAC on non-WOL cards where the RESET# of the VSC8201 is connected to the supply and not controlled by the MAC.

Alternatively, an external reset generator could be used to generate a reset pulse to the VSC8201 whenever an abnormal shutdown is detected. In this instance, the 125MHz clock output from the VSC8201 could be used as a clock source for the MAC.

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