NEC

MOS INTEGRATED CIRCUIT

μPD160970

8-ch level shift driver IC

DESCRIPTION

The μPD160970 is a level shift driver IC for LTPS (low-temperature polysilicon) TFT-LCDs featuring a 2-level output function and incorporates eight on-chip level shifters. This IC realizes a 20 V MAX. withstanding voltage due to a high-withstanding-voltage CMOS process and has an output ON-resistance and switching characteristics ideal for TFT driving in LCD panels.

FEATURES

- High withstanding voltage : 20 V (MAX.)
- Supports low-voltage input (logic power supply voltage : 3.0 to 3.6 V)
- Includes 8 level shifters (among which 2 circuits can switch between normal and inverted output)
- Small thin package : 24-pin plastic TSSOP (5.72 mm (225))

ORDERING INFORMATION

Part Number	Package
μPD160970MA-6A5	24-pin plastic TSSOP (5.72 mm (225))

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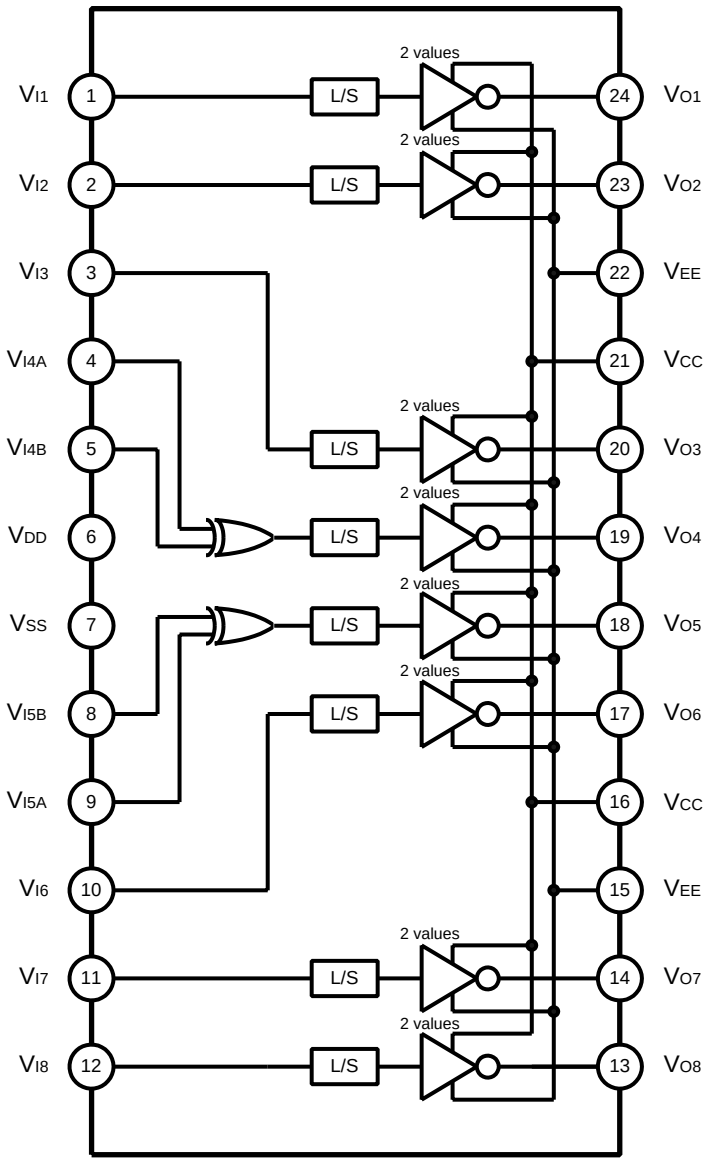
The mark ★ shows major revised points.

1. BLOCK DIAGRAM / PIN CONFIGURATION

• 24-pin plastic TSSOP (5.72 mm (225))

μPD160970MA-6A5



L/S : Level shifter (V_{DD}→V_{CC}, V_{SS}→V_{EE})

2. PIN FUNCTIONS

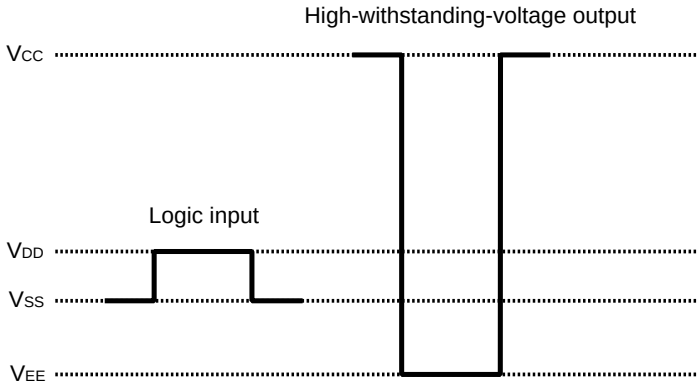
Pin Name	Pin Symbol	I/O	Function	Pin Name	Pin Symbol	I/O	Function
V_{I1}	1	Input	Logic input	V_{O8}	13	Output	High-withstanding-voltage output
V_{I2}	2			V_{O7}	14		
V_{I3}	3			V_{EE}	15	–	Negative power supply for high-withstanding-voltage block
V_{I4A}	4			V_{CC}	16	–	Positive power supply for high-withstanding voltage block
V_{I4B} Note	5			V_{O6}	17	Output	High-withstanding-voltage output
V_{DD}	6	–	Power supply for logic block	V_{O5}	18		
V_{SS}	7	–	Logic ground	V_{O4}	19		
V_{I5B} Note	8	Input	Logic input	V_{O3}	20		
V_{I5A}	9			V_{CC}	21	–	Negative power supply for high-withstanding-voltage block
V_{I6}	10			V_{EE}	22	–	Positive power supply for high-withstand-voltage block
V_{I7}	11			V_{O2}	23	Output	High-withstanding-voltage output
V_{I8}	12			V_{O1}	24		

Note Use the V_{I4B} and V_{I5B} pins at the DC level.

3. Relation of logic input and High-withstanding-voltage output

3.1 V_{I1} to V_{I3}, V_{I6} to V_{I8}

V_{In}	V_{On}
L	V_{CC}
H	V_{EE}



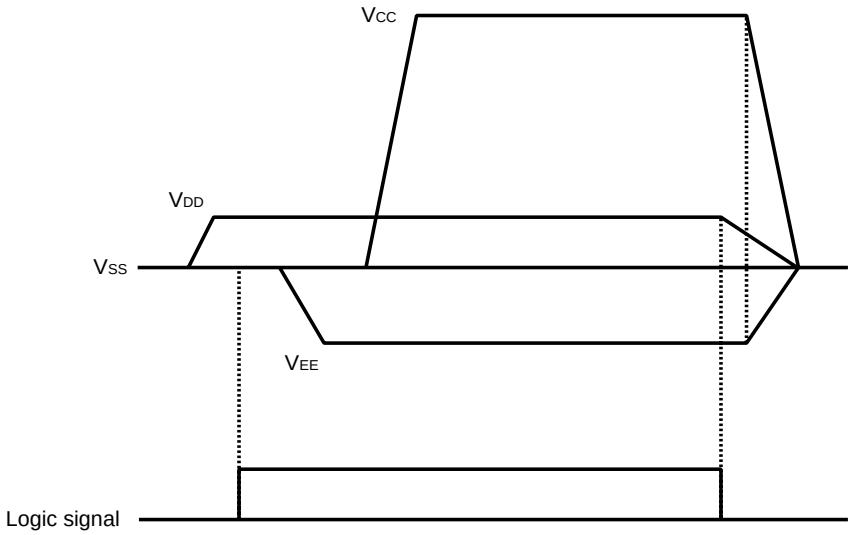
3.2 V_{I4A}/V_{I4B}, V_{I5A}/V_{I5B}

V_{InA}	V_{InB}	V_{On}
L	L (DC)	V_{CC}
H		V_{EE}
L	H (DC)	V_{EE}
H		V_{CC}

4. Usage Cautions

(1) The power-on sequence is $V_{SS} \rightarrow V_{DD} \rightarrow$ logic signal $\rightarrow V_{EE} \rightarrow V_{CC}$, and the power-off sequence is the reverse sequence.

- V_{SS} and V_{DD}, and V_{EE} and V_{CC} can be powered on simultaneously.
- To prevent an abnormal output operation, it is recommended to fix the logic input during the transition phase of V_{EE} and V_{CC} to either "H" or "L".



Remark The term "logic signal" as used above includes not only the rising edge/falling edge of the signal, but also "H" or "L" level input.

(2) To ensure the switching characteristics of the V_{I4A}/V_{I4B} and V_{I5A}/V_{I5B} signal input, be sure to make the V_{I4B} and V_{I5B} pins DC input. Also, be sure to fix unused input pins to "H" or "L".

(3) Perform thorough evaluation with the actual device for simultaneous switching of multiple output circuits, bearing in mind the allowable output current during switching.

(4) The output transistors in this device are designed for an impedance of several tens of ohms. Therefore, if driving a large load, IC malfunction and IC destruction or degradation may result owing to the influence of an output current of several hundred mA_{p-p} per output. To prevent such malfunction from occurring, a number of countermeasures can be implemented, including the following.

<1> Use a large-capacitance decoupling capacitor with superior high-frequency characteristics.

<2> Insert in series a damping resistor for limiting the output current between the output pin and the load.

Since the optimum values of constants differ depending on the equipment, determine the correct constants based on careful evaluation.

(5) Be sure to externally short power-supply pins for which several exist (V_{CC} and V_{EE}).

(6) Do not use the device with multiple output pons shorted. This may cause IC malfunction, destruction, or degradation.

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD}	–0.5 to +4.5	V
Positive power supply for high -withstanding-voltage block	V_{CC}	–0.5 to +17.0	V
Negative power supply for high -withstanding-voltage block	V_{EE}	–8.0 to +0.5	V
Bias power supply for high -withstanding-voltage block	V_{CC} -V_{EE}	–0.5 to +25.0	V
Input Voltage	V_I	–0.5 to V_{DD} + 0.5	V
Output Voltage	V_O	V_{EE} – 0.5 to V_{CC} + 0.5	V
Operating Ambient Temperature	T_A	–10 to +60	°C
Storage Temperature	T_{stg}	–40 to +125	°C
Power Dissipation	P_d	500[Note]	mW

Note When a glass epoxy board (100 mm x 100 mm x 1.0 mm, copper-plated area of 15%) is mounted.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –10 to +60°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
	V_{CC}		9.5	11.5	13.5	V
	V_{EE}		–6.5	–5.5	–4.5	V
	V_{CC} -V_{EE}		14.0	17.0	20.0	V
Clock Frequency	f_{CLK}				200	kHz

Electrical Characteristics (T_A = –10 to +60°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, V_{CC} = 11.5 V ± 1.0 V, V_{EE} = –5.5 V ± 0.5 V, t_r = t_f ≤ 5.0 ns)

Parameter	Symbol	Conditions		MIN.	TYP.[Note]	MAX.	Unit
Low-Level Input Voltage	V_{IL}	All input pins		V_{SS}		0.2 V_{DD}	V
High-Level Input Voltage	V_{IH}	All input pins		0.7 V_{DD}		V_{DD}	V
Low-Level Output Voltage	V_{OL}	I_{OL} = +1.0 mA, All output pins			–5.42	–4.87	V
High-Level Output Voltage	V_{OH}	I_{OH} = –1.0 mA, All output pins		10.37	11.42		V
Output ON Resistance	R_{ON}	I_O = ±1.0 mA, All output pins			80	130	Ω
Static Current	I_{DD}	V_I = V_{SS} no load	V_{DD}		0.1	10	μA
	I_{CC}		V_{CC}		0.1	10	μA
Input Leak Current	I_{IL}	V_I = V_{DD} or V_{SS}, All input pins		–1.0		1.0	μA
★ Input Capacitance	C_I				7		pF

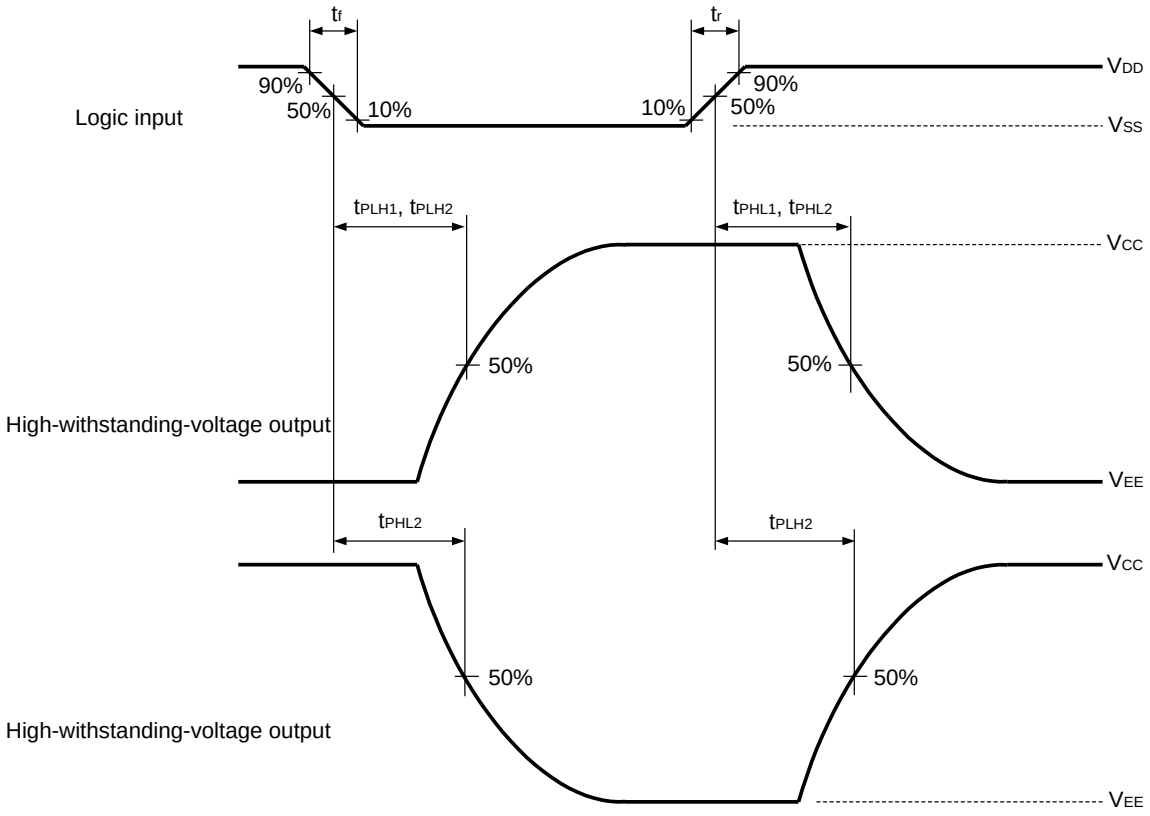
Note The TYP. value is a reference value when T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 11.5 V, V_{EE} = –5.5 V.

Switching Characteristics (T_A = –10 to +60°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, V_{CC} = 11.5 V ± 1.0 V, V_{EE} = –5.5 V ± 0.5 V, $t_r = t_f \leq 5.0$ ns)

Parameter	Symbol	Condition	MIN.	TYP.[Note]	MAX.	Unit
Output delay time1	t_{PHL1}	All output pins, no load,		35	140	ns
	t_{PLH1}	V_{O1}-V_{O3}, V_{O6}-V_{O8}		45	140	ns
Output delay time2	t_{PHL2}	All output pins, no load,		40	140	ns
	t_{PLH2}	V_{O4}, V_{O5}		50	140	ns

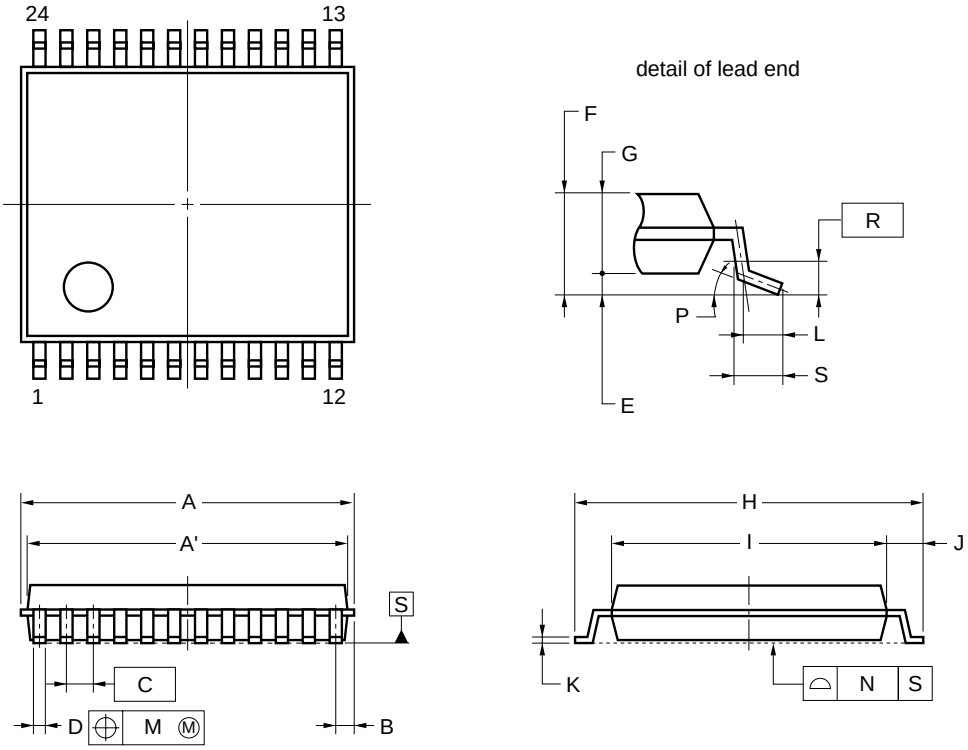
Note The TYP. value is a reference value when T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 11.5 V, V_{EE} = –5.5 V.

Switching Characteristics Waveform



6. PACKAGE DRAWING

24-PIN PLASTIC TSSOP (5.72 mm (225))



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.10
A'	6.5±0.1
B	0.575
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
H	6.4±0.1
I	4.4±0.1
J	1.0±0.1
K	0.17±0.025
L	0.5
M	0.10
N	0.08
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.6±0.15

P24MA-50-6A5

7. RECOMMENDED MOUNTING CONDITIONS

The μPD160970 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

Recommended Soldering Conditions for Surface Mounting Type

μPD160970MA-6A5 : 24-pin plastic TSSOP (5.72 mm (225))

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature : 235°C, Time : 30 seconds max. (at 210°C or higher), Count : Three times or less, Exposure, limit : None, Flux : Rosin flux with low chlorine (0.2 Wt% or below) recommended	IR35-00-3
VPS	Package peak temperature : 215°C, Time : 40 seconds max. (at 200°C or higher), Count : Three times or less, Exposure, limit : None, Flux : Rosin flux with low chlorine (0.2 Wt% or below) recommended	VP15-00-3
Wave Soldering	Package peak temperature : 260°C, Time : 10 seconds max., Preheating temperature : 120°C max., Exposure, limit : Once, Flux : Rosin flux with low chlorine (0.2 Wt% or below) recommended	WS60-00-1

Caution Do not use different soldering methods together.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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