

STC**Very Low Power/Voltage CMOS SRAM
128K X 8 bit****STC62WV1024****■ FEATURES**

- Wide Vcc operation voltage : 2.4V ~ 5.5V
- Very low power consumption :
 - Vcc = 3.0V C-grade : 17mA (@55ns) operating current
 - I-grade : 18mA (@55ns) operating current
 - C-grade : 14mA (@70ns) operating current
 - I-grade : 15mA (@70ns) operating current
 - 0.1uA (Typ.) CMOS standby current
 - Vcc = 5.0V C-grade : 46mA (55ns) operating current
 - I-grade : 47mA (55ns) operating current
 - C-grade : 38mA (70ns) operating current
 - I-grade : 39mA (70ns) operating current
 - 0.6uA (Typ.) CMOS standby current
- High speed access time :
 - 55 55ns
 - 70 70ns
- Automatic power down when chip is deselected

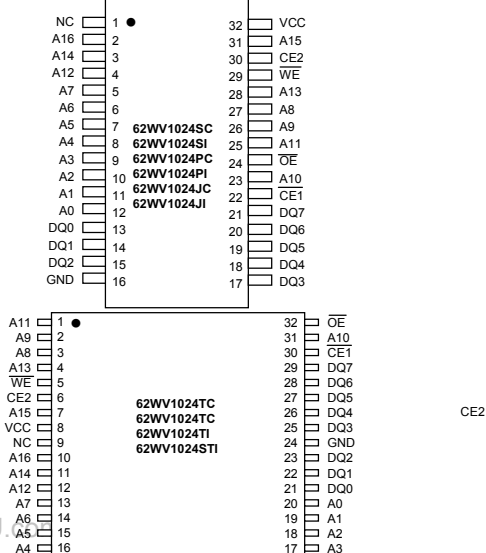
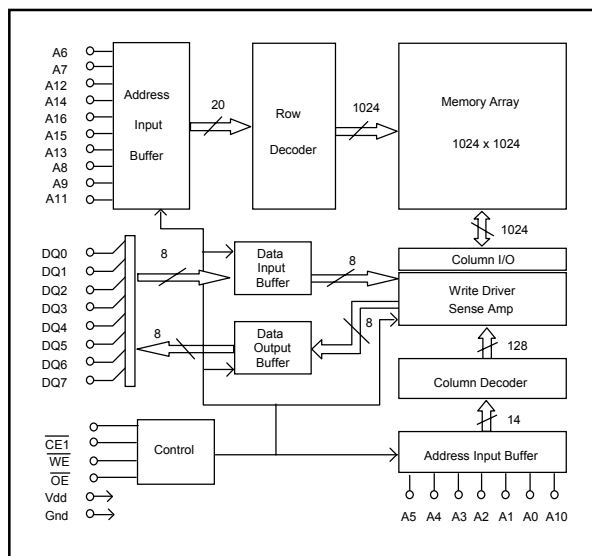
- Easy expansion with CE2, $\overline{CE1}$, and \overline{OE} options
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.5V

■ DESCRIPTION

The STC62WV1024 is a high performance, very low power CMOS Static Random Access Memory organized as 131,072 words by 8 bits and operates from a wide range of 2.4V to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.1uA at 3V/25°C and maximum access time of 55ns at 3V/85°C. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE1}$), an active HIGH chip enable (CE2), and active LOW output enable (\overline{OE}) and three-state output drivers. The STC62WV1024 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The STC62WV1024 is available in DICE form, JEDEC standard 32 pin 450mil Plastic SOP, 300mil Plastic SOJ, 600mil Plastic DIP, 8mm x13.4 mm STSOP and 8mmx20mm TSOP.

■ PRODUCT FAMILY

| PRODUCT FAMILY | OPERATING TEMPERATURE | Vcc RANGE | SPEED (ns) | POWER DISSIPATION | | | | PKG TYPE |
|----------------|-----------------------|-------------|------------|-----------------------|----------|----------------------|----------------|----------|
| | | | | STANDBY (Iccsb1, Max) | | Operating (Icc, Max) | | |
| | | | | Vcc=5.0V | Vcc=3.0V | Vcc=3V 70ns | Vcc=5V 70ns | |
| STC62WV1024SC | +0 °C to +70 °C | 2.4V ~ 5.5V | 55/70 | 8.0uA | 1.3uA | 14mA | 38mA | SOP-32 |
| STC62WV1024TC | | | | | | | | TSOP-32 |
| STC62WV1024STC | | | | | | | | STSOP-32 |
| STC62WV1024PC | | | | | | | | PDIP-32 |
| STC62WV1024JC | | | | | | | | SOJ-32 |
| STC62WV1024DC | | | | | | | | DICE |
| STC62WV1024SI | -40 °C to +85 °C | 2.4V ~ 5.5V | 55/70 | 20uA | 2.5uA | 15mA | 39mA | SOP-32 |
| STC62WV1024TI | | | | | | | | TSOP-32 |
| STC62WV1024STI | | | | | | | | STSOP-32 |
| STC62WV1024PI | | | | | | | | PDIP-32 |
| STC62WV1024JI | | | | | | | | SOJ-32 |
| STC62WV1024DI | | | | | | | | DICE |

■ PIN CONFIGURATIONS**■ BLOCK DIAGRAM**

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■ PIN DESCRIPTIONS

| Name | Function |
|--|---|
| A0-A16 Address Input | These 17 address inputs select one of the 131,072 x 8-bit words in the RAM |
| $\overline{CE1}$ Chip Enable 1 Input $\overline{CE2}$ Chip Enable 2 Input | $\overline{CE1}$ is active LOW and $\overline{CE2}$ is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected. |
| \overline{WE} Write Enable Input | The write enable input is active LOW and controls read and write operations. With the chip selected, when \overline{WE} is HIGH and \overline{OE} is LOW, output data will be present on the DQ pins; when \overline{WE} is LOW, the data present on the DQ pins will be written into the selected memory location. |
| \overline{OE} Output Enable Input | The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when \overline{OE} is inactive. |
| DQ0-DQ7 Data Input/Output Ports | These 8 bi-directional ports are used to read data from or write data into the RAM. |
| Vcc | Power Supply |
| Gnd | Ground |

■ TRUTH TABLE

| MODE | \overline{WE} | $\overline{CE1}$ | $\overline{CE2}$ | \overline{OE} | I/O OPERATION | Vcc CURRENT |
|------------------------------|-----------------|------------------|------------------|-----------------|---------------|-----------------------|
| Not selected (Power Down) | X | H | X | X | High Z | I_{CCSB}, I_{CCSB1} |
| | X | X | L | X | | |
| Output Disabled | H | L | H | H | High Z | I_{CC} |
| Read | H | L | H | L | DOUT | I_{CC} |
| Write | L | L | H | X | DIN | I_{CC} |

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| SYMBOL | PARAMETER | RATING | UNITS |
|--------|--------------------------------------|-----------------|-------|
| V TERM | Terminal Voltage with Respect to GND | -0.5 to Vcc+0.5 | V |
| T BIAS | Temperature Under Bias | -40 to +85 | °C |
| T STG | Storage Temperature | -60 to +150 | °C |
| P T | Power Dissipation | 1.0 | W |
| I OUT | DC Output Current | 20 | mA |

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

| RANGE | AMBIENT TEMPERATURE | Vcc |
|------------|---------------------|-------------|
| Commercial | 0 °C to +70 °C | 2.4V ~ 5.5V |
| Industrial | -40 °C to +85 °C | 2.4V ~ 5.5V |

■ CAPACITANCE ⁽¹⁾ (TA = 25°C, f = 1.0 MHz)

| SYMBOL | PARAMETER | CONDITIONS | MAX. | UNIT |
|--------|--------------------------|------------|------|------|
| CIN | Input Capacitance | VIN=0V | 6 | pF |
| CDQ | Input/Output Capacitance | VI/O=0V | 8 | pF |

1. This parameter is guaranteed and not 100% tested.

DC ELECTRICAL CHARACTERISTICS (TA = -40°C to +85°C)

| PARAMETER NAME | PARAMETER | TEST CONDITIONS | MIN. | TYP. ⁽¹⁾ | MAX. | UNITS | | |
|-----------------------------------|--|--|--|--|------|-----------------------|------------|----|
| V _{IL} | Guaranteed Input Low Voltage ⁽²⁾ | | V _{VCC} =3.0V V _{VCC} =5.0V | -0.5 | -- | 0.8 | V | |
| V _{IH} | Guaranteed Input High Voltage ⁽²⁾ | | V _{VCC} =3.0V V _{VCC} =5.0V | 2.0 2.2 | -- | V _{VCC} +0.3 | V | |
| I _{IL} | Input Leakage Current | V _{VCC} = Max, V _{IN} = 0V to V _{VCC} | -- | -- | 1 | μA | | |
| I _{LO} | Output Leakage Current | V _{VCC} = Max, $\overline{CE1} = V_{IH}$, CE2 = V _{IL} , or $\overline{OE} = V_{IH}$, V _{IO} = 0V to V _{VCC} | -- | -- | 1 | μA | | |
| V _{OL} | Output Low Voltage | V _{VCC} = Max, I _{OL} = 2.0mA | V _{VCC} =3.0V V _{VCC} =5.0V | -- | -- | 0.4 | V | |
| V _{OH} | Output High Voltage | V _{VCC} = Min, I _{OH} = -1.0mA | V _{VCC} =3.0V V _{VCC} =5.0V | 2.4 | -- | -- | V | |
| I _{CC} ⁽⁵⁾ | Operating Power Supply Current | $\overline{CE1} = V_{IL}$, or CE2 = V _{IH} , I _{DO} = 0mA, F = F _{max} ⁽³⁾ | 70ns | V _{VCC} =3.0V V _{VCC} =5.0V | -- | -- | 15 39 | mA |
| I _{CCSB} | Standby Current-TTL | $\overline{CE1} = V_{IH}$, or CE2 = V _{IL} , I _{DO} = 0mA | | V _{VCC} =3.0V V _{VCC} =5.0V | -- | -- | 0.5 1.0 | mA |
| I _{CCSB1} ⁽⁴⁾ | Standby Current-CMOS | $\overline{CE1} \geq V_{CC}-0.2V$ or CE2 $\leq 0.2V$, V _{IN} $\geq V_{CC}-0.2V$ or V _{IN} $\leq 0.2V$ | | V _{VCC} =3.0V V _{VCC} =5.0V | -- | -- | 0.1 20 | μA |

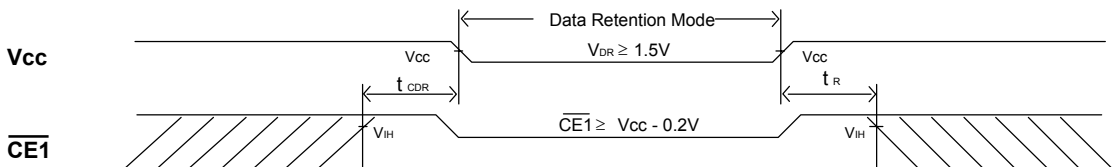
1. Typical characteristics are at TA = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. F_{max} = 1/t_{RC}.
4. I_{CCSB1_Max.} is 1.3uA/8.0uA at V_{VCC}=3.0V/5.0V and TA=70°C.
5. I_{CC_Max.} is 18mA(@3V)/47mA(@5V) under 55ns operation.

DATA RETENTION CHARACTERISTICS (TA = -40°C to +85°C)

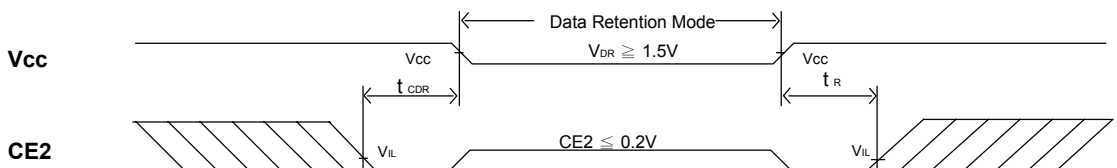
| SYMBOL | PARAMETER | TEST CONDITIONS | MIN. | TYP. ⁽¹⁾ | MAX. | UNITS |
|----------------------------------|--------------------------------------|--|--------------------------------|---------------------|------|-------|
| V _{DR} | V _{VCC} for Data Retention | $\overline{CE1} \geq V_{CC} - 0.2V$ or CE2 $\leq 0.2V$, V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$ | 1.5 | -- | -- | V |
| I _{CCDR} ⁽³⁾ | Data Retention Current | $\overline{CE1} \geq V_{CC} - 0.2V$ or CE2 $\leq 0.2V$, V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$ | -- | 0.05 | 0.3 | μA |
| t _{CDR} | Chip Deselect to Data Retention Time | See Retention Waveform | 0 | -- | -- | ns |
| t _R | Operation Recovery Time | | T _{RC} ⁽²⁾ | -- | -- | ns |

1. V_{VCC} = 1.5V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. I_{CCDR_MAX.} is 0.2uA at TA=70°C.

LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)








■ AC TEST CONDITIONS

(Test Load and Input/Output Reference)

| | |
|---|---|
| Input Pulse Levels | Vcc / 0V |
| Input Rise and Fall Times | 1V/ns |
| Input and Output Timing Reference Level | 0.5Vcc |
| Output Load | C _L = 30pF+1TTL C _L = 100pF+1TTL |

■ KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|----------------------------------|---|
|  | MUST BE STEADY | MUST BE STEADY |
|  | MAY CHANGE FROM H TO L | WILL BE CHANGE FROM H TO L |
|  | MAY CHANGE FROM L TO H | WILL BE CHANGE FROM L TO H |
|  | DON'T CARE: ANY CHANGE PERMITTED | CHANGE : STATE UNKNOWN |
|  | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

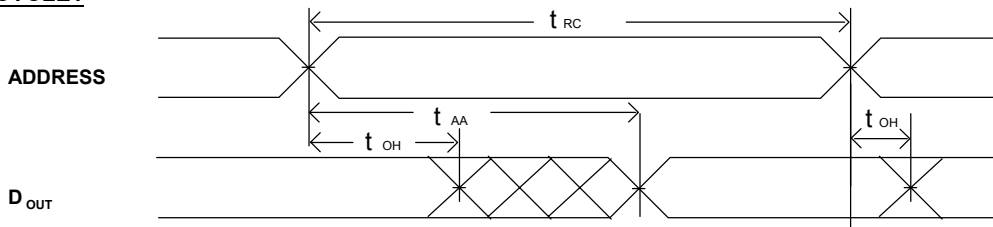
■ AC ELECTRICAL CHARACTERISTICS (TA = -40°C to + 85°C)

READ CYCLE

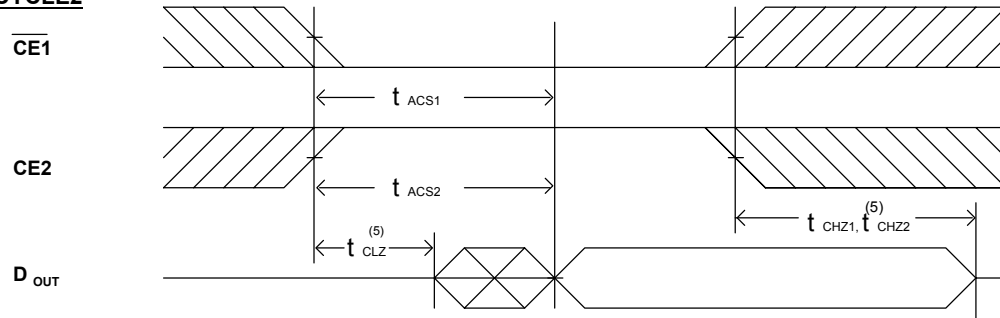
| JEDEC PARAMETER NAME | PARAMETER NAME | DESCRIPTION | CYCLE TIME : 55ns (Vcc = 3.0~5.5V) | | | CYCLE TIME : 70ns (Vcc = 2.7~5.5V) | | | UNIT |
|----------------------|-------------------|---|---------------------------------------|------|------|---------------------------------------|------|------|------|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| t _{AVAX} | t _{RC} | Read Cycle Time | 55 | -- | -- | 70 | -- | -- | ns |
| t _{AVQV} | t _{AA} | Address Access Time | -- | -- | 55 | -- | -- | 70 | ns |
| t _{E1LQV} | t _{ACS1} | Chip Select Access Time (CE1) | -- | -- | 55 | -- | -- | 70 | ns |
| t _{E2HOV} | t _{ACS2} | Chip Select Access Time (CE2) | -- | -- | 55 | -- | -- | 70 | ns |
| t _{GLQV} | t _{OE} | Output Enable to Output Valid | -- | -- | 30 | -- | -- | 40 | ns |
| t _{E1LQX} | t _{CLZ1} | Chip Select to Output Low Z (CE1) | 10 | -- | -- | 10 | -- | -- | ns |
| t _{E2HOX} | t _{CLZ2} | Chip Select to Output Low Z (CE2) | 10 | -- | -- | 10 | -- | -- | ns |
| t _{GLQX} | t _{OLZ} | Output Enable to Output in Low Z | 10 | -- | -- | 10 | -- | -- | ns |
| t _{E1HQZ} | t _{CHZ1} | Chip Deselect to Output in High Z (CE1) | -- | -- | 35 | -- | -- | 40 | ns |
| t _{E2HQZ} | t _{CHZ2} | Chip Deselect to Output in High Z (CE2) | -- | -- | 35 | -- | -- | 40 | ns |
| t _{GHQZ} | t _{OHZ} | Output Disable to Output in High Z | -- | -- | 30 | -- | -- | 35 | ns |
| t _{AXOX} | t _{OH} | Data Hold from Address Change | 10 | -- | -- | 10 | -- | -- | ns |

SWITCHING WAVEFORMS (READ CYCLE)

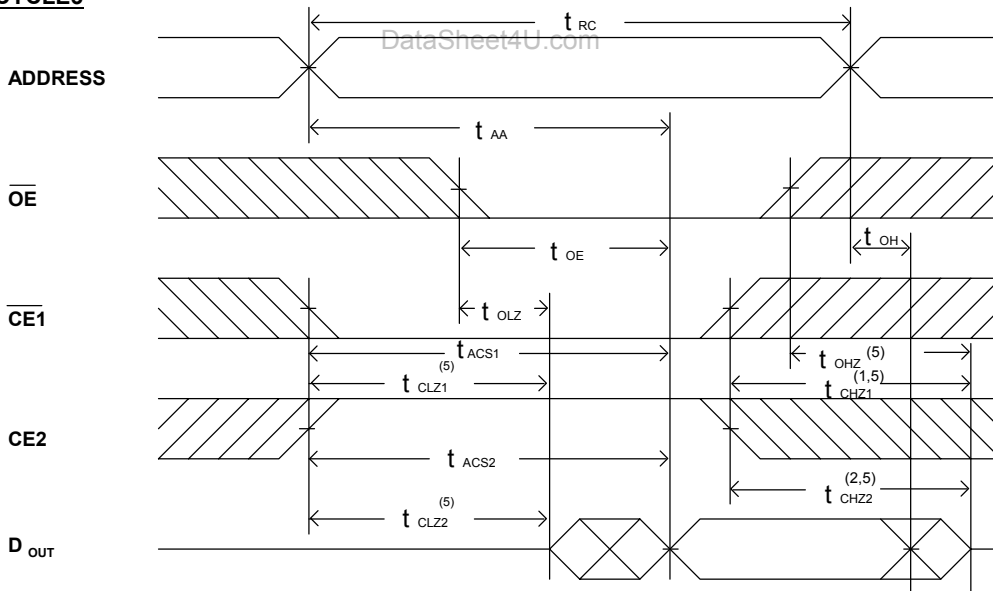
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:

1. WE is high in read Cycle.
2. Device is continuously selected when $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and/or CE2 transition high.
4. $\overline{OE} = V_{IL}$.
5. The parameter is guaranteed but not 100% tested.

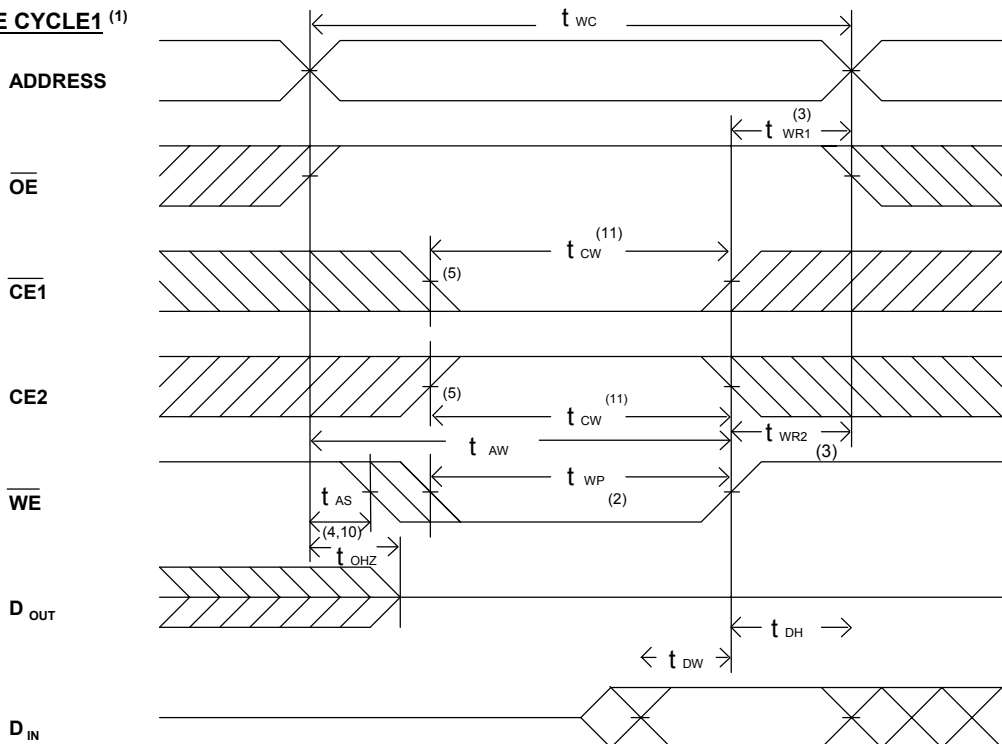
■ AC ELECTRICAL CHARACTERISTICS (TA = -40°C to + 85°C)

WRITE CYCLE

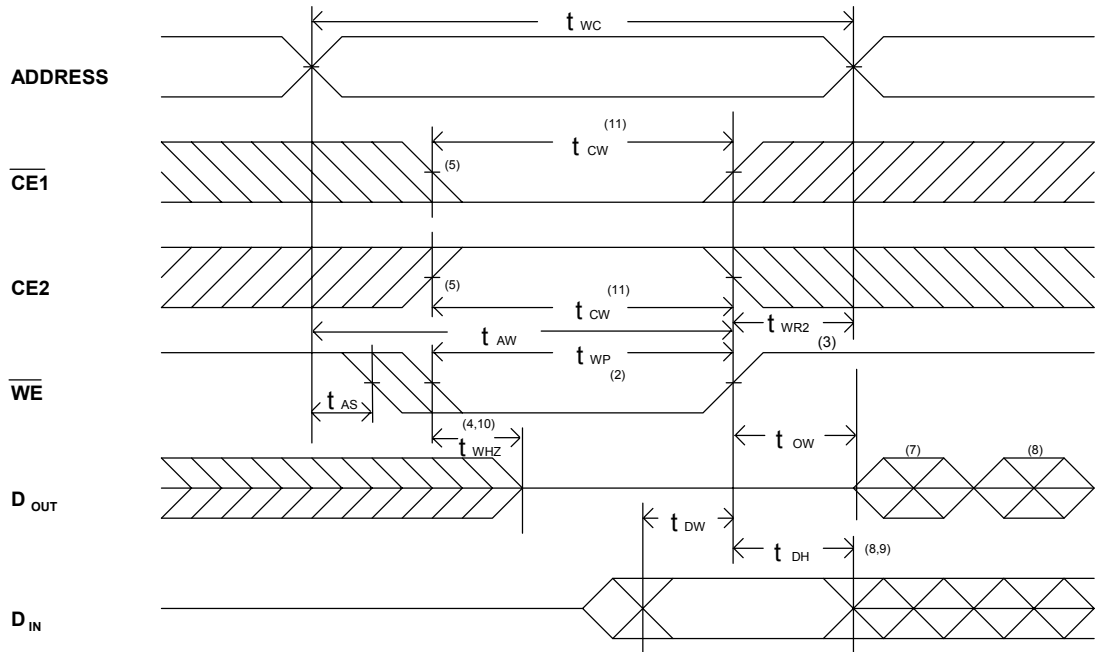
| JEDEC PARAMETER NAME | PARAMETER NAME | DESCRIPTION | CYCLE TIME : 55ns (Vcc = 3.0~5.5V) | | | CYCLE TIME : 70ns (Vcc = 2.7~5.5V) | | | UNIT |
|----------------------------|-------------------|---|---------------------------------------|------|------|---------------------------------------|------|------|------|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| t _{AVAX} | t _{wc} | Write Cycle Time | 55 | -- | -- | 70 | -- | -- | ns |
| t _{E1LWH} | t _{cw} | Chip Select to End of Write | 55 | -- | -- | 70 | -- | -- | ns |
| t _{AVWL} | t _{AS} | Address Set up Time | 0 | -- | -- | 0 | -- | -- | ns |
| t _{AVWH} | t _{AW} | Address Valid to End of Write | 55 | -- | -- | 70 | -- | -- | ns |
| t _{WLWH} | t _{WP} | Write Pulse Width | 35 | -- | -- | 50 | -- | -- | ns |
| t _{WHAX} | t _{WR1} | Write Recovery Time ($\overline{CE1}$, \overline{WE}) | 0 | -- | -- | 0 | -- | -- | ns |
| t _{E2LAX} | t _{WR2} | Write Recovery Time (CE2) | 0 | -- | -- | 0 | -- | -- | ns |
| t _{WLOZ} | t _{WHZ} | Write to Output in High Z | -- | -- | 25 | -- | -- | 30 | ns |
| t _{DVWH} | t _{DW} | Data to Write Time Overlap | 25 | -- | -- | 30 | -- | -- | ns |
| t _{WHDX} | t _{DH} | Data Hold from Write Time | 0 | -- | -- | 0 | -- | -- | ns |
| t _{GHOZ} | t _{OHZ} | Output Disable to Output in High Z | -- | -- | 25 | -- | -- | 30 | ns |
| t _{WHQX} | t _{OW} | End of Write to Output Active | 5 | -- | -- | 5 | -- | -- | ns |

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1⁽¹⁾



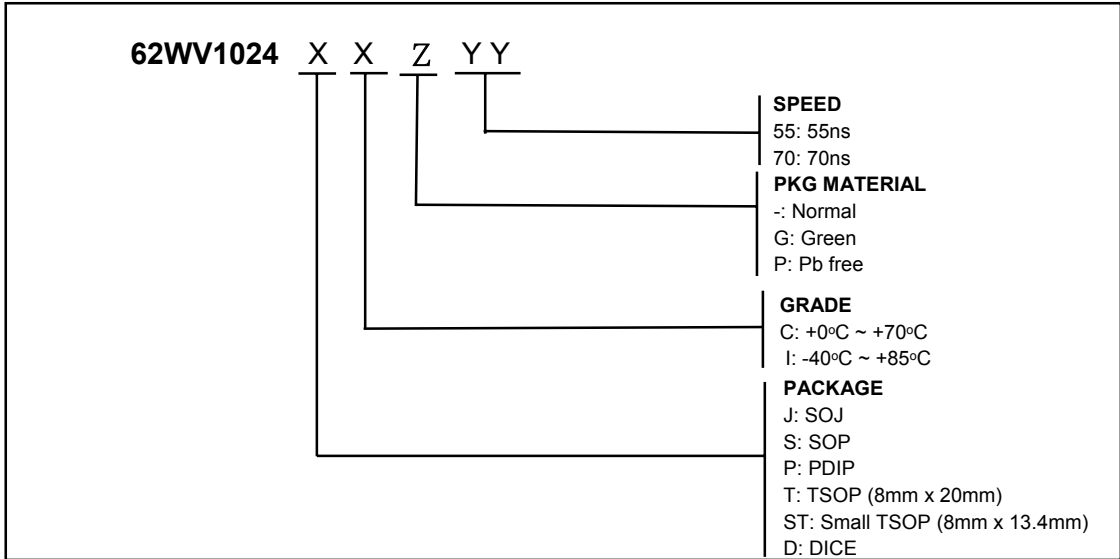
WRITE CYCLE2 (1,6)



NOTES:

1. \overline{WE} must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE1}$ and $CE2$ active and \overline{WE} low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE1}$ or \overline{WE} going high or $CE2$ going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE1}$ low transition or the $CE2$ high transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.
6. \overline{OE} is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE1}$ is low and $CE2$ is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $\overline{CE1}$ going low or $CE2$ going high to the end of write.

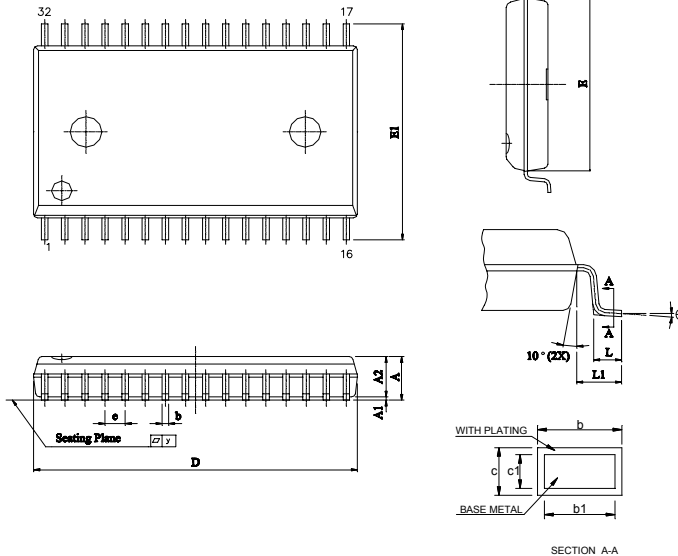
ORDERING INFORMATION



Note:

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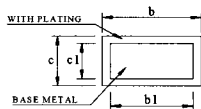
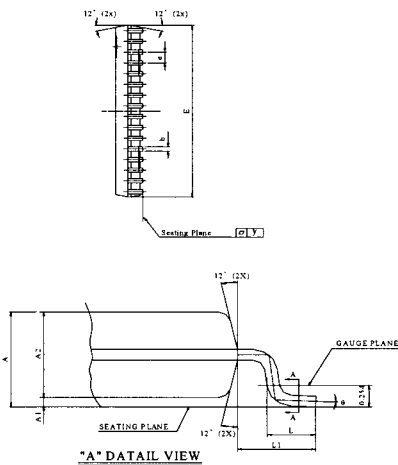
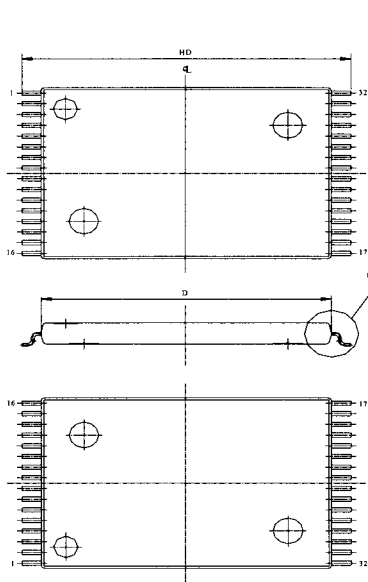
PACKAGE DIMENSIONS



| SYMBOL | UNIT | INCH | MM |
|--------|------|---------------|--------------|
| A | | 0.111±0.007 | 2.821±0.176 |
| A1 | | 0.009±0.005 | 0.229±0.127 |
| A2 | | 0.1055±0.0055 | 2.680±0.140 |
| b | | 0.014 ~ 0.020 | 0.35 ~ 0.50 |
| b1 | | 0.014 ~ 0.018 | 0.35 ~ 0.46 |
| c | | 0.006 ~ 0.012 | 0.15 ~ 0.32 |
| c1 | | 0.006 ~ 0.011 | 0.15 ~ 0.28 |
| D | | 0.805±0.005 | 20.447±0.127 |
| E | | 0.445±0.005 | 11.303±0.127 |
| E1 | | 0.555±0.012 | 14.097±0.305 |
| e | | 0.050±0.006 | 1.270±0.152 |
| L | | 0.033±0.010 | 0.834±0.25 |
| L1 | | 0.055±0.008 | 1.397±0.203 |
| y | | 0.004 Max. | 0.1 Max. |
| θ | | 0° ~ 10° | 0° ~ 10° |

SOP -32

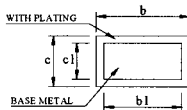
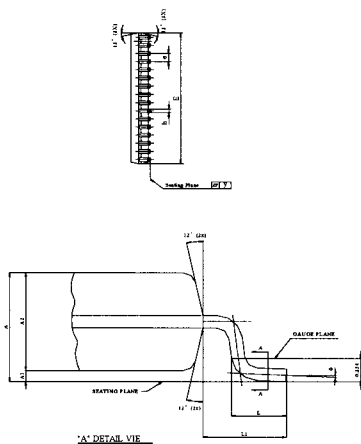
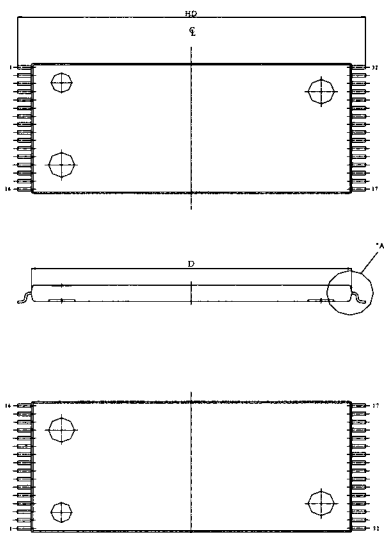
■ PACKAGE DIMENSIONS (continued)



SECTION A-A

| UNIT | INCH | MM |
|------|--|--|
| A | 0.0433± 0.004 | 1.10± 0.10 |
| A1 | 0.004± 0.002 | 0.10± 0.05 |
| A2 | 0.039± 0.002 | 1.00± 0.05 |
| b | 0.009± 0.002 | 0.22± 0.05 |
| b1 | 0.008± 0.001 | 0.20± 0.03 |
| c | 0.004 ~ 0.008 | 0.10 ~ 0.21 |
| c1 | 0.004 ~ 0.006 | 0.10 ~ 0.16 |
| D | 0.465± 0.004 | 11.80± 0.10 |
| E | 0.315± 0.004 | 8.00± 0.10 |
| e | 0.020± 0.004 | 0.50± 0.10 |
| HD | 0.528± 0.008 | 13.40± 0.20 |
| L | 0.0197 ^{+0.008} / _{-0.004} | 0.50 ^{+0.2} / _{-0.1} |
| L1 | 0.0315± 0.004 | 0.80± 0.10 |
| y | 0.004 Max. | 0.1 Max. |
| θ | 0° ~ 8° | 0° ~ 8° |

STSOP - 32

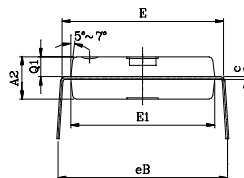
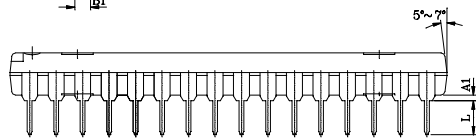
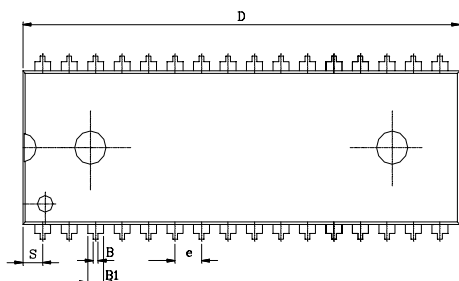


SECTION A-A

| UNIT | INCH | MM |
|------|--|--|
| A | 0.0433± 0.004 | 1.10± 0.10 |
| A1 | 0.004± 0.002 | 0.10± 0.05 |
| A2 | 0.039± 0.002 | 1.00± 0.05 |
| b | 0.009± 0.002 | 0.22± 0.05 |
| b1 | 0.008± 0.001 | 0.20± 0.03 |
| c | 0.004 ~ 0.008 | 0.10 ~ 0.21 |
| c1 | 0.004 ~ 0.006 | 0.10 ~ 0.16 |
| D | 0.724± 0.004 | 18.40± 0.10 |
| E | 0.315± 0.004 | 8.00± 0.10 |
| e | 0.020± 0.004 | 0.50± 0.10 |
| HD | 0.787± 0.008 | 20.00± 0.20 |
| L | 0.0197 ^{+0.008} / _{-0.004} | 0.50 ^{+0.2} / _{-0.1} |
| L1 | 0.0315± 0.004 | 0.80± 0.10 |
| y | 0.004 Max. | 0.1 Max. |
| θ | 0° ~ 8° | 0° ~ 8° |

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■ PACKAGE DIMENSIONS (continued)

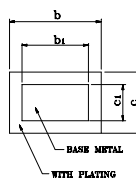
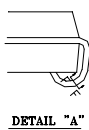
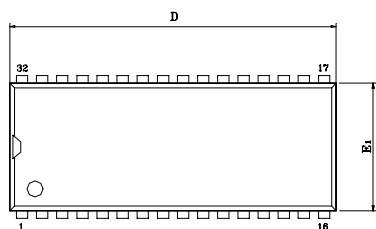


| UNIT STEP | INCH(BASE) | MM(REF) |
|--------------|-------------|--------------|
| A1 | 0.010(MIN) | 0.254(MIN) |
| A2 | 0.154±0.005 | 3.912±0.127 |
| B | 0.018±0.005 | 0.457±0.127 |
| B1 | 0.050±0.005 | 1.270±0.127 |
| c | 0.010±0.004 | 0.254±0.102 |
| D | 1.650±0.005 | 41.910±0.127 |
| E | 0.600±0.010 | 15.240±0.254 |
| E1 | 0.544±0.004 | 13.818±0.102 |
| e | 0.100(TYP) | 2.540(TYP) |
| eB | 0.650±0.020 | 16.510±0.508 |
| L | 0.130±0.010 | 3.302±0.254 |
| S | 0.075±0.010 | 1.905±0.254 |
| Q1 | 0.070±0.005 | 1.778±0.127 |

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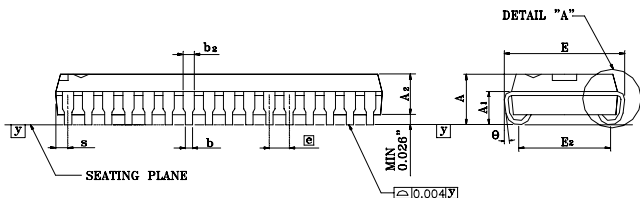


SECTION F-F

| Symbol | Dimension in inch | | | Dimension in mm | | |
|----------------|-------------------|-------|-------|-----------------|-------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.128 | 0.132 | 0.140 | 3.25 | 3.35 | 3.56 |
| A ₁ | 0.082 | — | — | 2.08 | — | — |
| A ₂ | 0.095 | 0.100 | 0.105 | 2.41 | 2.54 | 2.67 |
| b | 0.016 | 0.018 | 0.020 | 0.41 | 0.46 | 0.51 |
| b ₂ | 0.026 | 0.028 | 0.032 | 0.66 | 0.71 | 0.81 |
| c | 0.006 | 0.006 | 0.012 | 0.15 | 0.20 | 0.30 |
| D | 0.820 | 0.825 | 0.830 | 20.83 | 20.96 | 21.08 |
| E | 0.330 | 0.335 | 0.340 | 8.39 | 8.51 | 8.63 |
| E ₁ | 0.295 | 0.300 | 0.305 | 7.49 | 7.62 | 7.75 |
| E ₂ | 0.260 | 0.267 | 0.274 | 6.61 | 6.78 | 6.96 |
| θ | — | 0.050 | — | — | 1.27 | — |
| s | — | — | 0.048 | — | — | 1.22 |
| y | — | — | 0.004 | — | — | 0.10 |
| θ | -5° | 2° | 6° | -5° | 2° | 6° |

Note:

- DIMENSION D DOES NOT INCLUDE MOLD FLASH, LEAD BURRS, AND GATE BURRS, BUT MOLD MISMATCH IS INCLUDED. MOLD FLASH, LEAD BURRS, AND GATE BURRS SHALL NOT EXCEED .006" PER END. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .010" PER SIDE.
- DIMENSIONS D AND E₁ ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, LEAD BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION S INCLUDES MOLD PROTRUSION, MISMATCH AND SUPPORTING BAR BURRS.
- DIMENSION b₂ DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE b₂ DIMENSION TO BE GREATER THAN .037". THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE b₂ DIMENSION TO BE SMALLER THAN .025".



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