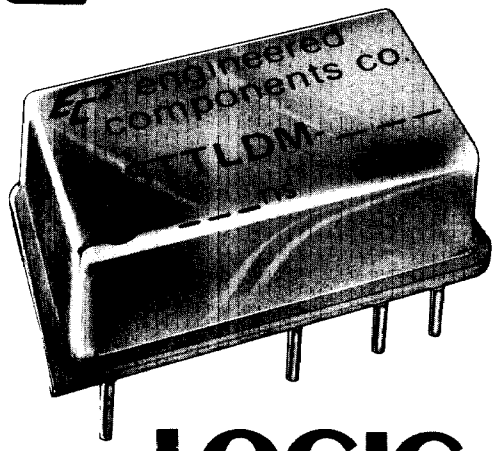
EC²



low profile

T²L COMPATIBLE

LOGIC DELAY MODULE

- T²L input and outputs
- Delays stable and precise
- 14-pin DIP package (.280 high)
- Available in delays from 25 to 1000ns
- 20% taps — each isolated and with 10 T²L fan-out capacity
- Fast rise time on all outputs

design notes

These hermetically sealed "DIP Series" Logic Delay Modules developed by Engineered Components Company have been designed to provide precise tapped delays with required driving and pick-off circuitry contained in a single 14-pin DIP package compatible with Schottky T²L and DTL circuits. These logic delay modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 3 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The HSTTLDM is offered in 24 delays from 25ns to 1000ns with each module incorporating taps at 20% increments of total delay. Delay tolerances are maintained as shown in the accompanying part number table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 4ns maximum when measured from 0.75V to 2.4V. Temperature coefficient of delay is approximately +500 ppm/°C over the operating temperature range of 0 to +70°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the selected output tap without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module has the capability of driving up to 20 T²L loads with a maximum of 10 loads on any one tap.

These "DIP Series" modules are packaged in a 14-pin DIP hermetically sealed, metal enclosure with glass-to-metal seal terminating pins. The pins meet the solderability requirements of MIL-STD-202, Method 208. Glass standoffs are provided on the header to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

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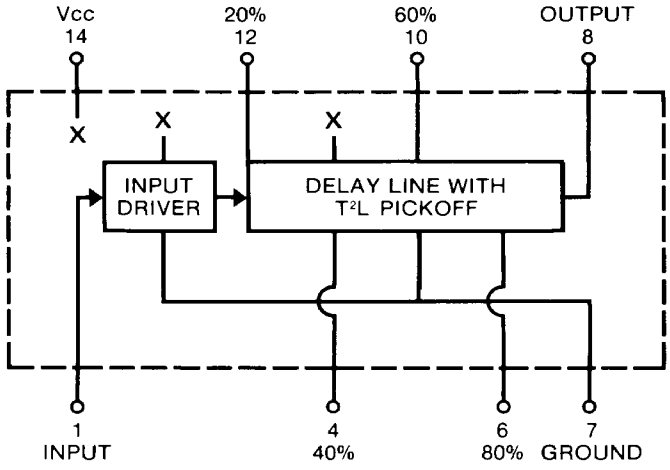
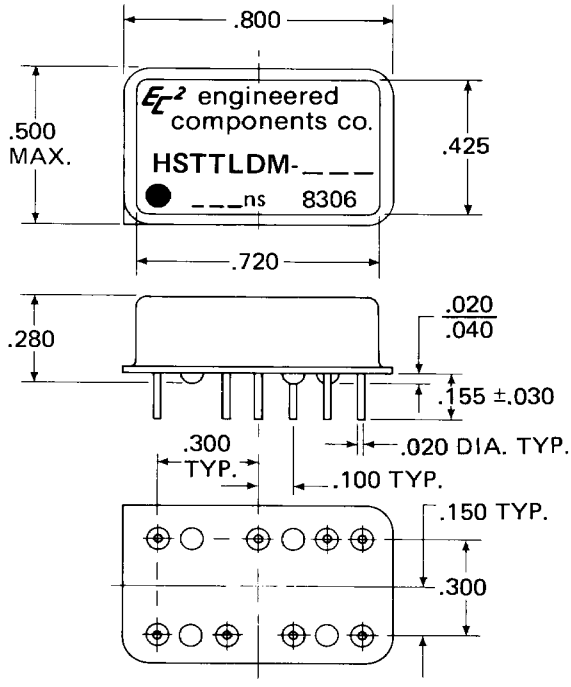
DESIGN NOTES (continued)

Marking consists of manufacturer's name, logo (EC^2), part number and date code of manufacture. All marking is applied by an electro-etching process in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. V_{CC} supply voltage is maintained at 5.0V DC.
3. All units are tested using a Schottky toggle-type positive input pulse and one Schottky T^2L load at the output being tested.
4. ϕ Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

* V_{CC} supply voltage: . . . . . 4.75 to 5.25V DC

V_{CC} supply current:

- Constant "0" in . . . . . 60ma typical
- Constant "1" in . . . . . 20ma typical

Logic 1 input:

- Voltage . . . . . 2V min.; 5.5V max.
- Current . . . . . 2.4V = 50ua max.
  5.5V = 1ma max.

Logic 0 input:

- Voltage . . . . . .8V max.
- Current . . . . . −2ma max.

Logic 1 Voltage out: . . . . . 2.4V min.

Logic 0 Voltage out: . . . . . .4V max.

Operating temperature range: . . . . . 0 to 70°C.

Storage temperature: . . . . . −55 to +125°C.

* Delays increase or decrease approximately 2% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)					
PART NO.	Tap 1	Tap 2	Tap 3	Tap 4	OUTPUT
HSTTLDM-25	5 ±1	10 ±1	15 ±1	20 ±1	25 ±1
HSTTLDM-30	6 ±1	12 ±1	18 ±1	24 ±1	30 ±1
HSTTLDM-35	7 ±1	14 ±1	21 ±1	28 ±1.5	35 ±1.5
HSTTLDM-40	8 ±1	16 ±1	24 ±1.5	32 ±1.5	40 ±1.5
HSTTLDM-45	9 ±1	18 ±1	27 ±1.5	36 ±1.5	45 ±2
HSTTLDM-50	10 ±1	20 ±1	30 ±1.5	40 ±2	50 ±2
HSTTLDM-75	15 ±1	30 ±1.5	45 ±2	60 ±2.5	75 ±2.5
HSTTLDM-100	20 ±1	40 ±1.5	60 ±2	80 ±3	100 ±3
HSTTLDM-125	25 ±1	50 ±2	75 ±2.5	100 ±3	125 ±4
HSTTLDM-150	30 ±1.5	60 ±2	90 ±3	120 ±4	150 ±5
HSTTLDM-175	35 ±1.5	70 ±2.5	105 ±4	140 ±5	175 ±5
HSTTLDM-200	40 ±1.5	80 ±2.5	120 ±4	160 ±5	200 ±6
HSTTLDM-225	45 ±2	90 ±3	135 ±4	180 ±6	225 ±7
HSTTLDM-250	50 ±2	100 ±3	150 ±4.5	200 ±6	250 ±8
HSTTLDM-300	60 ±2	120 ±4	180 ±5	240 ±7	300 ±9
HSTTLDM-350	70 ±2	140 ±4.5	210 ±7	280 ±9	350 ±11
HSTTLDM-400	80 ±3	160 ±5	240 ±7	320 ±10	400 ±12
HSTTLDM-450	90 ±3	180 ±6	270 ±8	360 ±11	450 ±14
HSTTLDM-500	100 ±3	200 ±6	300 ±9	400 ±12	500 ±15
HSTTLDM-600	120 ±4	240 ±7	360 ±11	480 ±15	600 ±18
HSTTLDM-700	140 ±4	280 ±9	420 ±13	560 ±17	700 ±20
HSTTLDM-800	160 ±5	320 ±10	480 ±15	640 ±19	800 ±20
HSTTLDM-900	180 ±6	360 ±11	520 ±16	720 ±20	900 ±22
HSTTLDM-1000	200 ±6	400 ±12	600 ±18	800 ±20	1000 ±22

ϕ All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.

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