HARRIS SEMICONDUCTOR

HIP0050

0.3A/50V Octal Low Side Power Driver with Serial Bus Control and Over-Current Fault Flag

December 1996

Features

- **Octal NDMOS Output Drivers in a High Voltage Power BiMOS Process**
  - **Each Capable of Sinking 300mA**
  - **Low Idle and Standby Current**
- **Over-Stress Protection - Each Output:**
  - **Over-Current Latch Off . . . . . 300mA Min**
  - **Over-Voltage Clamp . . . . . 50V Typ**
- **Thermal Shutdown with Hysteresis**
- **Serial Data Input, Parallel Output Power Drive**
- **Short Circuit Latch Off for Each Output**
- **Common Enable for Output Drivers and Data Storage Register**
- **Ambient Operating Temperature Range. . . . . .-40^{o}C to 85^{o}C**
  - **Optional 125^{o}C Maximum Ambient Operating Temperature Range (Dissipation Limited)**

Applications

- **Automotive and Industrial Systems**
- **Solenoids, Relays and Lamp Drivers**
- **Logic and µP Controlled Drivers**
- **Robotic Controls**

Description

The HIP0050 is a logic controlled, eight channel Octal Low Side Power Driver. As shown in the block diagram, the outputs are controlled via the serial data interface which allows the data to be shifted out, allowing control of other cascaded serial devices. If an Over-Current (OC) short circuit exists in one output, it may be independently shutdown while the other outputs remain in operation. When a shorted output is latched off, it may be turned back on when the next serial input data is latched. A fault flag ($\overline{FLT}$) is set to a low status to indicate current-limited shutdown. The outputs are independently latched off when an OC fault is detected. The fault latch is cleared on the next data strobe. Over-Temperature (OT) shutdown is provided with hysteresis to force global shutdown of all output drivers. Shutdown is maintained until the on-chip temperature falls below the minimum hysteresis threshold point.

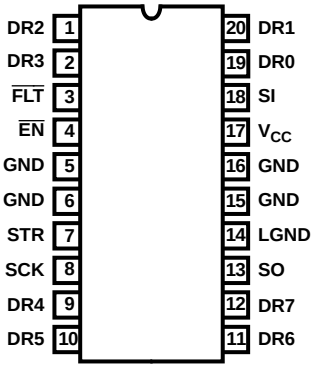
The HIP0050 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving lamps, displays, relays, and solenoids in applications where low operating power, high breakdown voltage, and high output current at high temperature is required. Higher current needs can be met by paralleling adjacent output drivers.

Ordering Information

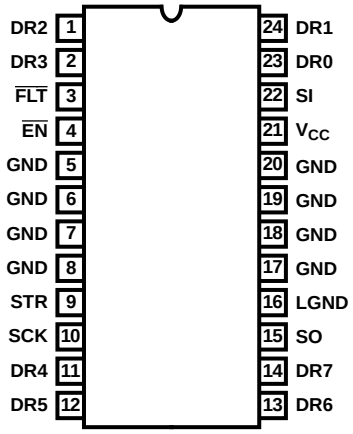
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HIP050IP	-40 to 85	20 Ld PDIP	E20.3
HIP0050IB	-40 to 85	24 Ld SOIC	M24.3

Pinouts

HIP0050 (PDIP)
TOP VIEW



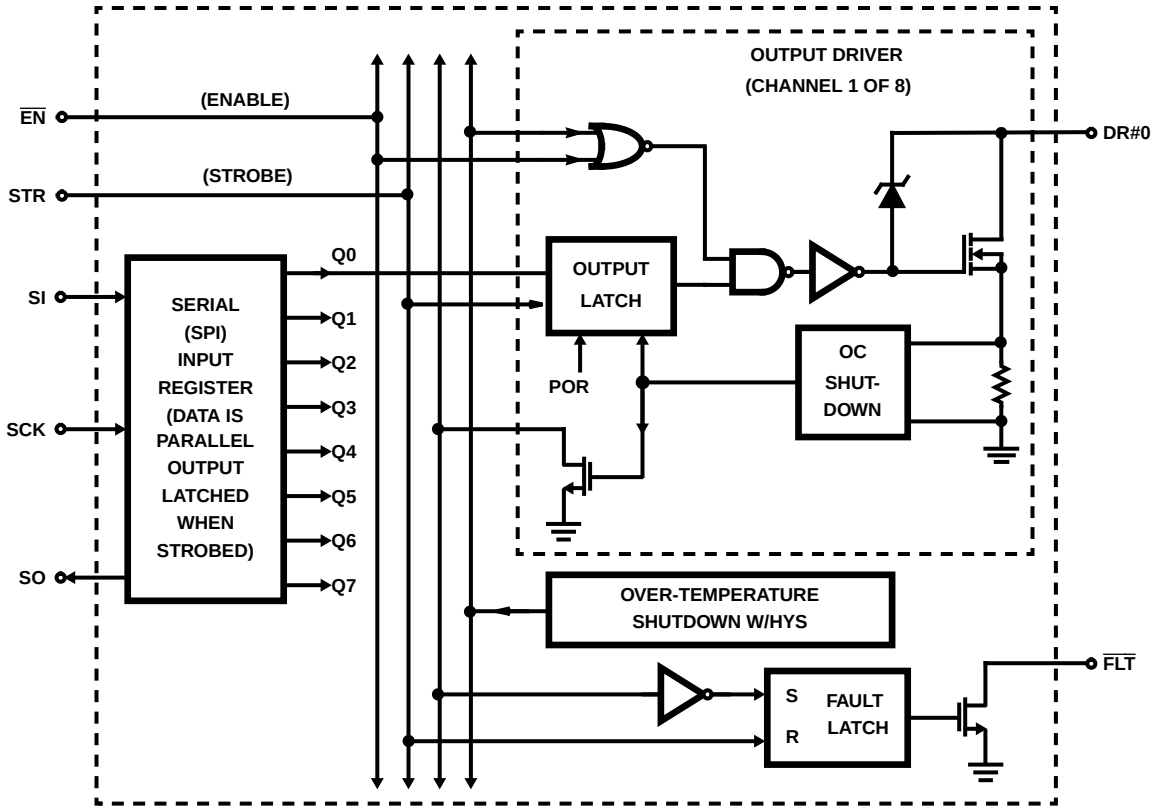
HIP0050 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4034.1**

Block Diagram



Output Control Logic Table

STROBE	8-BIT SERIAL DATA (LATCHED)								OUTPUT							
⎍	D1	D2	D3	D4	D5	D6	D7	D8	DR1	DR2	DR3	DR4	DR5	DR6	DR7	DR8
⎍	0	0	0	0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
⎍	1	0	0	0	0	0	0	0	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
⎍	1	1	0	0	0	0	0	0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
⎍	1	1	1	0	0	0	0	0	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
⎍	1	1	1	1	0	0	0	0	ON	ON	ON	ON	OFF	OFF	OFF	OFF
⎍	0	0	0	0	1	1	1	1	OFF	OFF	OFF	OFF	ON	ON	ON	ON
⎍	1	1	1	1	1	1	1	1	ON	ON	ON	ON	ON	ON	ON	ON

Absolute Maximum Ratings

Output Voltage, V_{OUT} (Note 1) . . . . . -0.3V to V_{OC}
Input Voltage, V_{IN} . . . . . -0.3V to V_{CC} +0.3V
Logic Supply Voltage, V_{CC} . . . . . -0.3V to +7V
Max Output Load Current, I_{LOAD} (Per Output, Note 2) . . . . . I_{CL}
Max. Output Load Current, I_{LOAD} (All Outputs ON, Note 2) 2A
Operating Ambient Temperature Range, T_A . . . . . -40^oC to 85^oC
Operating Junction Temperature Range. . . . . -40^oC to 150^oC
Storage Temperature Range, T_{STG} . . . . . -55^oC to 150^oC
Maximum Lead Temperature (Soldering 10s Max). . . . . 300^oC
(Lead Tips Only)

Thermal Information

Package	θ_{JC} ($^oC/W$)†	θ_{JA} ($^oC/W$)††	
		0	2
PDIP	10	50	35
SOIC	10	60	40

† Versus Additional Square Inches 1oz. copper on PCB.
†† Standard Test Board, 0.002 diameter T/C located at lead shoulder, middle lead.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Typical Logic Supply Voltage, V_{CC} . . . . . +5V
I_{CC} Supply Current, with 200mA each Output 2mA
I_{CC} Supply Current, with No Load 2mA
Input Low Voltage 1.0V
Input High Voltage 3.5V
Power Output Driver Voltage Range . . . . . 0 to V_{OC}
Power Output Driver Current Load, I_{DR} . . . . . 0 to I_{CL}
Typical Output r_{DSON} Channel Resistance 2Ω
Typical Output Rise Time 4µs
Typical Output Fall Time 10µs

Electrical Specifications

V_{CC} = 4.5V to 5.5V, V_{BATT} = 8V to 16V, T_A = -40^oC to 85^oC; Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS DRIVERS (DR0 TO DR7)						
Output Channel Resistance	r_{DSON}	Output Current = 200mA, T_A = 85^oC	-	2	4.0	Ω
Output Over-Current Shutdown Threshold	I_{CL}		300	-	500	mA
Output Clamping Voltage	V_{OC}	Outputs OFF	42	50	58	V
Output Clamping Energy	E_{OC}	1ms Single Pulse Width, T_A = 25^oC, (Refer to Figure 2 for SOA).	-	25	-	mJ
Output OFF Leakage Current	I_{OFF}	Output Voltage = 40V, T_A = 85^oC	-	-	10	µA
Output Rise Time	t_{RISE}	Load = 75Ω, 0.01µF (Parallel)	0.5	4	30	µs
Output Fall Time	t_{FALL}	Load = 75Ω, 0.01µF (Parallel)	0.5	10	30	µs
Output Delay from Strobe, High to Low Output Transition	t_{DHL}		1	4	10	µs
Output Delay from Strobe, Low to High Output Transition	t_{DLH}		0.2	2.6	10	µs
LOGIC SUPPLY						
Logic Supply Current, Loaded	I_{CC}	All Outputs ON, 0.2A Load Per Output	-	2	4	mA
Logic Supply Current, No Load	I_{CC}	All Outputs OFF	-	2	4	mA
Logic Supply Under-Voltage Reset Threshold		All Outputs OFF	3.5	-	4	V
LOGIC INPUTS ($\overline{EN}$, SI, SCK, STR)						
Threshold Voltage at Falling Edge	V_T-	V_{CC} = 5V ±10%	$0.2V_{CC}$	$0.3V_{CC}$	-	V
Threshold Voltage at Rising Edge	V_T+	V_{CC} = 5V ±10%	-	$0.6V_{CC}$	$0.7V_{CC}$	V
Hysteresis Voltage	V_H	V_T+ - V_T-	0.85	1.4	2.25	V
Leakage Current	I_{LIN}		-10	-	10	µA
SERIAL DATA CLOCK (SCK) (Refer to Figure 1 for Waveform Detail)						
Frequency	f_{SCK}		-	-	1.6	MHz
Pulse Width High	$t_{W(SCKH)}$		-	27	175	ns

Electrical Specifications V_{CC} = 4.5V to 5.5V, V_{BATT} = 8V to 16V, T_A = -40°C to 85°C; Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Width Low	$t_{W(SCKL)}$		-	27	175	ns
SERIAL DATA IN (SI) (Refer to Figure 1 for Waveform Detail)						
Input Setup Time	t_{SUI}		-	1.1	75	ns
Input Hold Time	T_{HI}		-	1.5	75	ns
STROBE (STR)						
Strobe Pulse Width	$t_{W(S)}$		-	12	150	ns
Clock to Strobe Delay	$t_{D(CS)}$		-	5	75	ns
SERIAL DATA OUT (SO) (Refer to Figure 1 for Waveform Detail)						
Low Level Output Voltage	V_{OL}	Sink Current = 1.6mA	-	0.2	0.4	V
High Level Output Voltage	V_{OH}	Source Current = -1.6mA	3.7	4.4	-	V
Propagation Delay	$t_{P(CD)}$		75	260	500	ns
PROTECTION PARAMETERS						
Fault Output ($\overline{FLT}$) Low	V_{OL}	Sink Current = 1.6mA	-	-	0.4	V
Over-Temp. (OT) Shutdown	T_{SD}		145	155	165	°C
OT Shutdown Hysteresis	T_H		5	10	20	°C

NOTES:

1. The MOSFET Output Drain is internally clamped with a Drain-to-Gate Zener Diode that turns on the MOSFET; holding the drain at the output clamp voltage V_{OC}.
2. The HIP0050 Output Drive is protected by an internal current shutdown. The I_{CL} over-current shutdown threshold parameter specification defines the maximum current. The minimum limit for this threshold is 300mA. The maximum current with all outputs ON may be further limited by dissipation.
3. Package dissipation is based on thermal resistance capability in a normal operating environment. The junction to ambient thermal resistance values are defined here as a PC Board mounted device with minimal copper. Due to the heat conducting capability of the DIP and SOIC package lead frames, 35°C/W thermal resistance can be achieved with approximately 2 square inches of 1 oz. copper PC Board area. The junction to lead thermal resistance values are based on measurements from the chip to the ground leads of the package.

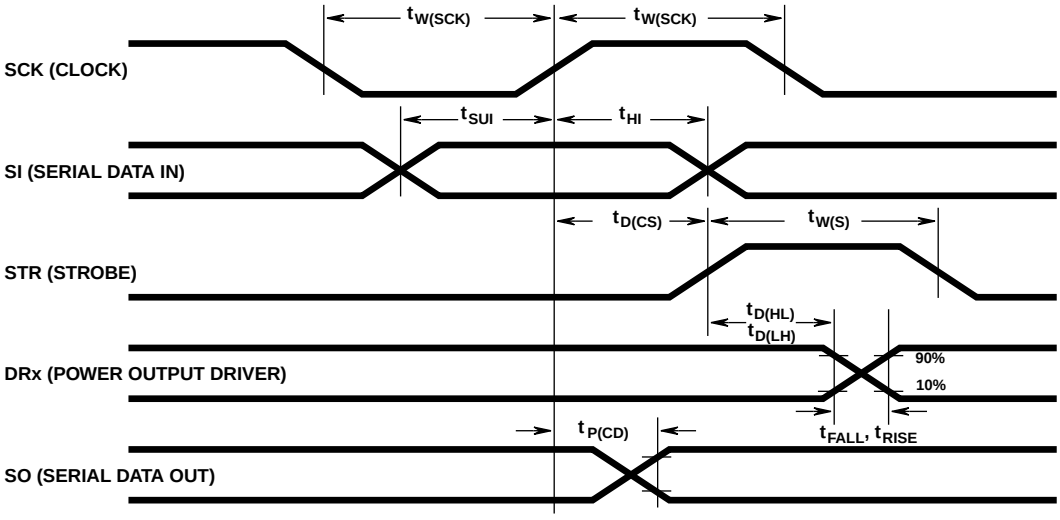


FIGURE 1. LOGIC TIMING CONTROL WAVEFORMS

Pin Descriptions

V_{CC} Power Pin

The V_{CC} pin is the positive 5V logic voltage supply input for the IC. The normal operating voltage range is 4.5V to 5.5V. When switched on, the POR forces all outputs off.

SCK Serial Clock Pin

SCK is the clock input for the SPI Interface. Output ON/OFF control data is clocked into an eight stage shift register on the rising edge of an external clock. This input has a Schmitt trigger.

SI Serial Data In Pin

SI is the Serial Data Input Pin for the SPI Interface. The eight power outputs are controlled by the serial data via the output data buffer. This input has a Schmitt Trigger.

STR Strobe Pin for the SPI Interface

When the STR Pin is high, data from the 8-bit shift register is passed into the output data buffers where it controls the ON-OFF state of each output driver. The data is latched in the output data buffers when STR goes low. This input has a Schmitt trigger.

SO Serial Data Out Pin

The serial data out allows other ICs to be serially cascaded. For example, a 10-bit LED driver may be located behind the HIP0050. A controlling microprocessor may then clock out 18-bits of information and simultaneously strobe both parts. The cascaded ICs may be the same or different from the HIP0050.

DR0 - DR7 Outputs 0 Thru 7

The drain output pins of the DMOS Power Drivers are capable of sinking 300mA. Each output has short circuit protection to independently shutdown the output under excessive high load current conditions.

$\overline{FLT}$ Fault Flag

The fault flag pin indicates an over-current in any one of the output drivers. (It is not an indicator for the thermal shutdown mode.) The $\overline{FLT}$ output is active low and can sink 1.6mA when activated. When latched low, it will remain latched until the next data strobe.

$\overline{EN}$ Enable Pin

The enable pin is an active low enable function for all eight output drivers. When $\overline{EN}$ is high, drive from the output data buffer is held low and all output drivers are disabled. When $\overline{EN}$ is low, the output drivers are enabled and data in the 8-bit shift register is transparent to the output data buffer. This input has a Schmitt trigger.

LGND and GND Pins

The LGND Pin is the 5V Logic Supply Ground for the IC and GND is a common ground for the power output drivers.

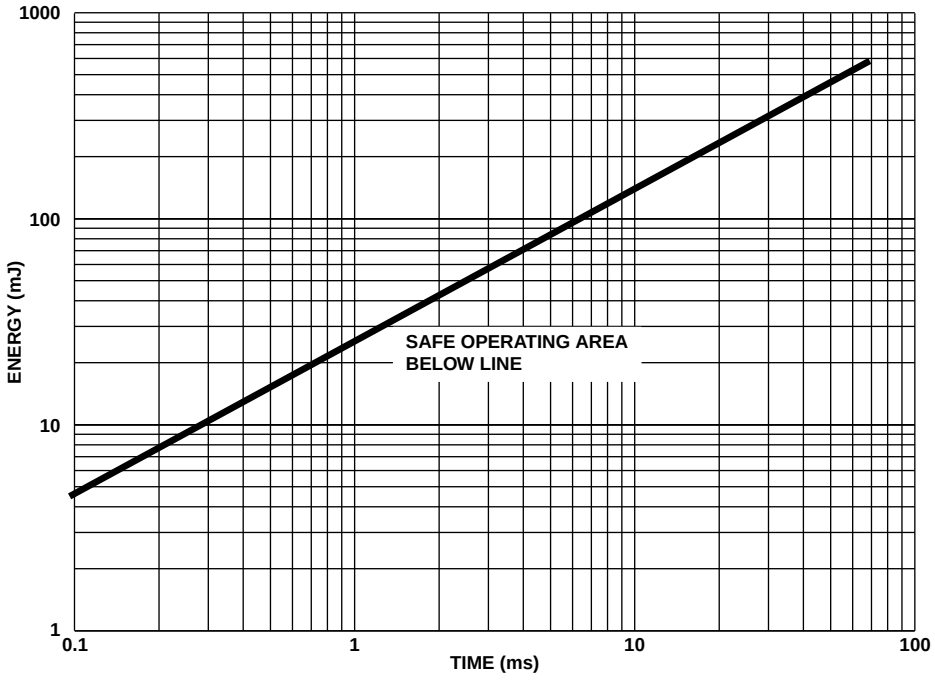
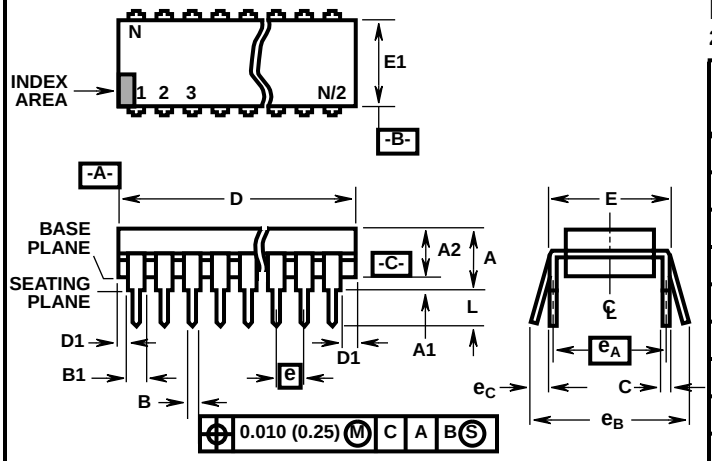


FIGURE 2. MAXIMUM SINGLE PULSE ENERGY SAFE OPERATING AREA FOR EACH CLAMPED OUTPUT DRIVER, $T_A = 25^oC$

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

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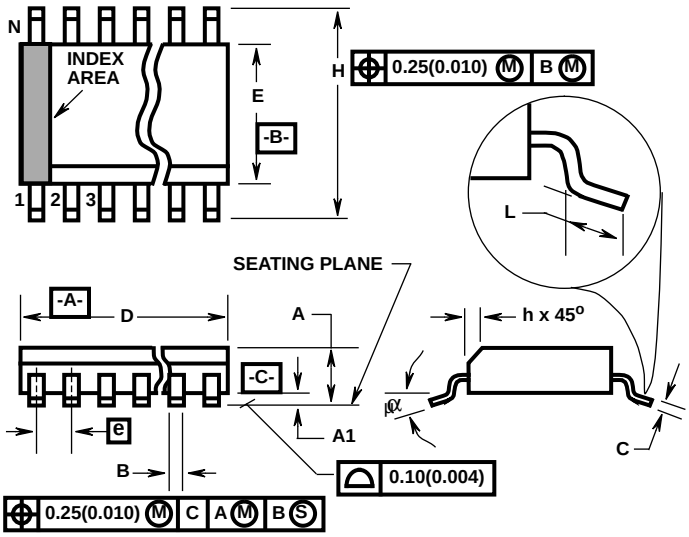
Small Outline Plastic Packages (SOIC)



M24.3 **(JEDEC MS-013-AD ISSUE C)**
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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