

HB56SW872ES-6/7

64 MB Buffered EDO DRAM DIMM
8-Mword $\times$ 72-bit, 4 k Refresh, 2-Bank Module
(36 pcs of 4 M $\times$ 4 Components)

HITACHI

ADE-203-765B (Z)
Rev. 2.0
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Description

The HB56SW872ES belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56SW872ES is a $8\text{M} \times 72$ dynamic RAM module, mounted 36 pieces of 16-Mbit DRAM (HM51W16405) sealed in TCP package and 2 pieces of 16-bit BiCMOS line driver (74LVT16244) sealed in TSSOP package. The HB56SW872ES offers Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56SW872ES is 168-pin socket type package (dual lead out). Therefore, the HB56SW872ES makes high density mounting possible without surface mount technology. The HB56SW872ES provides common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 3.3 V (+0.3/−0.15 V) supply
- JEDEC standard outline buffered 8 byte DIMM
- High speed
 - Access time: $t_{\text{RAC}} = 60/70$ ns (max)
: $t_{\text{CAC}} = 20/23$ ns (max)
- Low power dissipation
 - Active mode: 5.54/4.90 W (max)
 - Standby mode (TTL): 295.2 mW (max)
(CMOS): 165.6 mW (max)
- Buffered input except $\overline{\text{RAS}}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- EDO page mode capability
- 4,096 refresh cycle: 64 ms

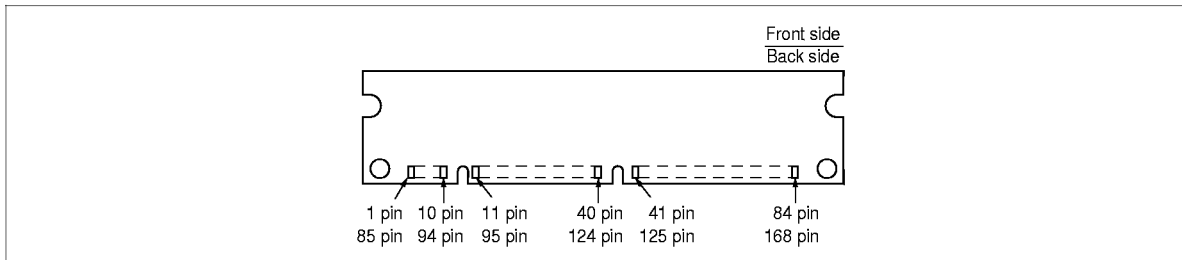
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- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh

Ordering Information

Type No.	Access time	Package	Contact pad
HB56SW872ES-6	60 ns	168-pin dual lead out socket type	Gold
HB56SW872ES-7	70 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	13	DQ9	25	NC	37	A8
2	DQ0	14	DQ10	26	V_{CC}	38	A10
3	DQ1	15	DQ11	27	$\overline{\text{WE0}}$	39	NC
4	DQ2	16	DQ12	28	$\overline{\text{CE0}}$	40	V_{CC}
5	DQ3	17	DQ13	29	NC	41	NC
6	V_{CC}	18	V_{CC}	30	$\overline{\text{RE0}}$	42	NC
7	DQ4	19	DQ14	31	$\overline{\text{OE0}}$	43	V_{SS}
8	DQ5	20	DQ15	32	V_{SS}	44	$\overline{\text{OE2}}$
9	DQ6	21	DQ16	33	A0	45	$\overline{\text{RE2}}$
10	DQ7	22	DQ17	34	A2	46	$\overline{\text{CE4}}$
11	DQ8	23	V_{SS}	35	A4	47	NC
12	V_{SS}	24	NC	36	A6	48	$\overline{\text{WE2}}$

Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
49	V _{CC}	79	PD1	109	NC	139	DQ56
50	NC	80	PD3	110	V _{CC}	140	DQ57
51	NC	81	PD5	111	NC	141	DQ58
52	DQ18	82	PD7	112	$\overline{\text{CE1}}$	142	DQ59
53	DQ19	83	ID0 (V _{SS})	113	NC	143	V _{CC}
54	V _{SS}	84	V _{CC}	114	$\overline{\text{RE1}}$	144	DQ60
55	DQ20	85	V _{SS}	115	NC	145	NC
56	DQ21	86	DQ36	116	V _{SS}	146	NC
57	DQ22	87	DQ37	117	A1	147	NC
58	DQ23	88	DQ38	118	A3	148	NC
59	V _{CC}	89	DQ39	119	A5	149	DQ61
60	DQ24	90	V _{CC}	120	A7	150	DQ62
61	NC	91	DQ40	121	A9	151	DQ63
62	NC	92	DQ41	122	A11	152	V _{SS}
63	NC	93	DQ42	123	NC	153	DQ64
64	NC	94	DQ43	124	V _{CC}	154	DQ65
65	DQ25	95	DQ44	125	NC	155	DQ66
66	DQ26	96	V _{SS}	126	B0	156	DQ67
67	DQ27	97	DQ45	127	V _{SS}	157	V _{CC}
68	V _{SS}	98	DQ46	128	NC	158	DQ68
69	DQ28	99	DQ47	129	$\overline{\text{RE3}}$	159	DQ69
70	DQ29	100	DQ48	130	$\overline{\text{CE5}}$	160	DQ70
71	DQ30	101	DQ49	131	NC	161	DQ71
72	DQ31	102	V _{CC}	132	$\overline{\text{PDE}}$	162	V _{SS}
73	V _{CC}	103	DQ50	133	V _{CC}	163	PD2
74	DQ32	104	DQ51	134	NC	164	PD4
75	DQ33	105	DQ52	135	NC	165	PD6
76	DQ34	106	DQ53	136	DQ54	166	PD8
77	DQ35	107	V _{SS}	137	DQ55	167	ID1 (V _{SS})
78	V _{SS}	108	NC	138	V _{SS}	168	V _{CC}

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Pin Description

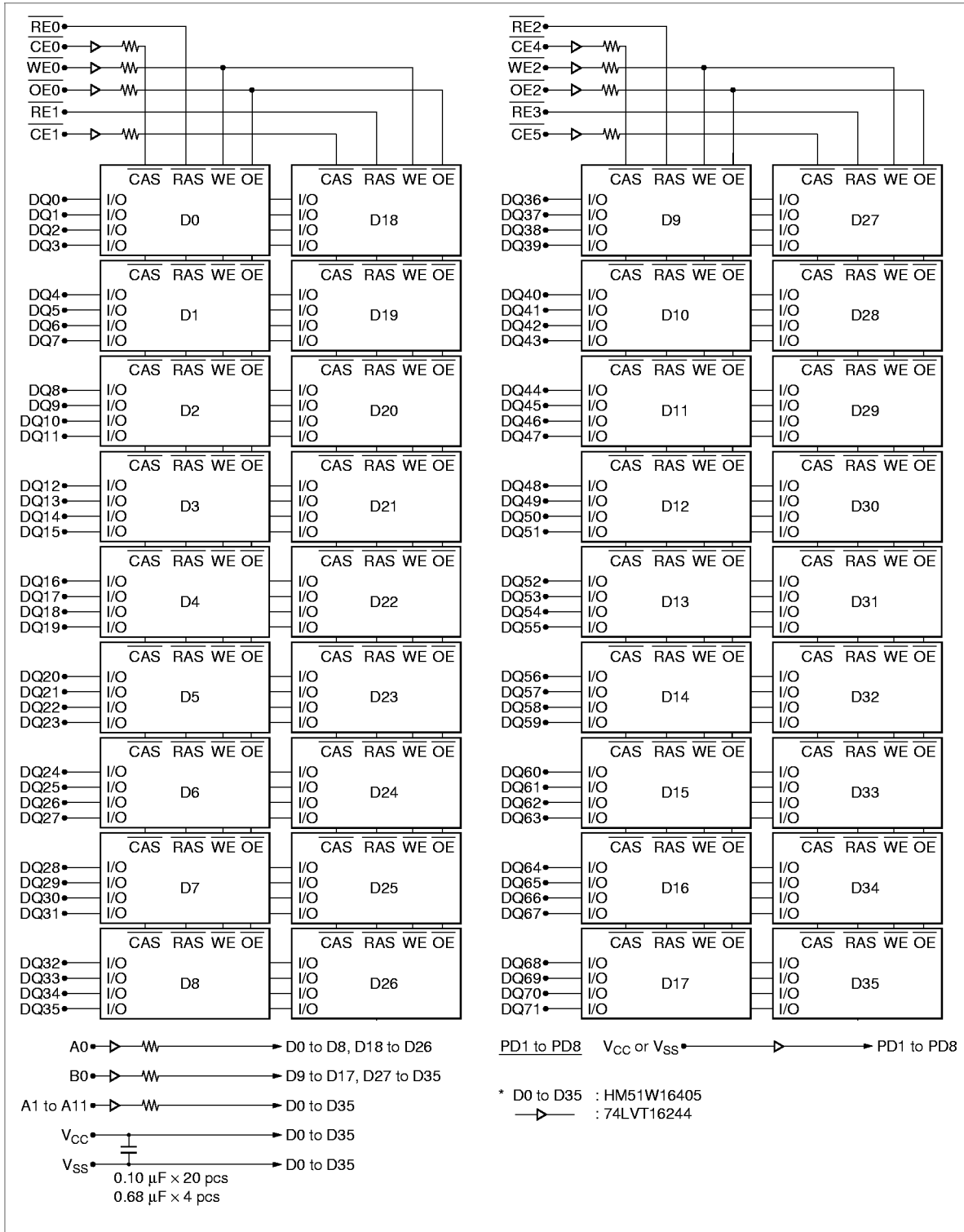
Pin name	Function
A0 to A11, B0	Address Input Row Address : A0 to A11, B0 Column Address : A0 to A9, B0 Refresh Address : A0 to A11, B0
DQ0 to DQ71	Data-in/Data-out
$\overline{RE0}$ to $\overline{RE3}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$, $\overline{CE1}$, $\overline{CE4}$, $\overline{CE5}$	Column address strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/Write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD8	Presence detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence detect enable
NC	No connection

Presence Detect Pin Assignment

Pin name	Pin No.	$\overline{PDE}$ = Low		$\overline{PDE}$ = High
		60 ns	70 ns	All
PD1	79	0	0	High-Z
PD2	163	0	0	High-Z
PD3	80	1	1	High-Z
PD4	164	1	1	High-Z
PD5	81	1	1	High-Z
PD6	165	1	0	High-Z
PD7	82	1	1	High-Z
PD8	166	0	0	High-Z

Note: 1: High level (Driver output)
0: Low level (Driver output)

Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	19	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.15	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 3.3\text{ V} +0.3/-0.15\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I_{CC1}	—	1540	—	1360	mA	$t_{RC} = \min$	1, 2
Standby current	I_{CC2}	—	82	—	82	mA	TTL interface $\overline{RAS}, \overline{CAS} = V_{IH}$ Dout = High-Z	
		—	46	—	46	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
$\overline{RAS}$ -only refresh current	I_{CC3}	—	1540	—	1360	mA	$t_{RC} = \min$	2
Standby current	I_{CC5}	—	190	—	190	mA	$\overline{RAS} = V_{IH}, \overline{CAS} = V_{IL}$ Dout = enable	1
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	—	1540	—	1360	mA	$t_{RC} = \min$	
EDO page mode current	I_{CC7}	—	1360	—	1270	mA	$t_{HPC} = \min$	1, 3
Input leakage current	I_{LI}	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 4.6\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 4.6\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V} +0.3/-0.15\text{ V}$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{CE}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RE}$)	C_{I3}	—	78	pF	1
Output capacitance (DQ)	$C_{I/O}$	—	27	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable Dout.

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AC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 3.3\text{ V} +0.3/-0.15\text{ V}$, $V_{SS} = 0\text{ V}$)^{*1, *2, *18, *19}

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	5	—	5	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	40	14	47	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	12	30	ns	4
$\overline{RAS}$ hold time	t_{RSH}	18	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	20	—	23	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7
Refresh period (4,096 cycles)	t_{REF}	—	64	—	64	ms	

Read Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	23	ns	9, 10, 17
Access time from address	t_{AA}	—	35	—	40	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	20	—	23	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	22
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	ns	13, 22
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	20	—	20	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	20	—	23	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	22
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	20	—	20	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	20	—	23	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	t_{RNCD}	60	—	70	—	ns	

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Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WCP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	—	18	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	15	—	18	—	ns	15

Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	49	—	57	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEHL}	15	—	18	—	ns	

Refresh Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	5	—	5	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	ns	

EDO Page Mode Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	40	—	45	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	40	—	45	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	t_{HPRWC}	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	62	—	ns	14

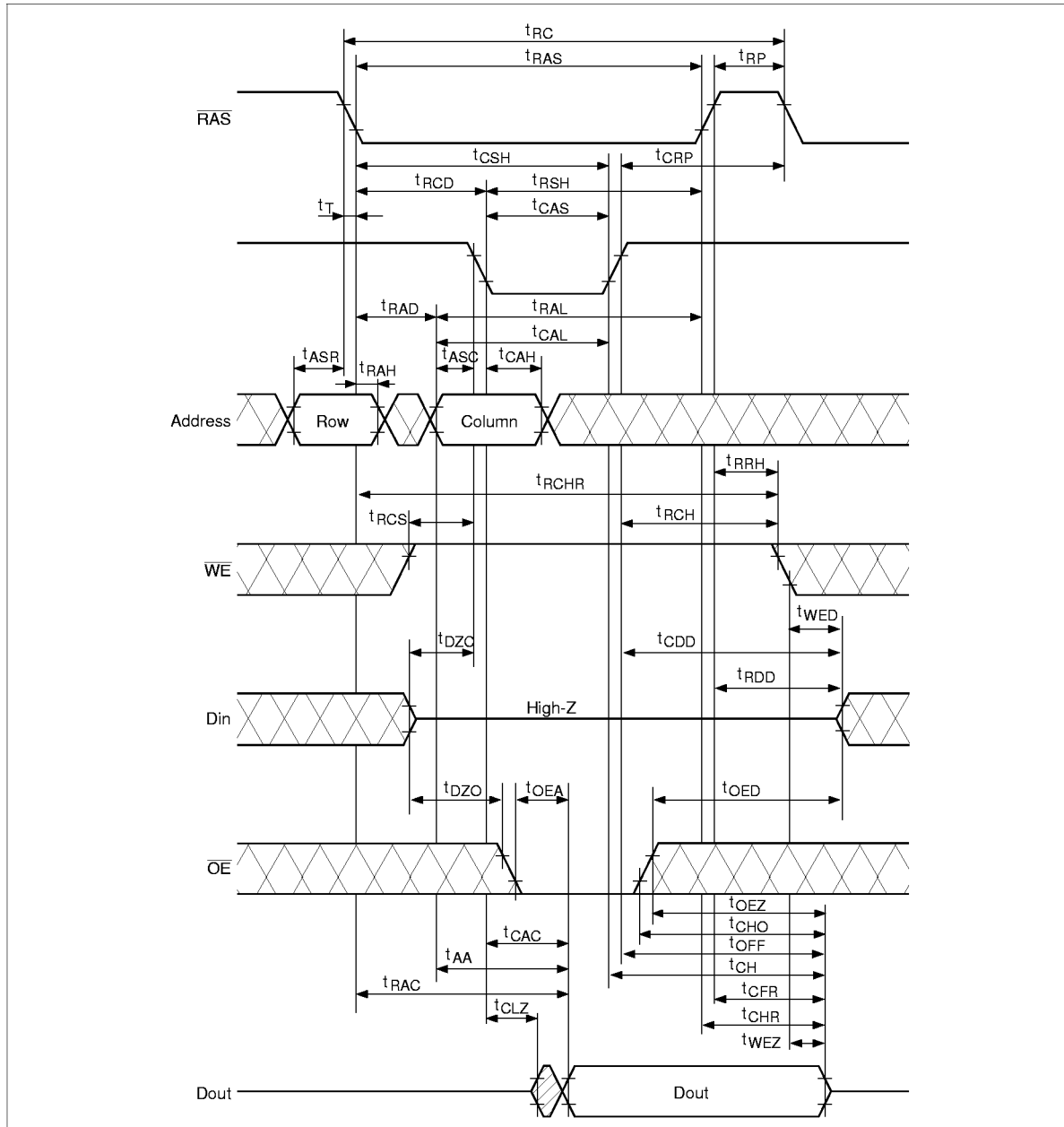
Notes: 1. AC measurements assume $t_T = 2$ ns.

2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh cycle or $\overline{CAS}$ -before- $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RAD}$ (max) + t_{AA} (max) - t_{CAC} (max), then access time is controlled exclusively by t_{CAC} .
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} , and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\min)$, $t_{CWD} \geq t_{CWD}(\min)$, and $t_{AWD} \geq t_{AWD}(\min)$ or $t_{CWD} \geq t_{CWD}(\min)$, $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CPW} \geq t_{CPW}(\min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OE} \geq t_{CWL}$, the DQ pin will remain open circuit (high impedance); $t_{OE} < t_{CWL}$, invalid data will be out at each DQ.
19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
20. $t_{HPC}(\min)$ can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_r$) becomes greater than the specified $t_{HPC}(\min)$ value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH}(\min)/V_{IL}(\max)$ level.
22. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
23. XXX: H or L (H: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$)
////////: Invalid Dout
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

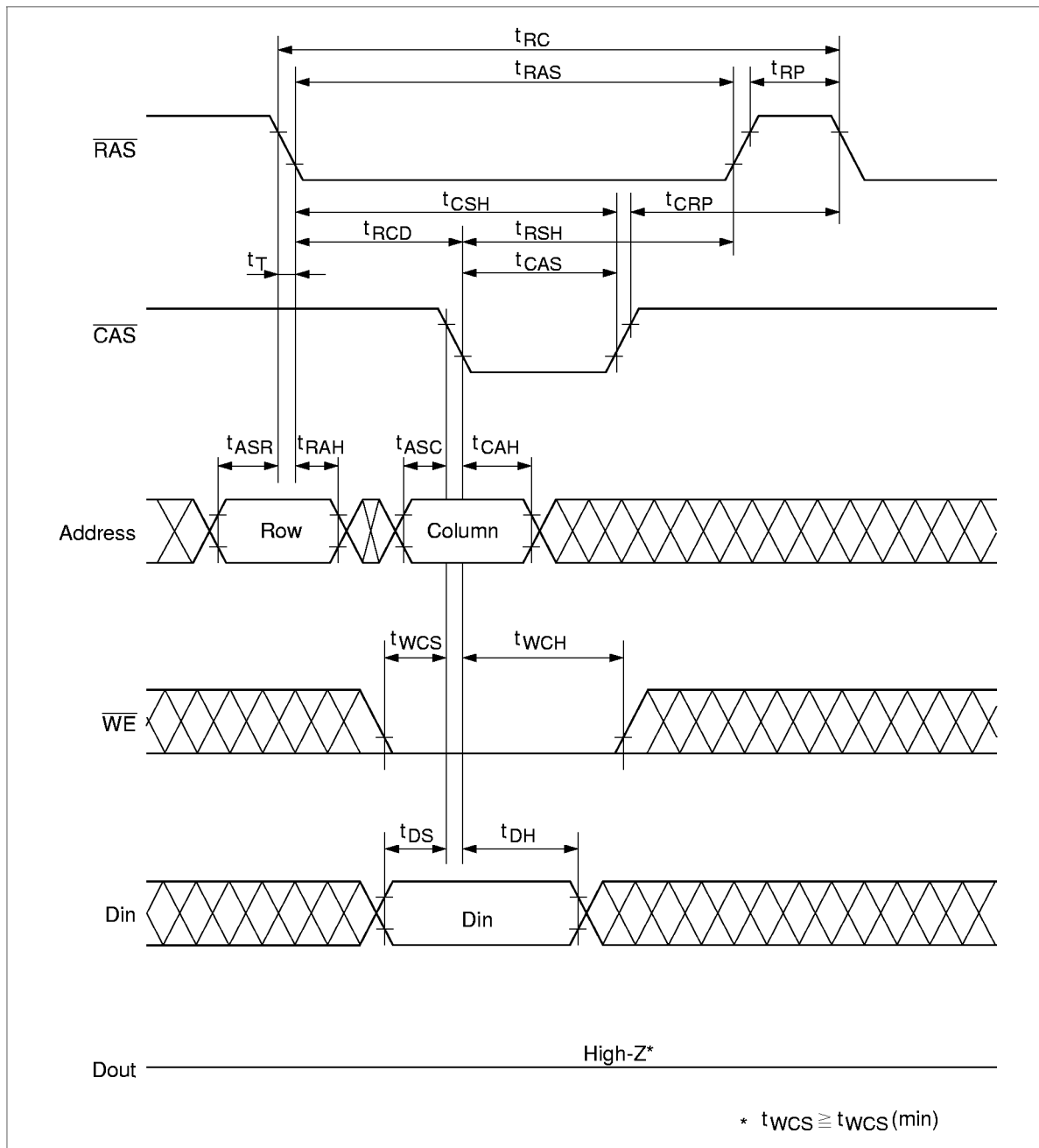
Timing Waveforms*²³

Read Cycle

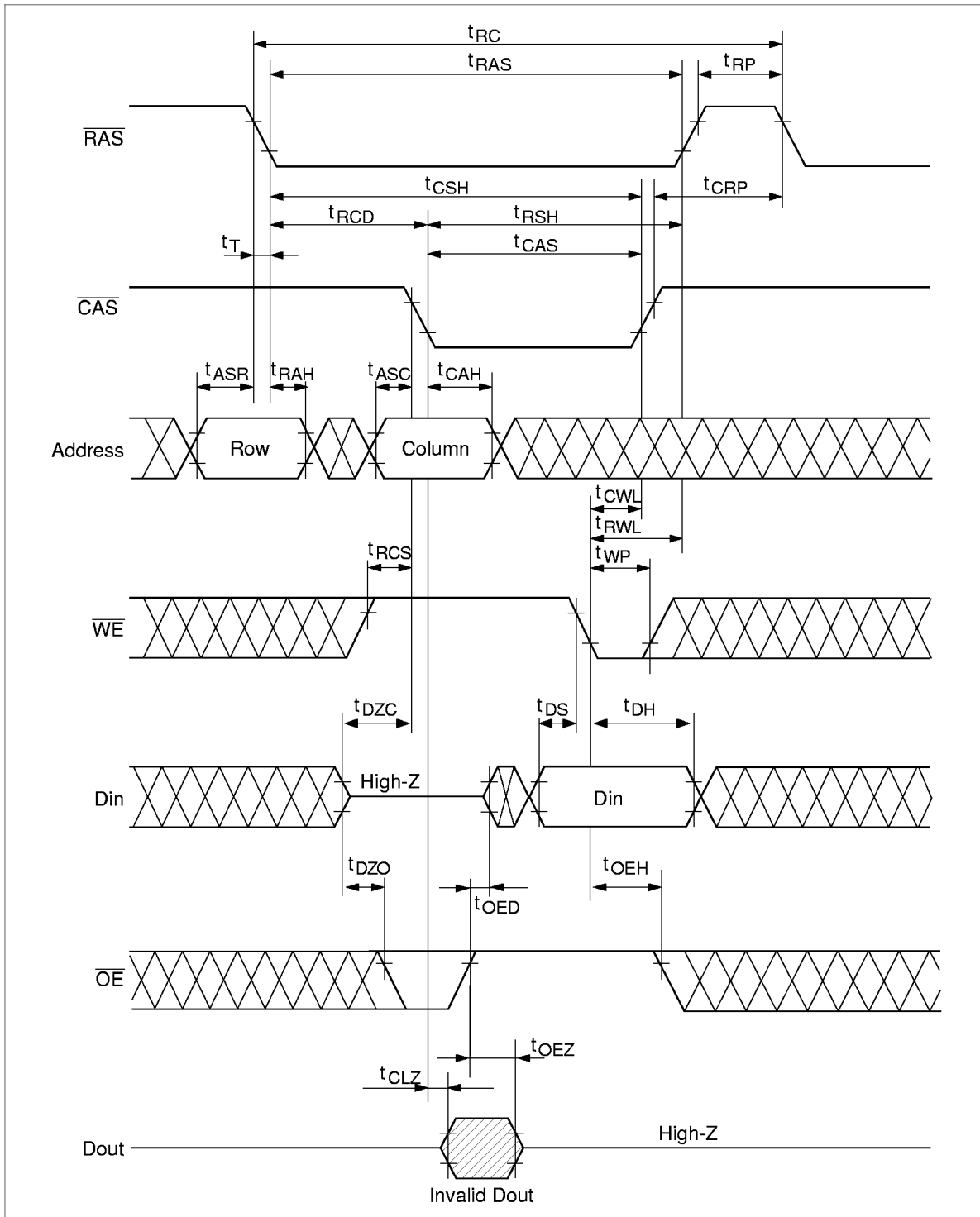


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Early Write Cycle

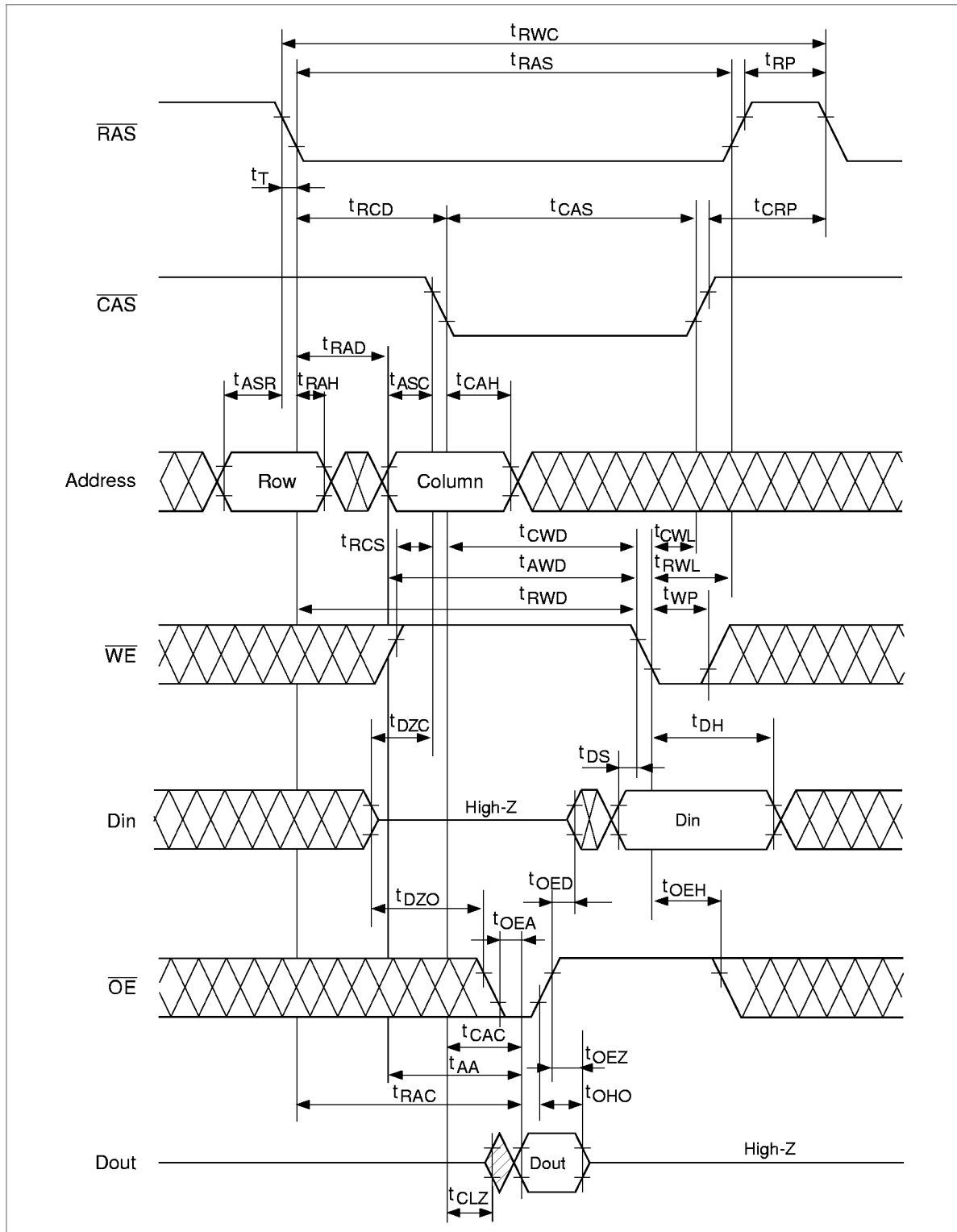


Delayed Write Cycle*18

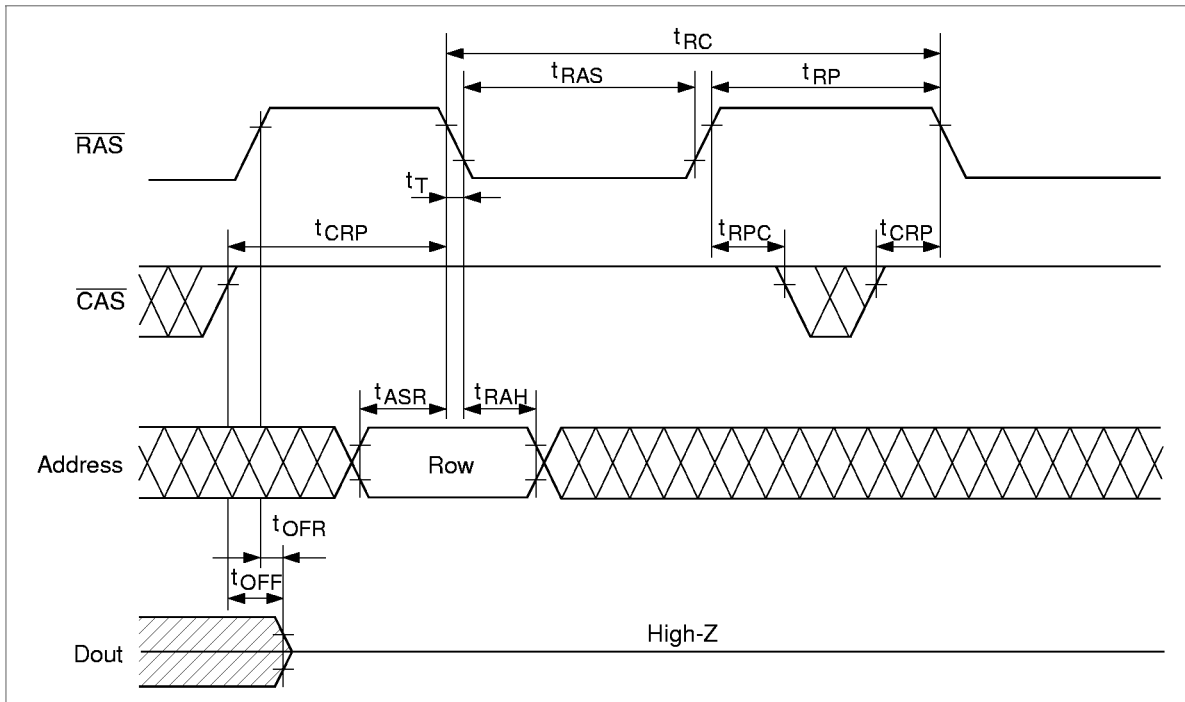


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Read-Modify-Write Cycle*18

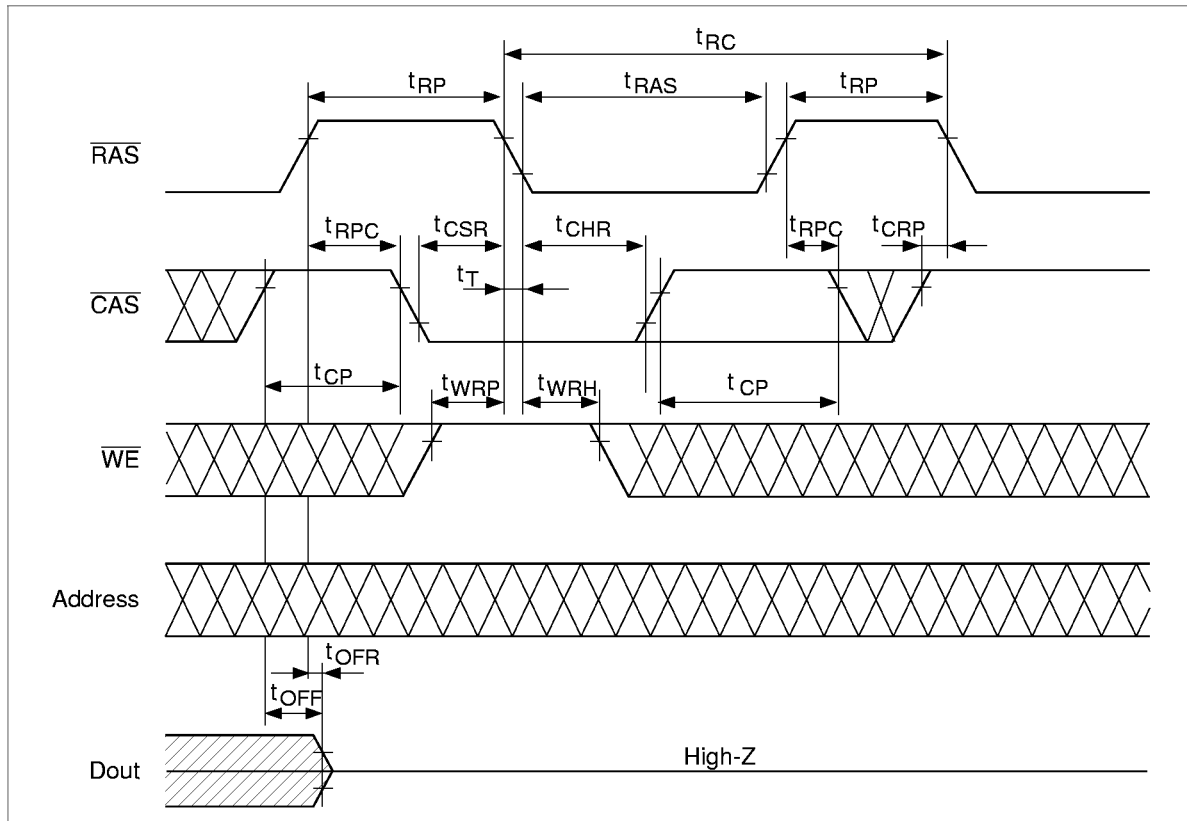


RAS-Only Refresh Cycle

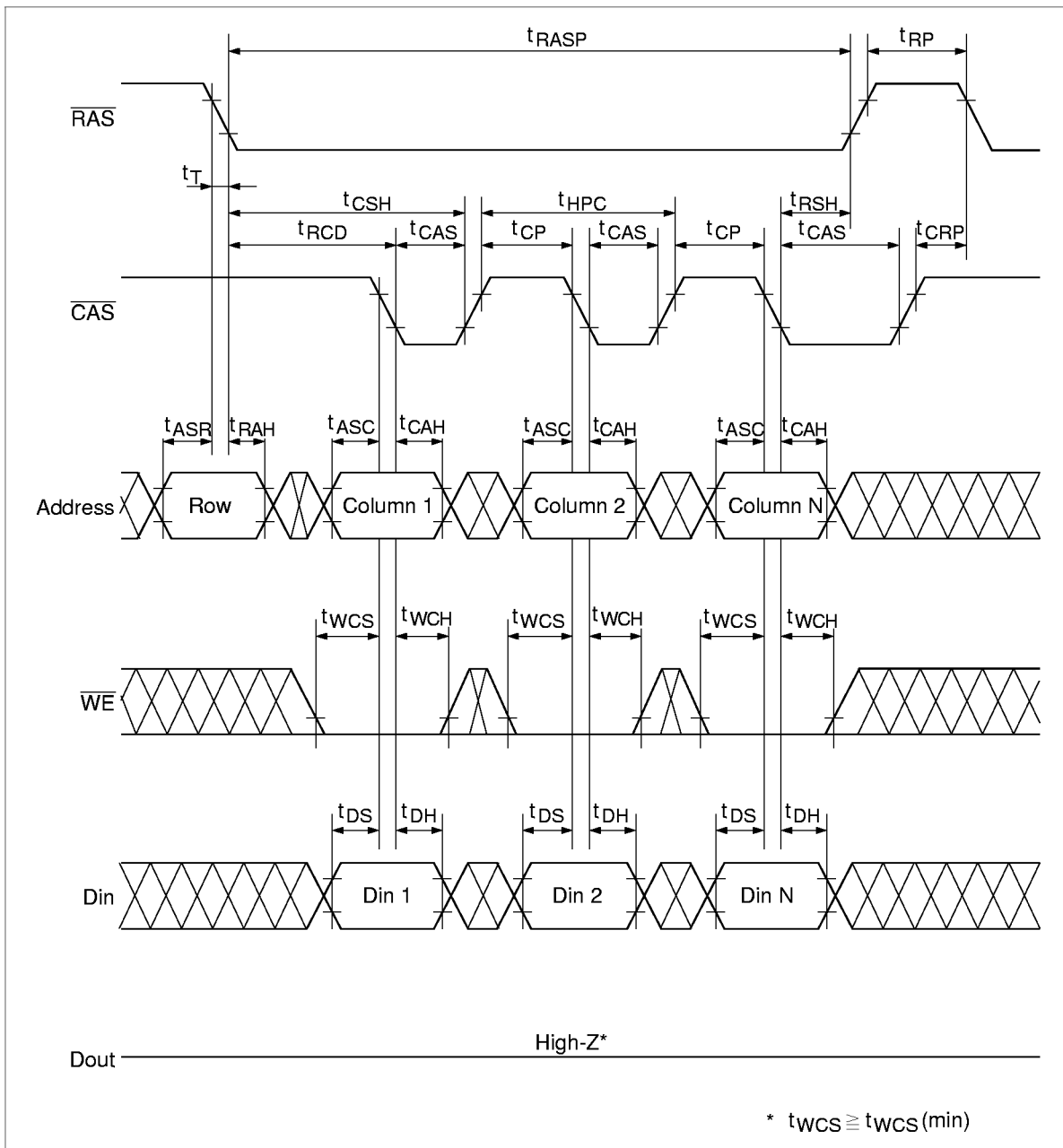


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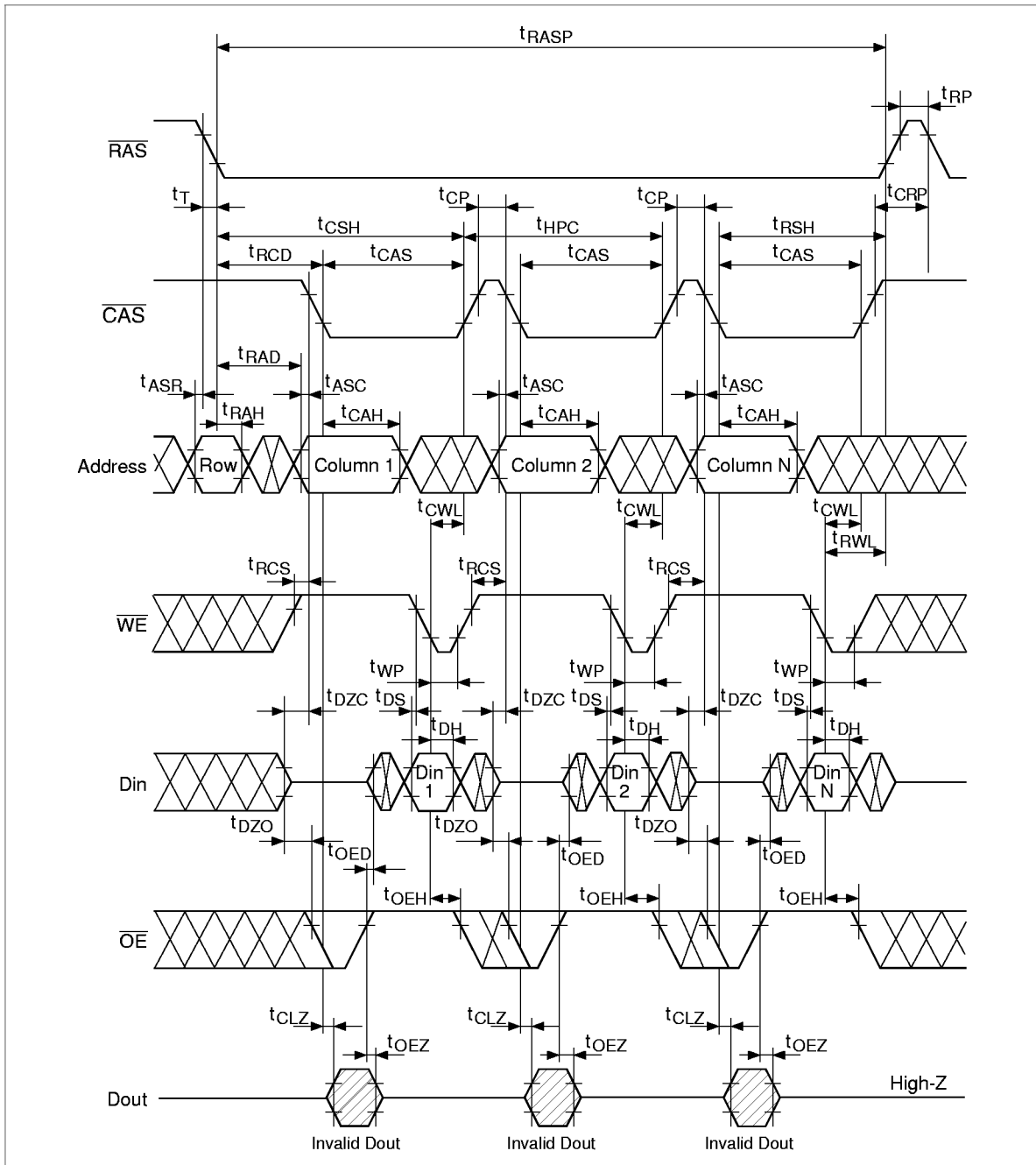
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

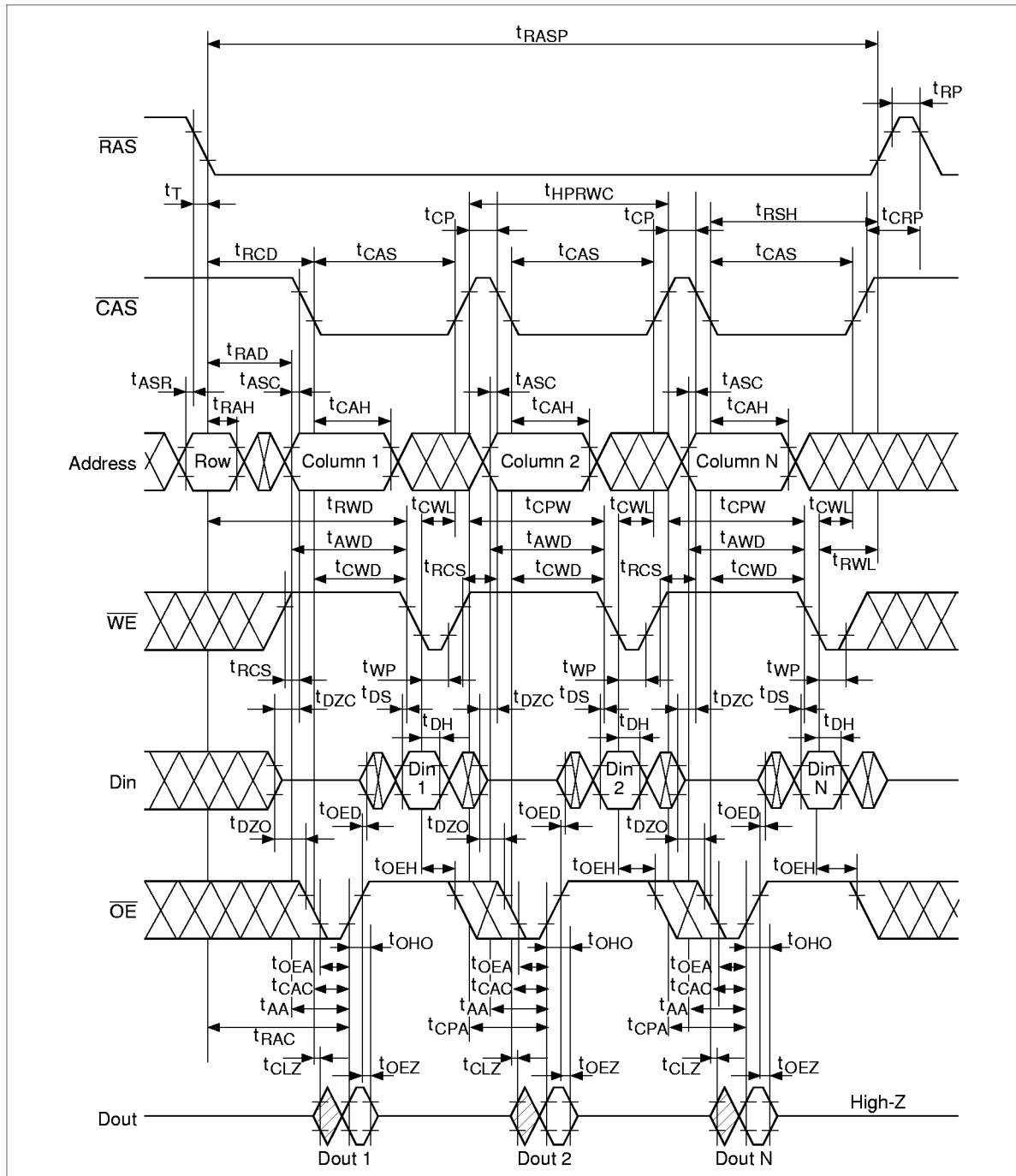


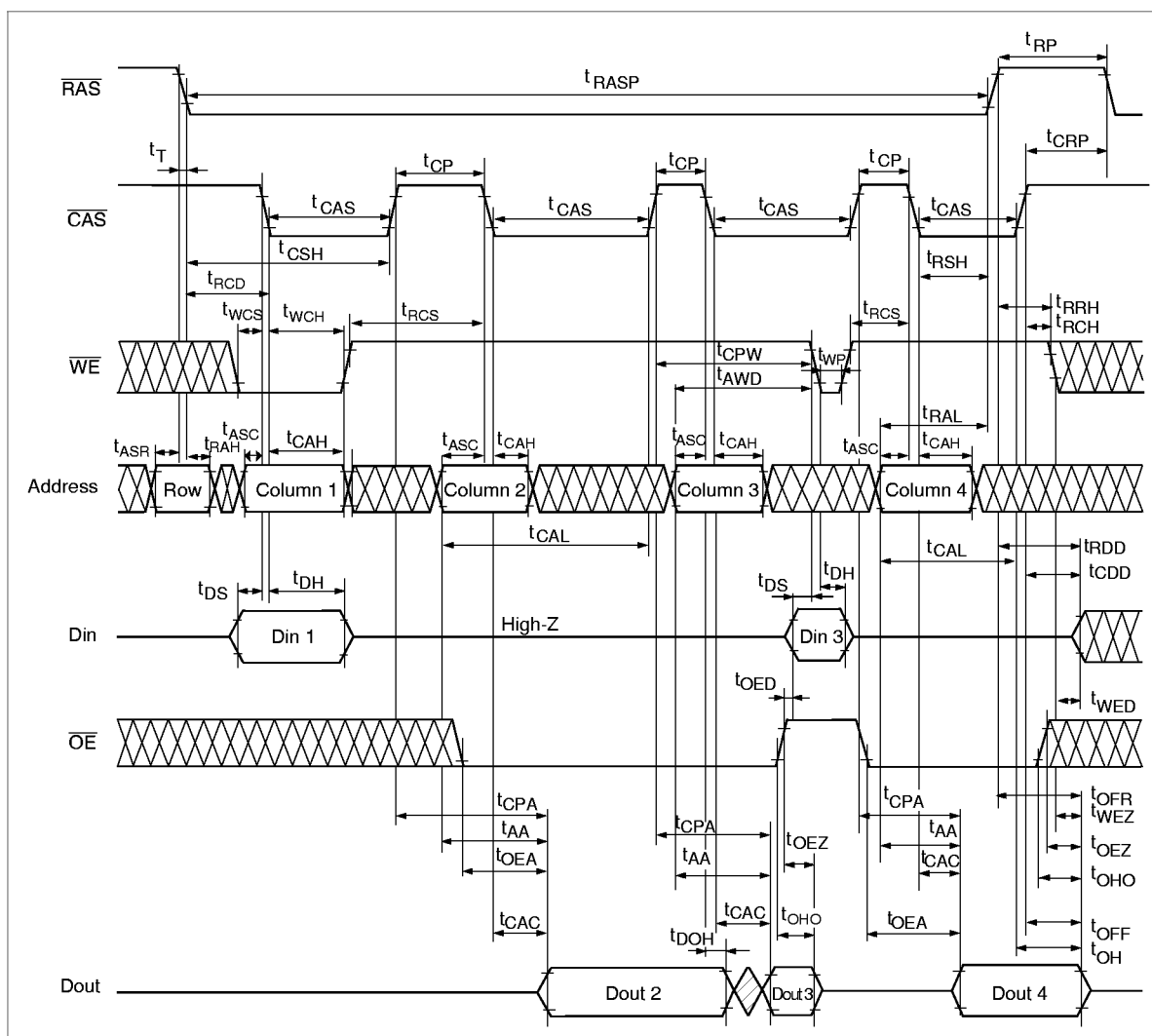
EDO Page Mode Early Write Cycle

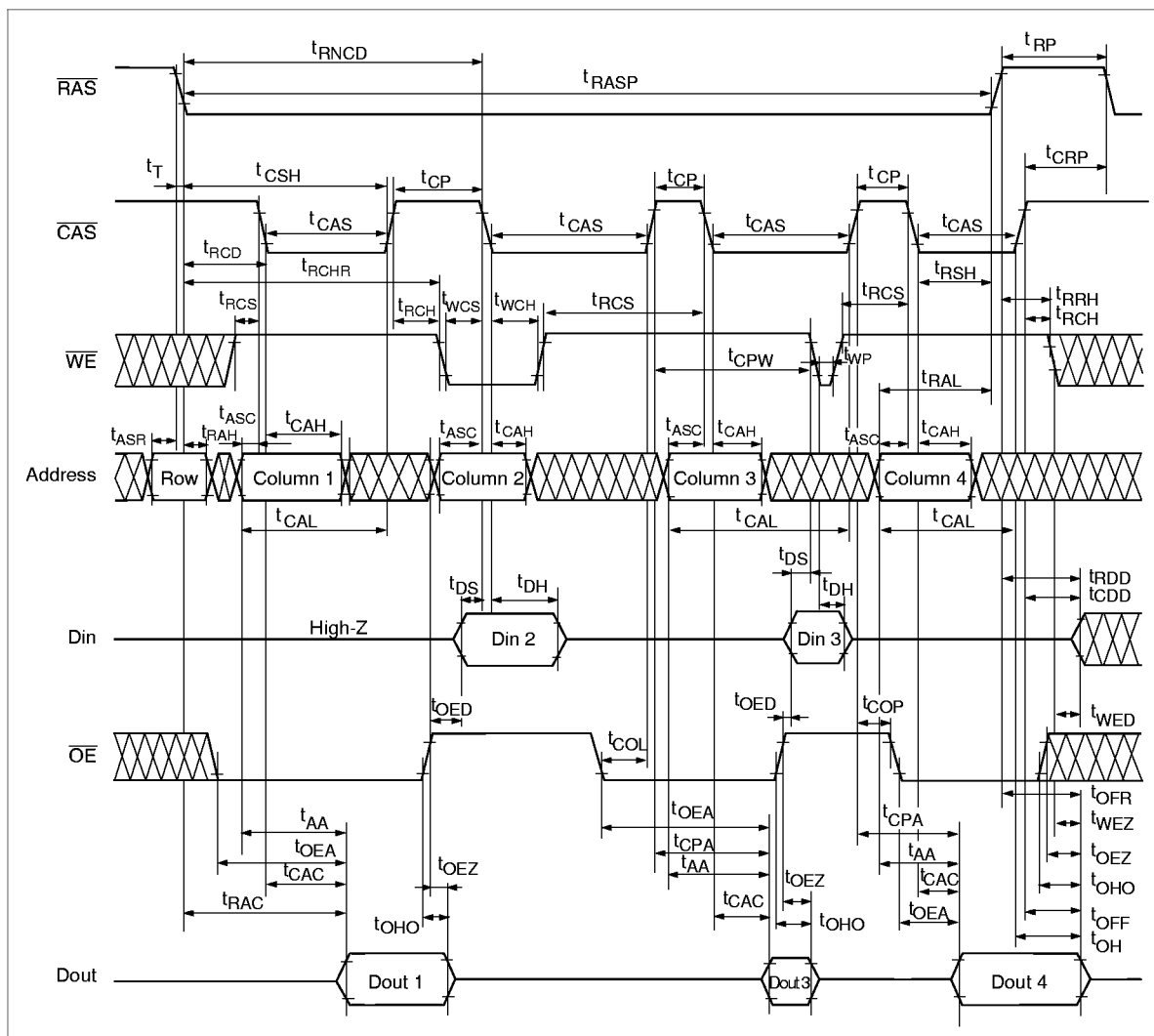


EDO Page Mode Delayed Write Cycle*18









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HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan

Tel: Tokyo (03) 3270-2111

Fax: (03) 3270-5109

For further information write to:

Hitachi Semiconductor
(America) Inc.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1897
U S A

Tel: 800-285-1601

Fax: 303-297-0447

Hitachi Europe GmbH
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München

Tel: 089-9 91 80-0

Fax: 089-9 29 30-00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 01628-585000
Fax: 01628-585160

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

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1.0	Apr. 4, 1997	Initial issue	S. Tsukui	K. Tsuneda
2.0	Nov. 1997	Change of Subtitle		