Final

Am99C10

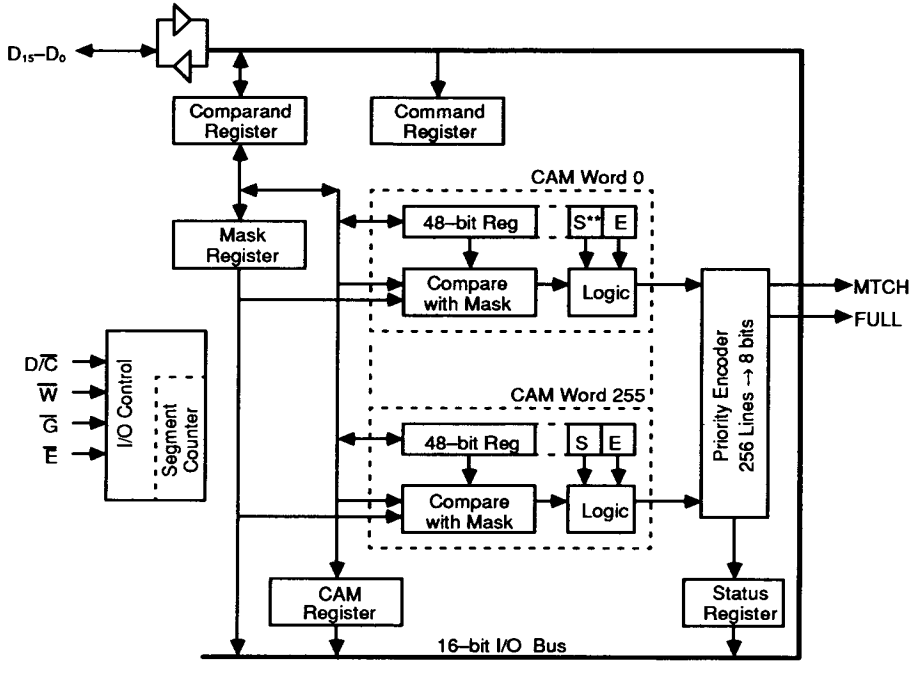
256 x 48 Content Addressable Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **256 word x 48-bit Content Addressable Memory (CAM)**
  - Optimized for Address Decoding in Local Area Networks (LAN) and bridging applications
- **Each CAM word has a 48-bit register and 48-bit maskable comparator**
  - Maskable-bits and maskable-words
- **48-bit input word compared against all 256 words in the CAM in a single (100ns) cycle**
- **Single and multiple match detection with fast on-chip priority address encoder**
- **Single cycle reset on all 256 words of the CAM Array**
- **User programmable word width of 16 bit or 48 bit**
- **Flexible operation and diagnostics capability through user programmable control logic**
- **TTL-compatible inputs and outputs**
- **Available in a 28-pin 400 mil CERDIP, (300 mil plastic DIP and 32-pin PLCC under development).**
- **Low power CMOS technology**
  - 715mW max. operating power
  - 55mW max. standby

BLOCK DIAGRAM



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GENERAL DESCRIPTION

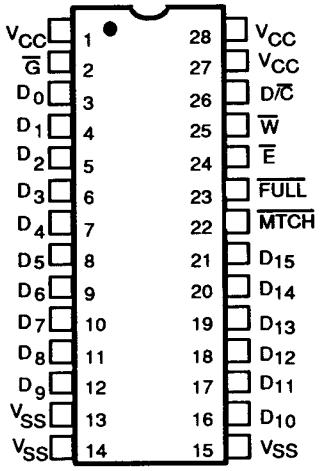
The Am99C10 is a high performance Content Addressable Memory (CAM) with a capacity of 256 words and a user-programmable word width of 16 bits or 48 bits. The Am99C10 is ideal for use in high speed Ethernet and FDDI local area network applications where it can function as an address filter and perform the network address look-up function. It can also find use in Database Machines, File Servers, Image Processing, Neural Networks and many other applications.

The Am99C10 CAM is composed of 256 words, each consisting of a 48-bit comparator and a 48-bit register. A block diagram of the Am99C10 is shown below. When data (the comparand) is presented to the CAM array, a simultaneous compare operation is performed between the comparand and all data (256 words) in the CAM in a single cycle. When the comparand and a word in the CAM are matched, the on-chip priority encoder generates a match word address identifying the location of the data in the CAM. If multiple matches occur, the encoder generates the lowest matched address. Any or all bits of the comparand value can be selectively masked. The masked bits do not participate in the compare decisions, allowing comparison on a portion of the data word.

The Am99C10 is user programmable. The user can read and write to any location in the CAM Array and to all of the Am99C10 internal registers. Each word in the CAM array can be loaded with data or set to the empty state so that it does not participate in match operations. All words in the CAM Array can be set to empty in a single cycle.

The Am99C10 is manufactured with state-of-the-art CMOS processing technology. It is assembled in a 28 pin, 400 mil CERDIP; a 300 mil plastic DIP and a 32 pin PLCC are under development, and require a single 5-V power supply.

CONNECTION DIAGRAM



V_{CC} = Power Supply
V_{SS} = Ground

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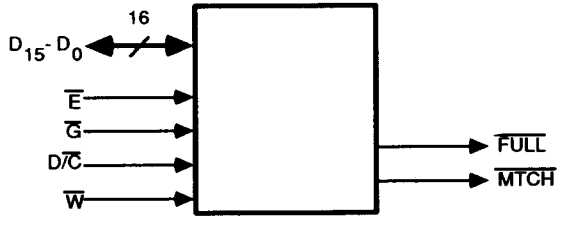
LOGIC SYMBOL



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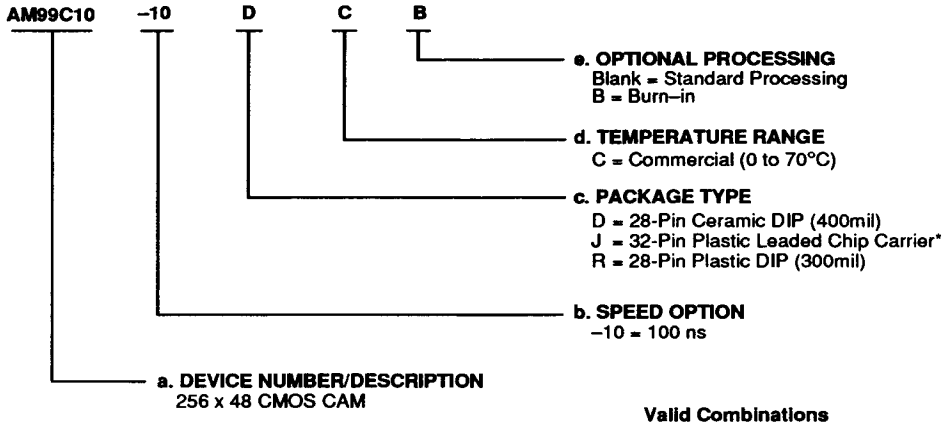
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM99C10	RC, RCB DC, DCB JC*, JCB*

* Under development

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

D/$\overline{C}$

Data/Command mode selection, Input, TTL

A LOW on this input selects the command mode. A HIGH on this input selects the data mode.

$\overline{W}$

Write enable, Input, TTL

This pin controls the writing of the internal registers and the CAM Array. New data may be written into a register or memory by forcing the appropriate state of D/$\overline{C}$ and $\overline{E}$, and by switching $\overline{W}$ LOW and back HIGH.

$\overline{G}$

Output Enable, Input, TTL

This pin controls reading of the internal registers. A LOW on both the $\overline{E}$ and $\overline{G}$ inputs gates the selected register onto the data bus and turns on the output drivers.

$\overline{E}$

Chip Enable, Input, TTL

A LOW on this input enables the chip operations as specified by the state of D/$\overline{C}$, $\overline{W}$, $\overline{G}$ inputs and the Command Register. A high on this pin powers down the chip. This signal must be low during all operations including match.

D_{15-0}

Data Bus, 16-bit, Bidirectional, Three-state

D0 is the least significant bit position and D_{15} is the most significant bit position. A HIGH on the Data Bus specifies logic 1 and a LOW specifies logic 0. The Data Bus is not driven by the device when $\overline{W}$ is LOW, when $\overline{G}$ is HIGH or when chip enable $\overline{E}$ is HIGH.

$\overline{FULL}$

Address Full, Output, TTL

A LOW on this output indicates that all the words in the 256 address locations in CAM Array are full. A HIGH on this output indicates that one or more words in the CAM Array are still available or that the $\overline{FULL}$ output is disabled. The $\overline{FULL}$ output is in the HIGH state when $\overline{E}$ is HIGH and is valid otherwise.

$\overline{MTCH}$

Match, Output, TTL

A LOW on this output indicates that the masked data of the Comparand Register and one or more words in the CAM Array are matched. A HIGH on this output indicates that a mismatch has taken place or that the match output is disabled. The match output is in the HIGH state when $\overline{E}$ is HIGH and is valid otherwise.

V_{CC}

Power Supply Pin, Input, +5 Volts

V_{SS}

Ground Supply Pin, Input, 0 Volts

FUNCTIONAL DESCRIPTION

The CAM ARRAY is a bank of 256 CAM words, each a combination of a 48 bit wide logic comparator and a 48 bit register, as shown in Figure 1. The CAM Array compares a 48 bit input data word against all of its 256 words simultaneously for logic equality in one cycle. If any of the CAM Array 256 words find an exact match with the incoming bit pattern, the CAM Array raises a Match flag and outputs the 8 bit address of the matching word.

When a Match cycle is initiated, every CAM word compares each bit in its register against the appropriate bit of the incoming 48 bit pattern. Additionally, a logic "1" (HIGH level) set in any Mask Register bit will disable that bit position in the CAM Array. A match is declared if all enabled CAM cells find an exact comparison with the input data. The CAM Array word that finds a match activates an internal signal called the Match Line (ML). There are 256 match lines: ML0-ML255.

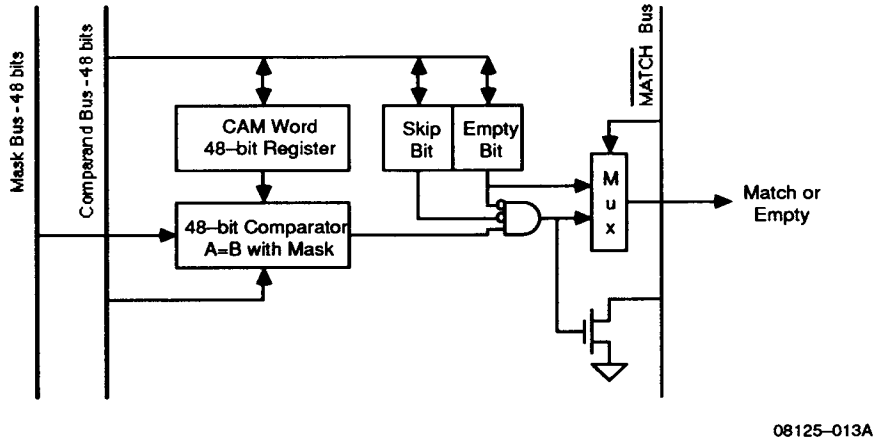


Figure 1. CAM Word Block Diagram

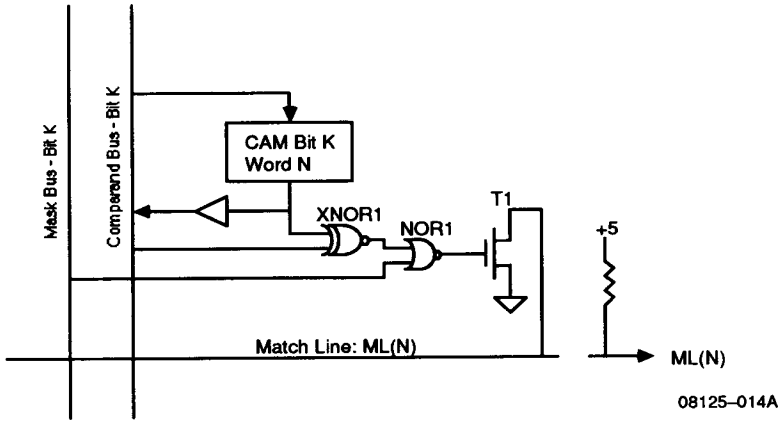


Figure 2. CAM Bit Block Diagram

Each CAM word consists of 48 CAM data bits. Each CAM data bit consists of a register bit latch, an exclusive-NOR comparator, an OR gate for masking, and a transistor for performing a 48-bit wire-AND across the 48 data bits, as shown in Figure 2. The logic comparator exclusive-Nors the contents of the register bit with the corresponding bit of the Comparand Register. A match between the two bits result in a HIGH level at the output of the exclusive-Nor gate (XNOR1). The output of XNOR1 is further gated (Nor function) with a bit of the Mask Register. A HIGH level on either one of the inputs to NOR1 forces its output LOW, indicating a match. The ML signal will stay HIGH (indicating a match for that CAM word) if all 48 CAM cells of this word have their T1 transistors shut off by their NOR1 gates. If any one of the 48 NOR1outputs is HIGH, the ML line will be forced LOW, indicating a mismatch.

The Priority Encoder identifies the address of the CAM word that found a match. All 256 comparators of the CAM Array receive the same bit pattern for matching at the same time, and more than one of them can find a match with the masked data. All 256 ML lines are presented to the Priority Encoder block that decides which comparator of the ones that activate their MLs has the lowest address. If at least one ML is active the Priority Encoder will activate the $\overline{\text{MTCH}}$ line and at the same time will set the $\overline{\text{MTC}}$ bit in the Status Register. The Priority Encoder will transfer the 8 bit address of the lowest matching CAM Array word to the Status Register.

Each of the 256 words of the CAM Array has two additional bits of memory associated with it – A Skip bit and an Empty bit. These are shown in the CAM Word Block Diagram. The actual size of the CAM is therefore 256 X 50 (48+2). Both the Skip and the Empty bits can disable a match for their word. The Skip bit can be used in situations where there are multiple matches – it gives the user the ability to detect additional words that were matched other than the one with the lowest address. The Empty bit indicates available or empty addresses in the CAM into which data can be written.

The Empty bit is also used by the Priority Encoder. The Priority Encoder identifies the lowest address of an Empty CAM Array word if no match occurred in any of the 256 words. If a match operation did not result in a positive match (the $\overline{\text{MTCH}}$ signal is HIGH) and if the CAM Array is not full (the $\overline{\text{FULL}}$ signal is HIGH) the Priority Encoder will generate the lowest empty address. The 8 bit empty address is accessed by reading the Status Register.

CAM Registers - Reading and Writing

The Am99C10 has 5 programmable registers involved in data transfers. The Command and Status registers are 16 bits wide, and the Comparand, Mask and CAM registers are 48 bits wide. Figure 3. is a model of the Am99C10 registers and their interaction with each other and the CAM Array. Table 1 lists the registers and their respective data sources and destinations.

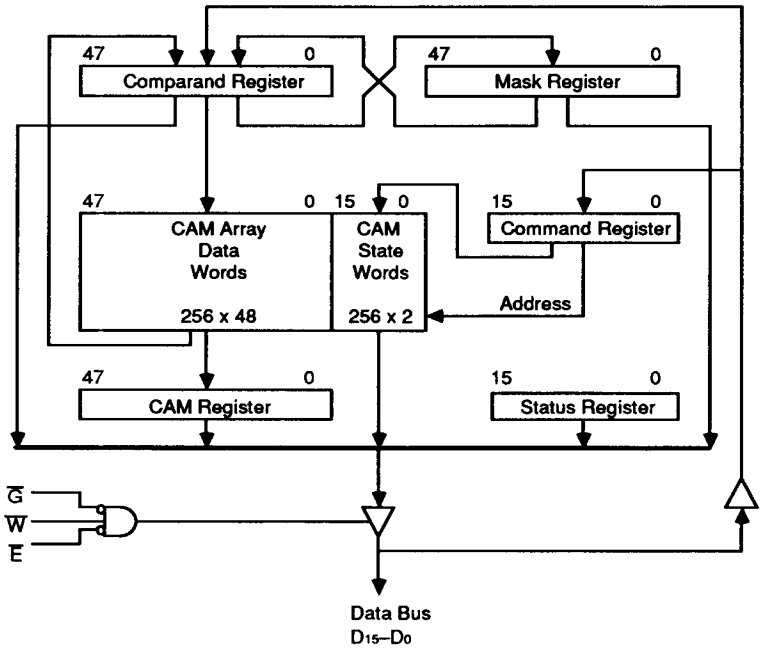


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Figure 3. CAM Register Transfer Model

Table 1. Am99C10 Registers

Register	Type	Size	Direction	Data Source	Destination
Command	Cmd	16	Input	D–Bus	–
Status	Cmd	16	Output	–	D–Bus
Comparand	Data	48	In / Out	D–Bus, CAM Array Mask Register	D–Bus, CAM Array Mask Register
Mask	Data	48	Output	Comparand Register	D–Bus, Comparand Register
CAM	Data	48	Output	CAM Array	D–Bus

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Data Bus Transfers

All data is transferred to and from the CAM over the 16-bit bidirectional Data Bus. Data transfer is controlled by a combination of 4 control signals ($\overline{E}$, D/$\overline{C}$, $\overline{W}$, and $\overline{G}$), as described in the Pin Description section.

Data is written into the Am99C10 by placing the data on the Data Bus and activating $\overline{W}$ and $\overline{E}$. When D/$\overline{C}$ is low (Command Write cycle), the input data is loaded into the Command Register. When D/$\overline{C}$ is high (Data Write cycle), the input data is loaded into the Comparand Register.

Data is read from the Am99C10 (output drivers enabled) when $\overline{G}$ and $\overline{E}$ are low and W is high. When D/$\overline{C}$ is low (Status Read cycle) the Status register is gated onto the Data Bus. When D/$\overline{C}$ is high (Data Read cycle) one of the data registers is gated onto the Data Bus. This register is selected by the contents of the Command register.

Prior to reading, a command is loaded into the Command Register to select which of the internal registers is to be read.

Data can be read from any register by loading the appropriate command into the Command register; however, data can be written only to the Comparand register. Data to be written to the Mask register or to the CAM array must first be written into the Comparand register and transferred to the Mask register or CAM array word by writing the appropriate transfer command to the Command register.

48–bit Data Transfers

Data is transferred to and from the Am99C10 in 16-bit words. Data for the 16-bit Command and Status registers are transferred in one read or write cycle. Data for the 48-bit Comparand, Mask and CAM registers are transferred to and from the chip in three cycles. Data transfer to and from each 48-bit register is done by dividing each register into three 16-bit segments. A two-bit counter, the Segment Counter is used to select which segment of a 48-bit register is to be loaded or read.

The Segment Counter is a two-bit binary counter that counts from 0 to 2 (modulo-three). It can be preset by writing a command code of "B", "C" or "D" to the Command register. In all three commands bits 10 and 11 (S0, S1) define the binary value (0,1 or 2) to be preset into the counter. Note that a value of 3 (S1,S0 = 11) in these bits will result in a value of 0 in the counter. The counter is also reset to 0 by the Initialize command, command code "0".

The Segment Counter is incremented after each data read or write cycle if the CAM is in the 48-bit mode. This allows a 48-bit register to be loaded or read in three successive cycles. The counter is clocked by the LOW-to-HIGH transition of W in case of a Data Write cycle and by the LOW-to-HIGH transition of $\overline{G}$ in case of a Data Read cycle.

When the Am99C10 is set to 48-bit mode, the user will normally execute 3 Data Write cycles or 3 Data Read cycles in sequence to transfer a 48 bit data word. At the end of such sequence the state of the Segment Counter is equal to its initial state before the data transfer began. This allows continuous 48-bit transfers without having to preset the Segment Counter between words. This is useful in the CAM's normal operating mode of checking a stream of 48-bit words for a match.

Note that reading a 16-bit State word requires only one cycle. If the CAM is in the 48-bit mode, this data read operation will increment the Segment Counter. Any subsequent cycles that use the Segment Counter have to take this into account.

16-bit Mode Data Transfers

In 16 bit mode the Segment Counter is not incremented and it points to one of the three segments of the Comparand, Mask and CAM Registers. Writing and reading the selected segment of those registers is achieved in one cycle. However, internal transfers between the registers and the CAM Array as well as the Match operation are done on all 48 bits.

CAM Array-Reading and Writing

To write a word into the CAM Array, the data is first loaded into the Comparand register and then transferred from the Comparand register to the register in the selected CAM word by executing a transfer command. The transfer command is executed by writing a command word (command code = 6 or E) into the Command register. The transfer command contains the address of the CAM word to be written.

To read a word from the CAM Array, data is transferred from the CAM array to either the Comparand or CAM registers by writing the appropriate command (command code = 7 or D, respectively) into the Command register. The transfer command contains the address of the CAM word to be read. The CAM Array word is then read from the register selected by the command.

Writing into the Skip or Empty bit in a CAM word is done directly by writing the appropriate command code (command code = 9 or A, respectively) into the Command register. The command word contains the value of the Skip or Empty bit to be written and the address of the CAM word containing the bit.

The same command codes (9 or A) which are used to set a specific Skip or Empty bit can also be used to set all Skip or Empty bits in the CAM array. If bit 11of these command words is a one, the address portion of the command is ignored and the value of the Skip or Empty bit is written into all words of the CAM array. This is useful in clearing all Skip and Empty bits.

The Skip and Empty bits of a CAM word are also cleared to zero when data is written into the CAM using command code E. This allows writing a new word of data into an empty CAM word without requiring an extra cycle to clear the Skip and Empty bits.

The Skip and Empty bits of all CAM words can be preset to the empty state by writing an Initialize command (command code = 0) to the Command register. Initialize clears all Skip bits to zero and sets all Empty bits to one, corresponding to an empty CAM condition.

To read the Skip and Empty bits of a word from the CAM Array, the State Memory is selected as the source of data driving the Data Bus by writing the appropriate command (command code = 5) into the Command register. That command contains the address of the CAM word whose state is to be read. The State word (i.e., the Skip and Empty bits of the CAM Array word) are then read directly. Reading the State word requires only one Data Read cycle.

Match Operations

Comparison of data in the Comparand against the 256 words of data in the CAM array is called a match operation. The result of a match operation is a match address which appears in the Status register and the activation of the $\overline{MTCH}$ and $\overline{FULL}$ flags. Match operations require one cycle (100 ns) for valid flags and two cycles (200 ns) before status read operations can be started.

A match operation can be initiated by writing a command into the Command register or by writing data into the Comparand register. A match operation begins after a single data write to the Comparand Register in 16-bit mode or after three data write cycles to the Comparand Register in 48-bit mode. Note that the $\overline{E}$ line must be kept low for the match time, t_{MPE} (200 ns) after the write to allow the match to occur.

If a match occurs, the $\overline{MTC}$ bit is set in the Status register and the $\overline{MTCH}$ pin is activated if it has been enabled. The address of the word that matched appears in the lower 8 bits of the Status register. If more than one match occurs, the $\overline{MUL}$ flag is set in the status register, indicating a multiple match. In this case, the match address is that of the match word with the lowest numerical address. If no match occurs, the $\overline{MTC}$ bit and $\overline{MTCH}$ flag are not set, and the address is that of the first empty word, i.e. the empty word with the lowest address.

$\overline{MTC}$ is the same flag as $\overline{MTCH}$. The match flag $\overline{MTC}$ and multiple match flag $\overline{MUL}$ cannot be disabled by the Command Write. These flags respond each time new data is written into the Comparand Register.

In 48-bit mode, the match output $\overline{MTCH}$ is disabled and held HIGH until the Segment Counter reaches zero, (S1 = L and S0 = L) even if the match output has been enabled by the Command Write operation. In the 16-bit mode, the Segment Counter state does not affect the match output $\overline{MTCH}$.

The match flag access time is measured from a low-to-high transition of $\overline{W}$ to high-to-low transition of $\overline{MTCH}$ flag.

Match and Full Flags

The Am99C10 has two output signals that indicate its status - Full, $\overline{FULL}$ and Match, $\overline{MTCH}$.

The Full signal, $\overline{FULL}$, indicates whether the CAM Array is full or not. A low level on $\overline{FULL}$ indicates that all 256 words of the CAM Array are full. A high on this output indicates that one or more words in the CAM Array are still available or that the $\overline{FULL}$ output is disabled. The $\overline{FULL}$ output can be disabled (= HIGH) under program control or when the chip is disabled (Chip Enable $\overline{E}$ is high).

The Match signal, $\overline{MTCH}$, indicates whether a match has been detected, i.e. that the masked data of the Comparand Register and one or more words in the CAM Array are matched. A high on this output indicates that a mismatch has taken place or that the match output is disabled. The $\overline{MTCH}$ output can be disabled (= HIGH) under program control or when the chip is disabled (Chip Enable $\overline{E}$ is high).

Status Register Format

The Status register shows the results of match operations and the contents of the Segment Counter. The State Register is read onto the Data Bus by executing a Status Read cycle. Since it takes time to encode a match address (t_{MPE}), the Status Read cannot immediately follow a Command Write cycle or a Data Write cycle if a valid match address is sought. A time delay of (t_{MPE}) after the last command or data write before reading the Status register will guarantee proper address encoding. A Status Read operation does not affect the state of the flags or other register contents.

The Status Register has 3 fields - the Address field (A_0 - A_7), the Segment Counter State (S0 - S1) and the Flags field ($\overline{MTC}$, $\overline{MUL}$ and $\overline{FUL}$), as shown in Figure 4.

$\overline{MTC}$

A LOW on $\overline{MTC}$ (D_{15}) indicates that at least one word in the CAM Array and the masked data of the Comparand Register are matched. A HIGH indicates that no word in the CAM Array found a match. The $\overline{MTC}$ flag is the same as the match output signal $\overline{MTCH}$ except the $\overline{MTC}$ flag cannot be disabled.

$\overline{MUL}$

A LOW on $\overline{MUL}$ (D_{14}) indicates that two or more words in the CAM Array match the masked data of the Comparand Register. It is activated during a Match operation and latched by an internal clock at the end of the Match cycle.

$\overline{FUL}$

A LOW on $\overline{FUL}$ (D_{13}) indicates that the CAM Array is full. The $\overline{FUL}$ flag is the same as the full output signal $\overline{FULL}$ except the $\overline{FUL}$ flag cannot be disabled. It is activated during a Match operation and latched by an internal clock at the end of the Match cycle.

S1, S0

The Segment Counter bits (S0 - S1) are driven by the two flip-flops that comprise the Segment Counter. These two bits (D_{10} and D_{11}) reflect the current state of the Segment Counter.

15	14	13	12	11	10	9	8	7 ... 0
$\overline{MTC}$	$\overline{MUL}$	$\overline{FUL}$	0	S1	S0	0	0	Address

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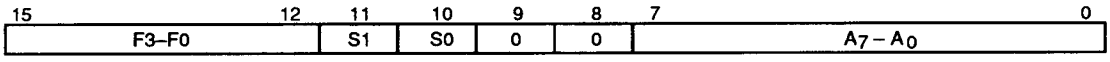
Figure 4: Status Word Bit Assignment

A_7–A_0

Lowest address of the matched word in the CAM when data in the Comparand Register and the data in the CAM are matched ($\overline{MTCH}$ = L, $\overline{MTC}$ = L and $\overline{FULL}$ = don't care). Lowest address of empty 48-bit word in the CAM when data is mismatched and the CAM is not full ($\overline{FULL}$ = H). Address is undefined when data is mismatched and CAM is full.

Command Register Format

The Am99C10 can execute a variety of commands. Each command is executed by writing the appropriate command word to the Command register. All commands are executed during the write pulse applied to the the write clock, $\overline{W}$. The format of the Command Register is shown in Figure 5, and a summary of the commands is shown in Table 2.



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F3-F0: A 4 bit Instruction Code which defines one of sixteen commands.
S0 - S1: Modifier bits for the various commands.
A_0 - A_7 An Address field which selects one of the 256 CAM Array data or State words.

Figure 5: Command Register Bit Assignment

Table 2. 99C10 Command Summary

Op Code	Operation		S1	S0	A_0-A_7	Start Match
0	Initialize		X	X	X	X
1	Flag Output control enable/disable		MTCH	FULL	X	X
2	16/48 bit Mode Select		48-bit	X	X	X
3	Comparand Reg. --> Mask Reg		X	X	X	Start
4	Mask Reg. --> Comparand Reg.		X	X	X	Start
5	SIM --> Data Bus		X	X	CAM State	X
6	Comparand Reg. --> CAM Array		X	X	CAM Data	Start
7	CAM Array --> Comparand Reg.		X	X	CAM Data	Start
8	Reserved		X	X	X	X
9	Skip Control	Per Word All Words	0 1	Skip Skip	CAM State X	Start
A	Empty control	Per Word All Words	0 1	Empty Empty	CAM State X	Start
B	Comparand Reg. --> Data Bus		Segment Counter		X	X
C	Mask Reg. --> Data Bus		Segment Counter		X	X
D	CAM Array --> CAM Reg. --> Data Bus		Segment Counter		CAM Data	X
E	Comparand Reg. -->CAM Array, clear S +E		X	X	CAM Data	Start
F	Reserved		X	X	X	X

Op Code 0
Initialization

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Not Used											

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All Skip-bits are set to "0" (LOW level) meaning–don't skip, and all Empty-bits are set to "1" (HIGH level) meaning-empty. This is equivalent to resetting the CAM Array. The $\overline{MTCH}$ and $\overline{FULL}$ outputs are enabled. The mode is set to 48-bit mode. The Mask Register and Segment Counter are reset to zero. Subsequent data writes and reads are to and from the Comparand Register.

Op Code 1
Flag Output Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	S1	S0	Not Used									

08125–020A

This command controls the enable and disable of the $\overline{FULL}$ and $\overline{MTCH}$ status output pins. The S0 and S1 fields of this command are latched into the control logic. Once loaded, they control the status output pins $\overline{FULL}$ and $\overline{MTCH}$ as follows: When S0 is 0, the $\overline{FULL}$ output is disabled and remains unconditionally HIGH. When S0 is 1, the $\overline{FULL}$ output is enabled and may be asserted when $\overline{E}$ is low. When S1 is 0, the $\overline{MTCH}$ output is disabled and remains unconditionally high. When S1 is 1, the $\overline{MTCH}$ output is enabled and may be asserted if $\overline{E}$ is low.

Op Code 2
Mode Select

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	S1	Not Used										

08125–021A

This command sets the 99C10 into the 16-bit or 48-bit mode. The S1 bit in the command is loaded into the 16/48-bit mode control register. The 16-bit mode is enabled when S1 is 0, and the 48-bit mode is enabled when S1 is 1. The Am99C10 will remain in the mode selected until another Command Write is executed with Op Code "0" or "2".

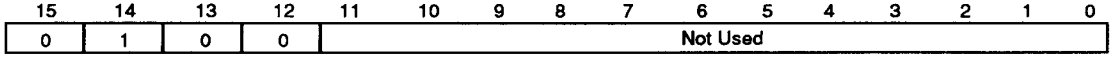
Op Code 3
Move Comparand Register to Mask Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	Not Used											

08125–022A

The 48-bit contents of the Comparand Register is loaded into the Mask Register. The Segment Counter is not affected. A Match cycle will begin automatically following this command.

Op Code 4
Move Mask Register to Comparand Register



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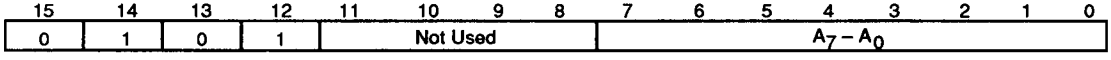
The 48-bit contents of the Mask Register is loaded into the Comparand Register. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

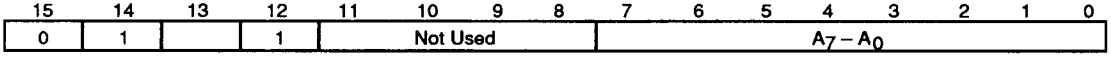
Op Code 5
Enable Output from State Memory to Data Bus



08125–024A

This command selects a State word in the CAM Array as the source of data to be read. The Skip-bit and Empty-bit appear on bits D_{14} and D_{15} of the Data Bus, all other bits of the bus are driven LOW. The Segment Counter is not changed.

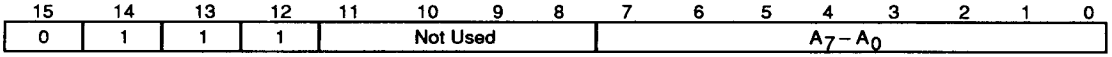
Op Code 6
Move Comparand Register to CAM Array



08125–025A

The 48-bit contents of the Comparand Register are written into the CAM Array data word. The 16/48 bit mode select setting does not affect this instruction. The Empty-bit and Skip-bit in the State Memory are not changed. The CAM Array address is specified by the Command Register address field. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

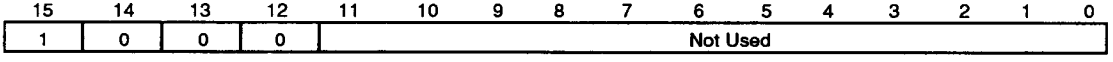
Op Code 7
Move CAM Array to Comparand Register



08125–026A

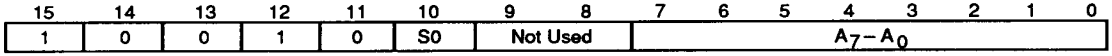
The 48-bit contents of the CAM Array data word specified by the address field are loaded into the Comparand Register. The Segment Counter is not changed. The State Memory is not changed. The 16/48 bit mode select setting does not affect this instruction. A Match cycle will begin automatically following this command.

Op Code 8
Reserved



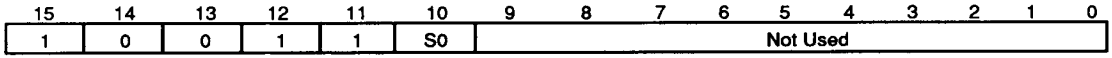
08125–027A

Op Code 9
Skip-bit Control



08125–028A

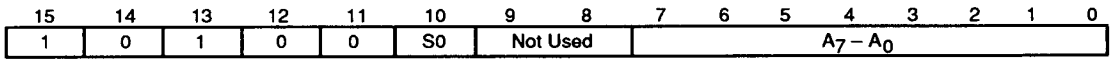
When bit 11 in the Command Register is LOW, S0 is loaded into the Skip-bit within the State word location specified by the Command Register address field. A Match cycle will begin automatically following this command.



08125–029A

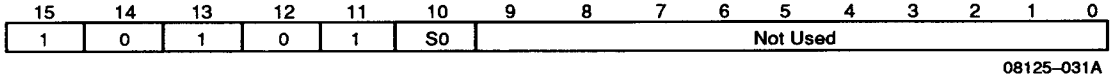
When bit 11 in the Command Register is HIGH, S0 is loaded into all skip-bit memory locations. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Op Code A
Empty-bit Control



08125–030A

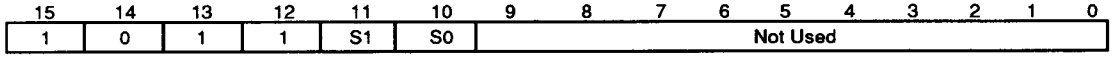
When bit 11 in the Command Register is LOW, S0 is loaded into the Empty-bit within the State word location specified by the Command Register address field. A Match cycle will begin automatically following this command.



08125–031A

When bit 11 in the Command Register is HIGH, S0 is loaded into all Empty-bit memory locations. The Segment Counter is not changed. A Match cycle will begin automatically following this command

Op Code B
Enable Output from Comparand Register to Data Bus

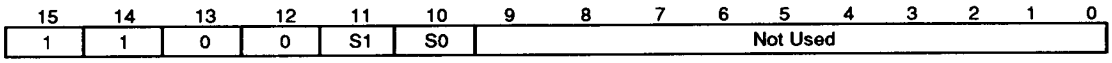


08125–032A

This command selects the Comparand Register as the source of data to be read. The S0 and S1 data in the Command Register are clocked into the Segment Counter at the end of this Command Write cycle. When S0 and S1 are 11, the Segment Counter is reset to zero. Subsequent Data Read operations result in data flowing from the Comparand Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle will automatically increment the modulo-three Segment Counter.

Op Code C

Enable Output from Mask Register to Data Bus

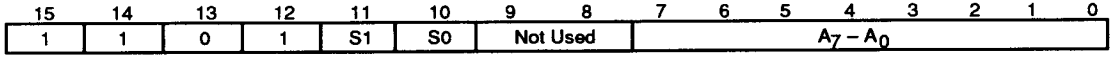


08125–033A

This command selects the Mask Register as the source of data to be read. The S0 and S1 data in the Command Register are clocked into the Segment Counter at the end of this Command Write cycle. When S0 and S1 are 11, the Segment Counter is reset to zero. Subsequent Data Read operations result in data flowing from the Mask Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle will automatically increment the modulo-three Segment Counter.

Op Code D

Move CAM to CAM Register, Enable Output from CAM Register to Data Bus

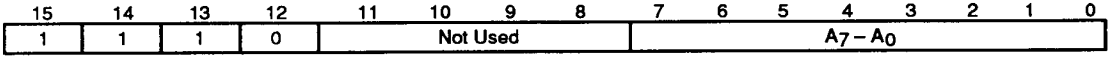


08125–034A

This command selects the CAM Register as the source of data to be read. The S0 and S1 data in the Command Register are moved to the Segment Counter. When S0 and S1 are 11, the Segment Counter is reset to zero. The CAM Array word specified by the address field is transferred to the CAM Register. Subsequent Data Read operations result in data flowing from the CAM Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle automatically increments the modulo-three Segment Counter.

Op Code E

Move Comparand Register to CAM (Set Empty-bit and Skip-bit LOW)

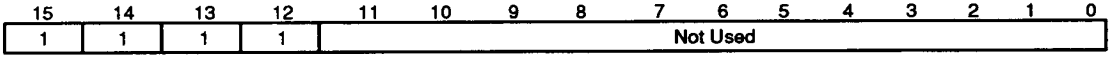


08125–035A

The 48-bit contents of the Comparand Register is written into the CAM Array data word specified by the address field. The 16/48 bit mode select setting does not affect this instruction. Both the Empty-bit and the Skip-bit in the State Memory address specified by the Command Register address field are set cleared to zero (Not Empty and Don't Skip). The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Op Code F

Reserved



08125–036A

Typical Command Sequences

The following are examples of some common sequences of commands.

Power-up Initialization

After power-up, the CAM must be initialized. This is done by executing the Initialize command. All the CAM words are reset to the empty state, and the device is set up in the 48-bit mode. Another command is needed if the16-bit mode is desired.

For 48-bit mode:

Command Write 0000 = Initialize	(16/48 mode is set automatically to 48 bit mode)

For 16-bit mode:

Command Write 0000 = Initialize	(16/48 mode is set automatically to 48 bit mode)
Command Write 2000 = Mode Select	(S1=0, Set mode to 16 bit)

Loading CAM Array with Data

After initialization, the CAM must be loaded with data in order to be used. Since all locations are initialized to the empty state, the CAM can be loaded starting from address zero. This is done by loading the Comparand register and writing a command with an op code of E, which will transfer the data to a specified CAM word and clear the Skip and Empty bits of that word.

Filling the CAM in the 48-bit mode is normally done using the following command sequence:

Data Write (D_{15} -- D_0 --> Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Command Write E0XX = Comparand Register -->CAM Array + Clear S+E
(Repeat for every CAM Array word to be loaded.)

Filling the CAM in the 16-bit mode is done using the following command sequence:

Command Write BX00 = Comparand Register -->Data Bus (Load Segment Counter)
Data Write (D_{15} -- D_0 -->Comparand Register) (segment selected by counter)
Command Write E0XX = Comparand Register -->CAM Array + Clear S+E (all 48 bits are written).

Repeat the last two steps for every CAM Array word to be loaded.
Repeat all three steps when a different 16 bit segment is to be loaded.

Load Mask Register

The mask register is loaded by writing the data into the Comparand Register and then writing a command to transfer the data from the Comparand register to the Mask register.

Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Command Write 3000 = Comparand Register -->Mask Register

48 bit Compare for Match (48-bit Mode)

To perform a match operation on new data, the data to be tested is written into the Comparand register, time is allowed for the match operation to be performed, and then the match flag and match address are read from the Status register. Note that no special command is required to start the match: it begins after the last word is loaded into the Comparand register.

Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Wait one cycle (allow time for Match operation - 2 cycles if Status read)
Check $\overline{\text{MTCH}}$ output pin, or Status Read, check bits 15, 14 and 13 ($\overline{\text{MTC}}$, $\overline{\text{MUL}}$, $\overline{\text{FUL}}$)

Check for Multiple Matches

Typical match operations yield a single match. Some applications, however may yield multiple matches. In this case, the addresses of each match may be read by successively reading the current lowest address, setting its Skip bit, and reading the next lowest address, etc., until no matches are left.

Status Read, bit 15 ($\overline{\text{MTC}}$) = 0, bit 14 ($\overline{\text{MUL}}$) = 0
Status bits 7-0 contain the address of the lowest word in the CAM that found a match.
Read and save the match address, use it to form the next command

Command Write 94XX = Skip Control - F(9), set bit 11(S1) = 0, set bit 10 (S0) = 1(Skip),
Set the Skip bit: Command bits 7-0 to the lowest matching word address.

Wait two cycles for the next Match operation to complete and the Status register to settle
Status Read
Check $\overline{\text{MTC}}$ for match, save the address if $\overline{\text{MTC}}$ =0
Status bits 7-0 contain the address of the lowest word in the CAM that found a match.
Read and save the match address, use it to form the next command

Repeat the last three steps until there are no more matches

Finding and Loading an Empty Location

A CAM word may be empty since initialization or it can be declared empty by setting its Empty bit. Data is added to the CAM by finding an empty location and writing into it. This is done by loading the data to be written into the Comparand register and checking for a match. If the data is not already stored in the CAM, the match operation will respond with the address of the lowest empty word. (If a match was found, a copy of the data already exists in the CAM.) The address of the empty word is used to write the new data into the empty word.

Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Wait two cycles (allow time for Match operation and priority encode)
Status Read, check bits 15 ($\overline{\text{MTC}}$) should be 1, and 13 ($\overline{\text{FUL}}$) should be 1,
Bits 0-7 contain the address of the lowest empty word in the CAM.
Command Write E0XX = Comparand Register -->CAM Array + Flags,
Bits 0-7 should have the address of the empty word from the Status Read.

Reading Data

To read the contents of a word in the CAM Array

Command Write D0XX = CAM Array -->CAM Register -->Data Bus,
Bits 0-7 indicate the address of the word to be read.

Data Read - (CAM Register (15-0) -->D_{15} - D_0)
Data Read - (CAM Register (31-16) -->D_{15} - D_0)
Data Read - (CAM Register (47-32) -->D_{15} - D_0)

Example of a Command Sequence

Table 3 shows the control signals, data bus contents and Segment Counter contents for a typical command sequence. The sequence consists of initialization, filling the CAM Array, and loading the Mask Register. A data pattern is then loaded into the Comparand Register, a match is executed and the sequence terminates with the reading of the Status Register.

Table 3. Command Sequence Example

Cycle Type	Instruction	$\overline{E}$	D/$\overline{C}$	$\overline{W}$	$\overline{G}$	Data Bus (Hex)	Segment Counter Before	Segment Counter After	Operation
Command Write	Initialize	L	L	C	H	0XXX	XX	00	Set default conditions
Data Write	—	L	H	C	H	3210	00	01	D_{15}–D_0 —> Comparand Reg (15–0)
Data Write	—	L	H	C	H	7654	01	10	D_{15}–D_0 —> Comparand Reg (31–16)
Data Write	—	L	H	C	H	BA98	10	00	D_{15}–D_0 —> Comparand Reg (47–32)
Command Write	Comparand Reg. —> CAM	L	L	C	H	E000	00	00	"BA9876543210" into CAM word 0
⋮	⋮					⋮		⋮	⋮
Data Write	—	L	H	C	H	1111	00	01	D_{15}–D_0 —> Comparand Reg (15–0)
Data Write	—	L	H	C	H	2222	01	10	D_{15}–D_0 —> Comparand Reg (31–16)
Data Write	—	L	H	C	H	4444	10	00	D_{15}–D_0 —> Comparand Reg (47–32)
Command Write	Comparand Reg. —> CAM	L	L	C	H	E0FF	00	00	"444422221111" into CAM word 255
Data Write	—	L	H	C	H	00FF	00	01	D_{15}–D_0 —> Comparand Reg (15–0)
Data Write	—	L	H	C	H	0000	01	10	D_{15}–D_0 —> Comparand Reg (31–16)
Data Write	—	L	H	C	H	FF00	10	00	D_{15}–D_0 —> Comparand Reg (47–32)
Command Write	Comparand Reg. —> Mask Reg.	L	L	C	H	3000	00	00	"FF00000000FF" into Mask Register
Data Write	—	L	H	C	H	7654	00	01	D_{15}–D_0 —> Comparand Reg (15–0)
Data Write	—	L	H	C	H	BA98	01	10	D_{15}–D_0 —> Comparand Reg (31–16)
Data Write	—	L	H	C	H	FEDC	10	00	D_{15}–D_0 —> Comparand Reg (47–32)
Wait (Match)	—	L	X	H	H	XXXX	00	00	Compare "XXDCBA9876XX" against CAM
Wait (Encode)	—	L	X	H	H	XXXX		00	Encode match address —> Status reg
Status Read	—	L	L	H	C	Status	00	00	Check Flags

L = LOW
H = HIGH
C = LOW going pulse

08125–037A

CAM Applications

Content Addressable Memory (CAM) devices have many potential applications. The availability of high density CAM devices such as the Am99C010 will allow many applications to be developed which were not practical in the past because of lack of CAM devices. Some of these application areas are:

Local Area Network (LAN) bridge address filtering
Local Area Network (LAN) ring message insertion and removal

Data base machine support - Search and sort accelerators
Pattern recognition - String search engines, etc.
Image processing and machine vision - Pattern recognition, Image registration, etc.
Neural net simulation
AI language support - (LISP, etc.) garbage collection support, PROLOG accelerators, etc.

Local Area Network Bridge Address Filtering

Bridges between high speed Local Area Networks (LAN) provide a good example of CAM use. A LAN bridge provides transparent communication between two networks. An example is a bridge between a 100MBit/second FDDI network and an Ethernet network. A block diagram of such a network system is shown in Figure 6, and a block diagram of the bridge is shown in Figure 7.

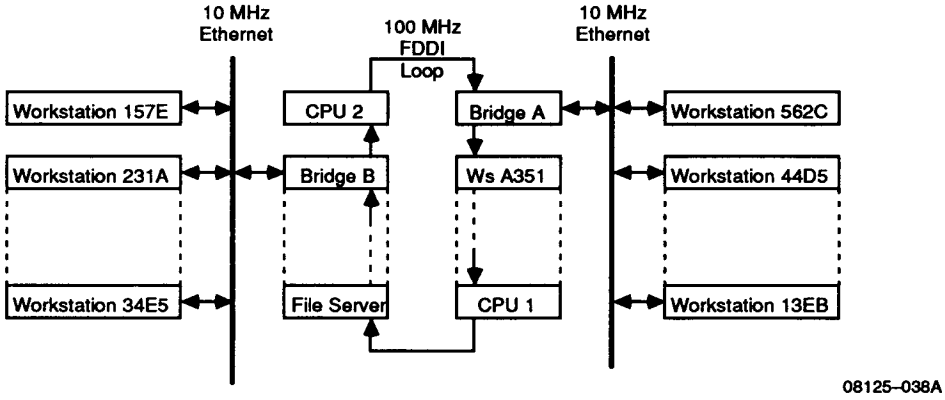


Figure 6: FDDI-Ethernet Network System

The function of the FDDI-Ethernet bridge is to pass messages between the two networks in order to allow the various workstations to communicate. Messages are sent according to unique 48-bit addresses assigned to each workstation. Each message contains the source address and the destination address. The notations shown in the workstation boxes in Figure 6 are assumed to be examples of these addresses: e.g. 157E, 231A, etc.. F

Let us assume that workstation 562C sends a message to workstation 231A. In order for this to occur, the first FDDI-Ethernet bridge must pass along the address to the FDDI loop. The second bridge must recognize that the message is for one of the workstations on its Ethernet LAN and pass it along to workstation 231A.

The problem for the FDDI-Ethernet bridge is to recognize-in time-that the message is for a station on its Ethernet LAN and no other. There could be 4000 workstations on the Ethernet LAN. This means that the bridge must check the message destination address against 4000 addresses in order to determine whether to accept the message and pass it on to the Ethernet.

Address identification must be done quickly. The message acceptance decision must be made before the arrival of the next message, i.e. within the minimum message time. If the minimum message length is 9 bytes on a 100 mbit/sec FDDI network, the decision must be made in 720 ns, including 480 ns to acquire the address. The Am99C10 can do the job in 480+100=580 ns. At these speeds, the Am99C10 is not only effective, it is the only practical, cost effective approach.

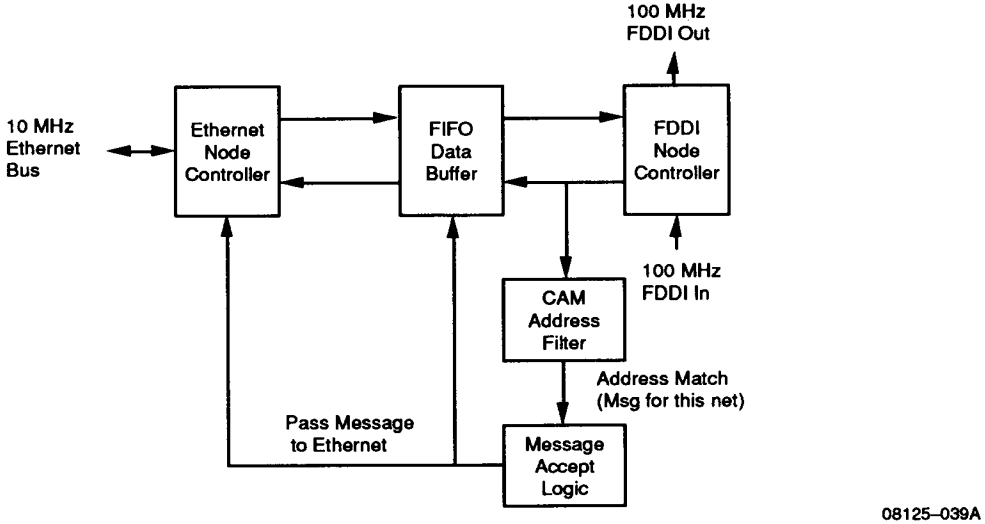


Figure 7: FDDI-Ethernet Bridge Block Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Voltage on Any Pin with Respect to GND	–0.5 to + 7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to + 85°C
Supply Voltage (V_{CC})	+4.75 to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS are valid over the operating range unless otherwise specified. All values are guaranteed maximum type limits.

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{OH}	Output High current	V_{OH} = 2.4 V, V_{CC} = 4.5 V	–1.6		mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V	+2.4		mA
V_{IH}	Input High Voltage		2.2	V_{CC} + .5	V
V_{IL}	Input LOW Voltage	(Note 3)	–0.5	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		2.0	µA
I_{OZ}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{E} \ge V_{IH}$ or $\overline{G} \ge V_{IH}$		2.0	µA
I_{CC1}	Static Operating Supply Current	$\overline{E} \ge V_{IL}$		70	mA
I_{CC2}	Dynamic Operating Supply Current, 48-bit mode	Cycle = 48-bit Data Write $\overline{E} \ge V_{IL}$, f = 1/twc		110	mA
I_{CC3}	Dynamic Operating Current, 16-bit mode	Cycle = 16-bit Data Write $\overline{E} \ge V_{IL}$, f = 1/twc		130	mA
I_{SB1}	Standby Current TTL Input Levels	$\overline{E} \ge V_{IH}$ V_{CC} = Max		10	mA
I_{SB2}	Standby Current CMOS Input Levels	$\overline{E} \ge (V_{CC} - 0.2V)$; $V_{IN} \le 0.2V$ or $V_{IN} \ge (V_{CC} - 0.2)$		10	mA

AC CHARACTERISTICS

Parameter Symbol	Parameter Description	Min.	Max.	Unit	Note
Common Parameters					
t_{DCS}	D/C, E setup before read or write	0		ns	
t_{DCH}	D/C, E hold time after read or write	5		ns	
Read Cycle Parameters					
t_{RC}	Read cycle time	100		ns	
t_{RP}	Read cycle pulse width	75			8
t_{RR}	Read recovery time	25		ns	
t_{OLZ}	Output enable time to low Z	10		ns	4,8
t_{OHZ}	Output disable time to high Z	5	30	ns	4,6
t_{RA}	Read access time		65	ns	
t_{FA}	Flag enable time		30	ns	4
t_{FH}	Flag disable time		30	ns	4
Write Cycle Parameters					
t_{WC}	Write cycle time	100		ns	
t_{WP}	Write pulse width	75			8
t_{WR}	Write recovery time	25		ns	7
t_{DS}	Data setup time before write	0		ns	
t_{DH}	Data hold time after write	5		ns	
t_{MAF}	Match time to flags after write		100	ns	7
t_{MPE}	Match priority encode time after write		200	ns	7
t_{MA}	Match access time to Status after write		$t_{MPE} + t_{RA}$		

Notes:

1. Absolute maximum ratings are intended for user guidelines and are not tested.
2. Ambient temperature is defined as the instant-on case temperature.
3. Undershoot to –3.0 V for 10 ns maximum between the 50 amplitude points is permissible.
4. Parameter guaranteed by design and characterization data but not 100 tested.
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance (see test load A in switching test circuits) unless otherwise noted. Output timing reference is 1.5 V.
6. Test load B. Disable time is measured as the time to a +500 mV change from prior output level.
7. $\overline{E}$ must be low and $\overline{W}$ must be high for t_{MAF} during the match cycle following command or data write for the internal circuitry to generate the match.
8. $\overline{W}$ and $\overline{G}$ may not overlap: i.e., may not both be low at the same time (while $\overline{E}$ is low).

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
CI	Input Capacitance	F = 1 MHz, V_{IN} = 0 V		10	pF
CI/O	Input/Output Capacitance	F = 1 MHz, $V_{I/O}$ = 0 V		10	pF

Notes:

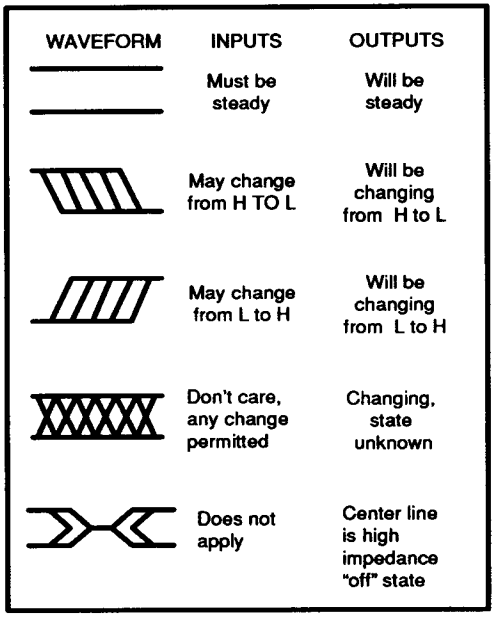
1. These parameters are guaranteed by characterization but not tested. Measurements performed at T_A = +25°C.

Data Transfer Control Signals

OPERATION MODE	CONTROL SIGNALS				DATA BUS	SUPPLY CURRENT
	$\overline{E}$	D/$\overline{C}$	$\overline{W}$	$\overline{G}$		
Command Write	L	L	L	H	Data In	I_{CC1}, I_{CC2}
Data Write	L	H	L	H	Data In	I_{CC1}, I_{CC2}, I_{CC3}
Status Read	L	L	H	L	Data Out	I_{CC1}, I_{CC2}
Data Read	L	H	H	L	Data Out	I_{CC1}, I_{CC2}
Output Disabled	L	X	H	H	Hi – Z	I_{CC1}
Standby	H	X	X	X	Hi – Z	I_{SB1}, I_{SB2}
Invalid	L	X	L	L	Hi – Z	—

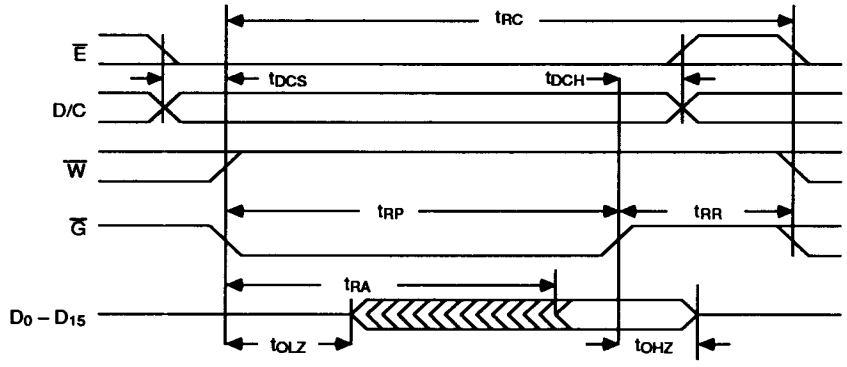
08125–003A

SWITCHING WAVEFORMS
Key To Switching Waveforms



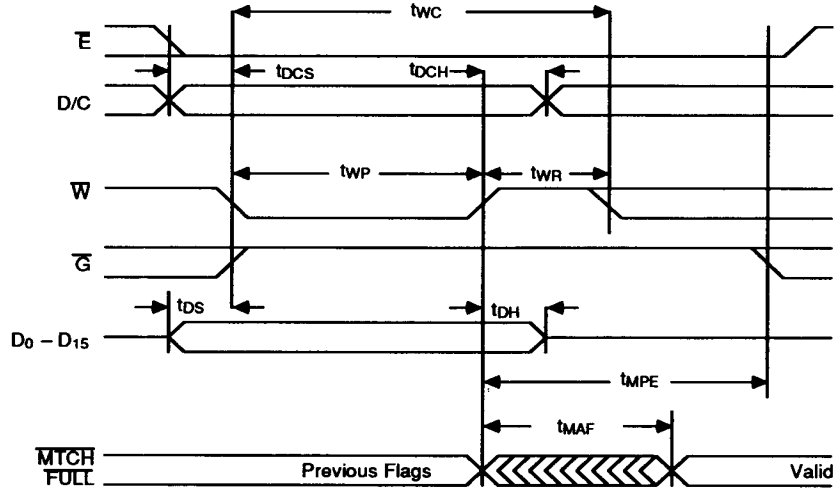
KS000010

Read Timing Diagram



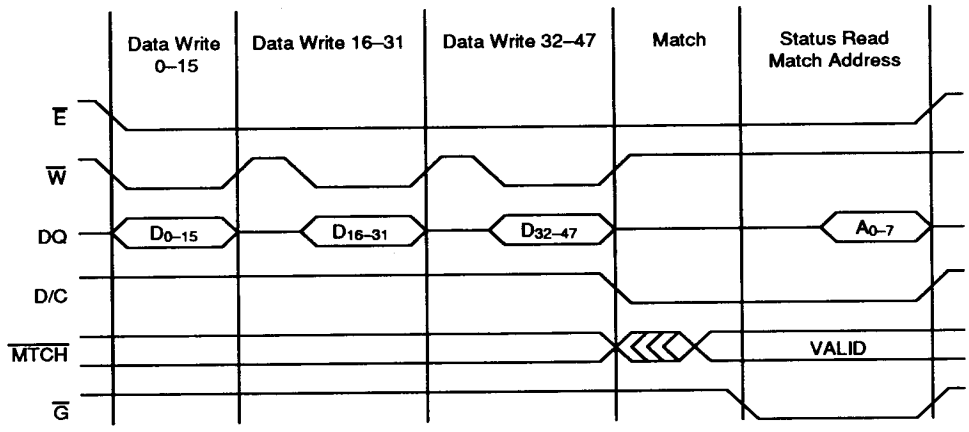
08125–008A

Write Timing Diagram



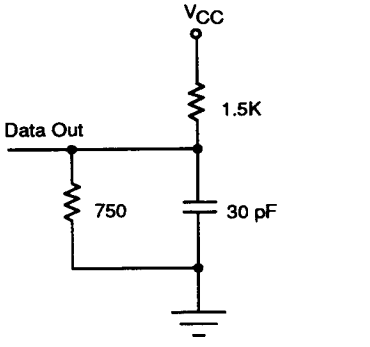
08125–009A

Match Timing Diagram (Reference)



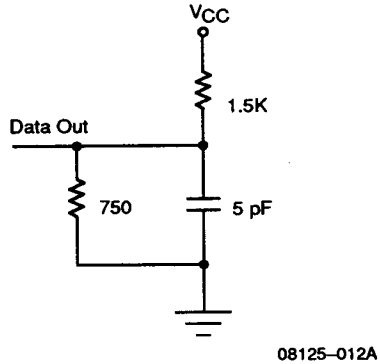
08125–010A

SWITCHING TEST CIRCUITS



08125–011A

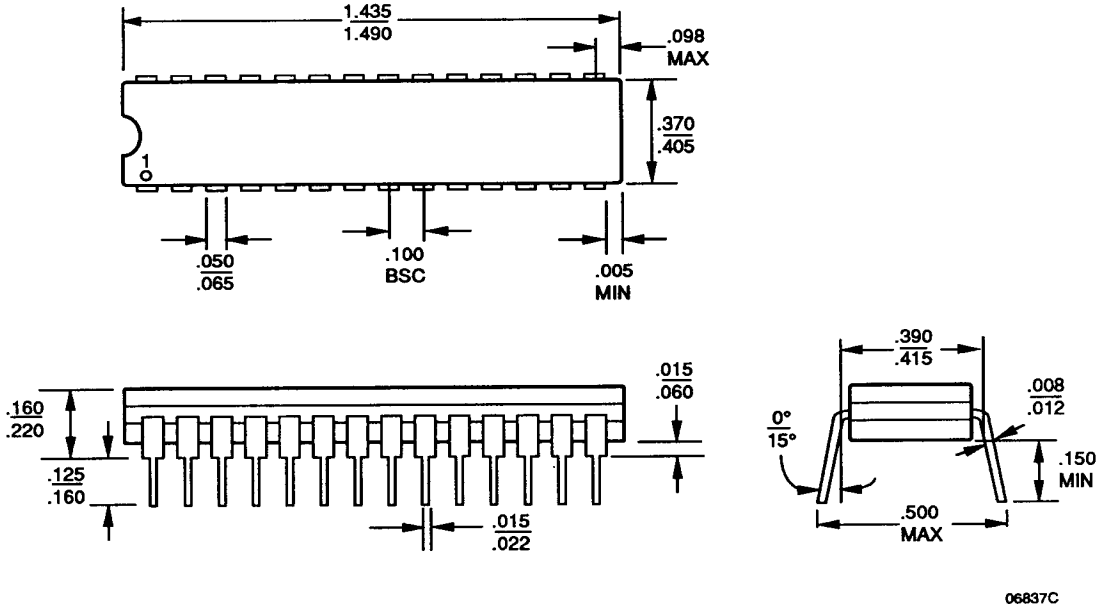
Test Load A



08125–012A

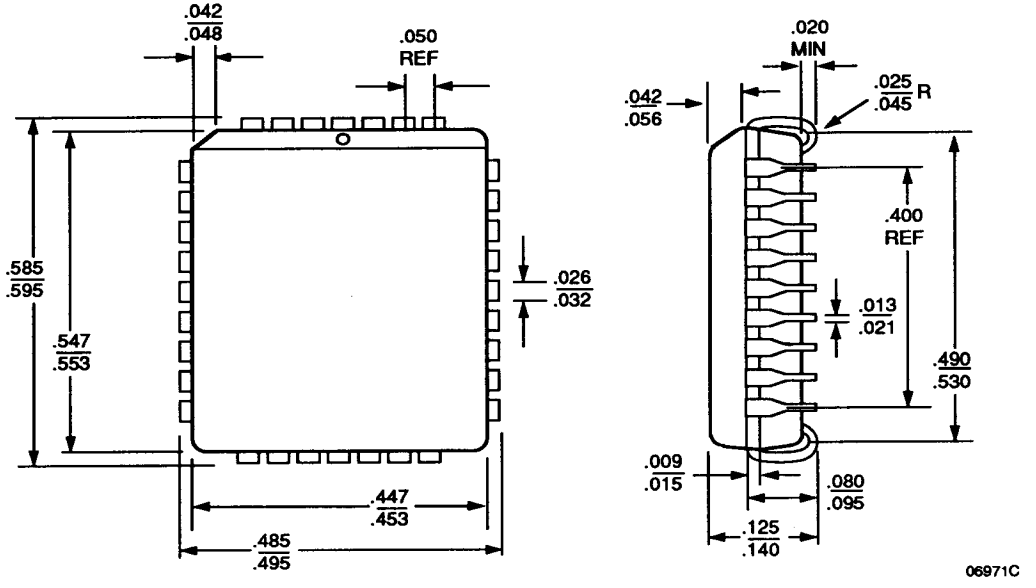
Test Load B

PHYSICAL DIMENSIONS
CD 4028



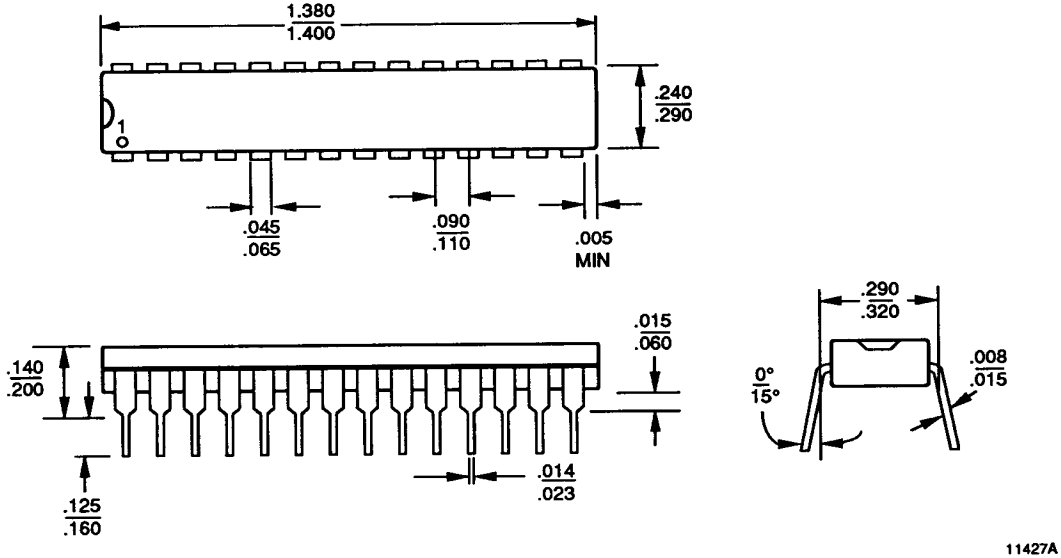
06837C

PL 032



06971C

PHYSICAL DIMENSIONS, (Continued)
PD 3028



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