Electrical Specifications

15

This chapter describes the electrical specifications for the V_R4300 processor.

15.1 LVCMOS

The V_R4300 meets and exceeds the JEDEC standard for low-voltage CMOS-compatible VLSI digital circuits (LVCMOS).

15.2 DC Characteristics

Maximum Ratings

NOTE: Operation beyond the limits set forth in Table 15-1 may impair the useful life of the device.)

Table 15-1 Maximum Ratings

Parameter	Symbol	Test Conditions	Minimum	Maximum	Units
Supply Voltage	VCC		3.0	3.6	V
Input Voltage	VIN		-.5[1]	VCC + 0.5	V
Storage Temperature	TST		-65	+150	C
Operating Temperature	TC	Case temperature	0	+85	C

Note: Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

(1) VIN Min. = -3.0V for pulse width less than 15ns.

Operating Parameters

Table 15-2 Operating Parameters

Parameter	Symbol	Conditions	62.5 MHz		Units
			Minimum	Maximum	
Output HIGH Voltage	VOH	VCC = Min. IOH=-4ma	2.4		V
Clock Output HIGH Voltage[3]	VOHC	VCC = Min. IOH=-4ma	2.7		V
Output LOW Voltage	VOL	VCC = Min. IOL=4ma		.4	V
Input HIGH Voltage[2]	VIH		2	VCC+.5	V
Input LOW Voltage[1,2]	VIL		-.5(1)	.8	V
MasterClock Input HIGH Voltage	VIHC		0.8 VCC	VCC+.5	V
MasterClock Input LOW Voltage	VILC		-.5(1)	0.2 VCC	V
Input Capacitance	CIn			10	pF
Output Capacitance	COut			10	pF
Operating Current	ICC	VCC = 3.0V, TC=0C		0.67	A
Input Leakage	ILeak			10	µA
Input/Output Leakage	IOLeak			20	µA

Note:

(1) VIL Min. = -3.0V for pulse width less than 15 ns.

(2) Except for MasterClock input

(3) Applies to TClock output

15.3 AC Characteristics

All output timings assume a 50 pf capacitive load. Output timings should be derated where appropriate, as listed in Table 15-3.

MasterClock and Clock Parameters

Table 15-3 MasterClock and Clock Parameters

Parameter	Symbol	Test Conditions	62.5 MHz		Units
			Minimum	Maximum	
MasterClock High	t_{MCHigh}	Transition ≤ 5ns	4		ns
MasterClock Low	t_{MCLow}	Transition ≤ 5ns	4		ns
MasterClock Freq[1]			20	62.5	MHz
MasterClock Period	t_{MCP}		16	50	ns
Clock Jitter	$t_{MCJitter}$			+/-500	ps
MasterClock Rise Time	t_{MCRise}			4	ns
MasterClock Fall Time	t_{MCFall}			4	ns
JTAG Clock Period	$t_{JTAGCKP}$		$4*t_{MCP}$		ns

Note:
(1) Operation of V_R4300 is only guaranteed with the Phase Lock Loop enabled.

System Interface Parameters

Table 15-4 System Interface Parameters

Parameter	Symbol	62.5 MHz		Units
		Minimum	Maximum	
Data Output [1,2,3]	t_{DO}	2	8	ns
Data Setup [3]	t_{DS}	3.5		ns
Data Hold [3]	t_{DH}	1.5		ns
Clock Rise Time[4]	t_{CORise}		4	ns
Clock Fall Time[4]	t_{COFall}		4	ns
Clock High Time[4]	t_{COHigh}	4		ns
Clock Low Time[4]	t_{COLow}	4		ns

Note:

(1) Timings are measured from 1.5V of the SClock to 1.5V of signal.

(2) Capacitive load for all output timings besides Status is 50pf.

(3) Data Output, Data Setup and Data Hold apply to all logic signals driven out of o driven into the V_R4300 on the system interface. Clocks are specified separately.

(4) TCLock.

Capacitive Load Deration

Table 15-5 Capacitive Load Deration

Parameter	Symbol	62.5 MHz		Units
		Minimum	Maximum	
Load Derate	CLD		2	ns/25pF

Packaging

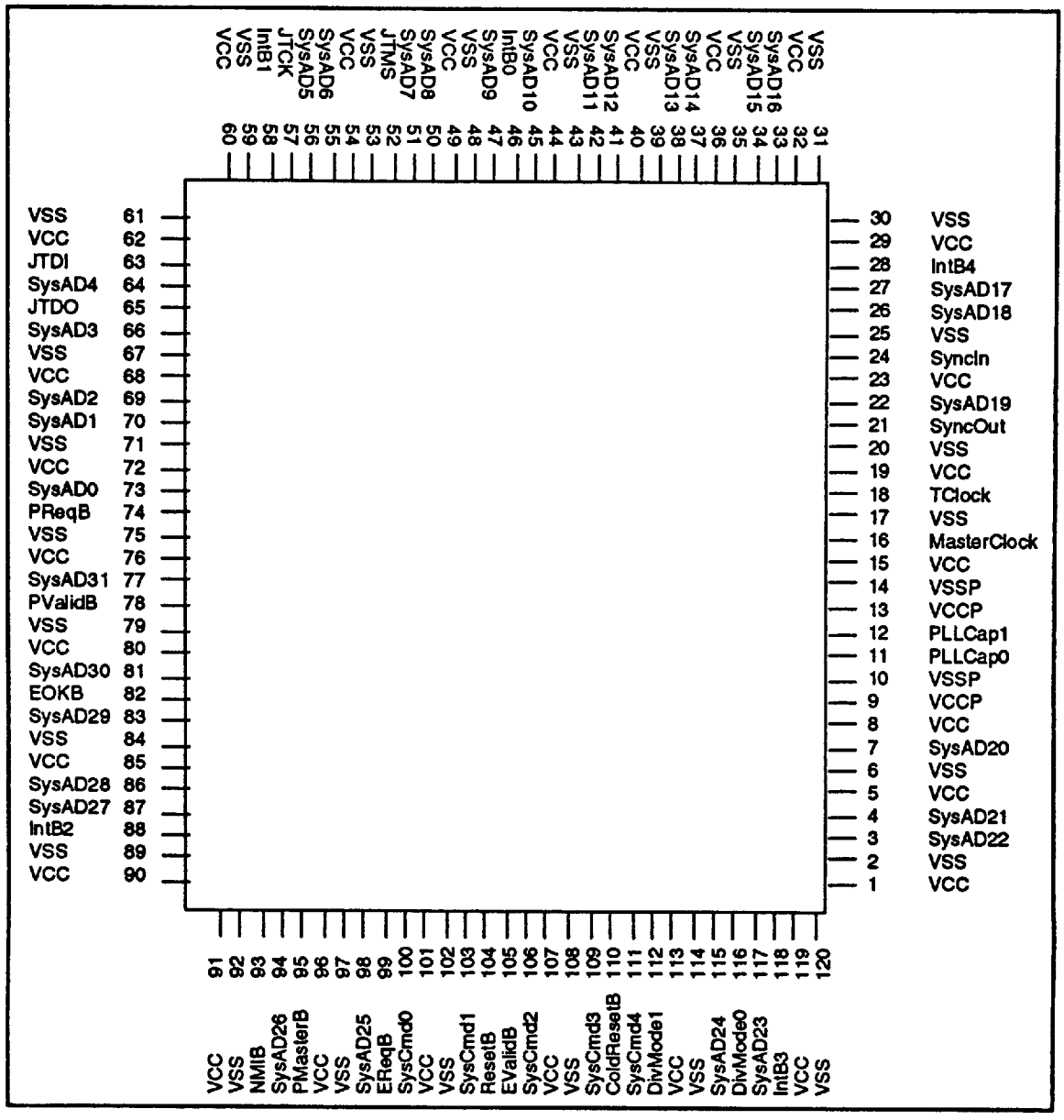
16

This chapter describes the packaging for the V_R4300 processor. Signals with a "B" suffix, such as ColdResetB, are low active. The "B" is synonymous with the asterisk, "*", used elsewhere in this manual.

120-pin PQFP Pin-out

VCC	31	VSS	61	VSS	91	VCC
VSS	32	VCC	62	VCC	92	VSS
SysAD22	33	SysAD16	63	JTDI	93	NMIB
SysAD21	34	SysAD15	64	SysAD4	94	SysAD26
VCC	35	VSS	65	JTDO	95	PMasterB
VSS	36	VCC	66	SysAD3	96	VCC
SysAD20	37	SysAD14	67	VSS	97	VSS
VCC	38	SysAD13	68	VCC	98	SysAD25
VCCP	39	VSS	69	SysAD2	99	EReqB
VSSP	40	VCC	70	SysAD1	100	SysCmd0
PLLCAP0	41	SysAD12	71	VSS	101	VCC
PLLCAP1	42	SysAD11	72	VCC	102	VSS
VCCP	43	VSS	73	SysAD0	103	SysCmd1
VSSP	44	VCC	74	PReqB	104	ResetB
VCC	45	SysAD10	75	VSS	105	EValidB
MasterClock	46	IntB0	76	VCC	106	SysCmd2
VSS	47	SysAD9	77	SysAD31	107	VCC
TClock	48	VSS	78	PValidB	108	VSS
VCC	49	VCC	79	VSS	109	SysCmd3
VSS	50	SysAD8	80	VCC	110	ColdResetB
SyncOut	51	SysAD7	81	SysAD30	111	SysCmd4
SysAD19	52	JTMS	82	EOKB	112	DivMode1
VCC	53	VSS	83	SysAD29	113	VCC
SyncIn	54	VCC	84	VSS	114	VSS
VSS	55	SysAD6	85	VCC	115	SysAD24
SysAD18	56	SysAD5	86	SysAD28	116	DivMode0
SysAD17	57	JTCK	87	SysAD27	117	SysAD23

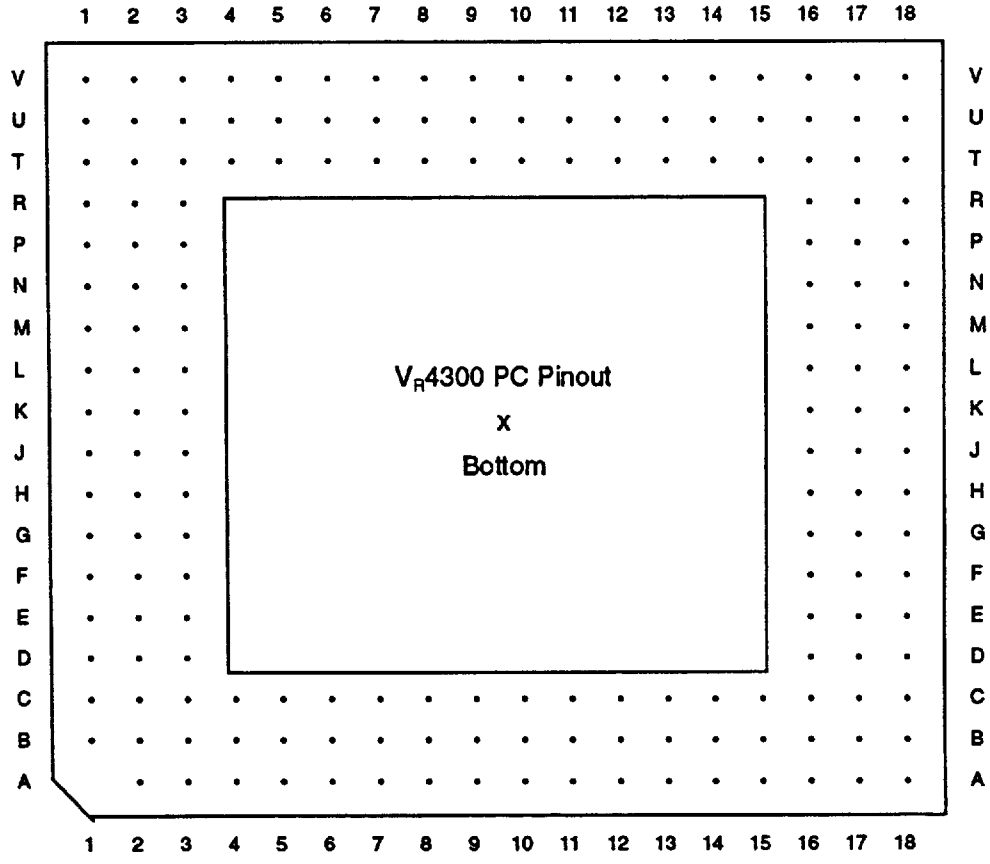
120 Pin PQFP Physical Pin Location



179-pin PGA Pin-out

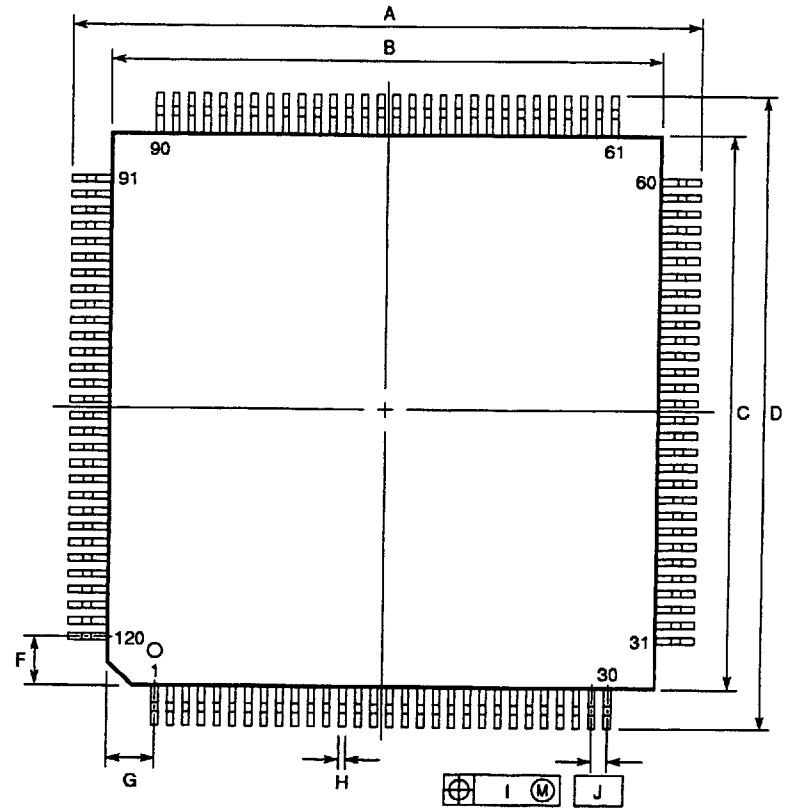
A1	No pin	C10	SysAD9	K1	VCC	T10	SysCmd2
A2	VCC	C11	NC	K2	SysAD31	T11	ColdResetB
A3	VSS	C12	SysAD11	K3	NC	T12	DivMode1
A4	VCC	C13	SysAD13	K16	VSSP	T13	NC
A5	JTCK	C14	SysAD16	K17	VCCP	T14	DivMode0
A6	VSS	C15	NC	K18	VSS	T15	IntB3
A7	VCC	C16	NC	L1	VSS	T16	NC
A8	VSS	C17	NC	L2	NC	T17	NC
A9	VCC	C18	VSS	L3	PValidB	T18	VCC
A10	VSS	D1	VSS	L16	SysAD20	U1	VCC
A11	VCC	D2	JTDI	L17	TestModeB	U2	NC
A12	VSS	D3	NC	L18	VCC	U3	NC
A13	VCC	D16	NC	M1	VCC	U4	NC
A14	VSS	D17	NC	M2	SysAD30	U5	PMasterB
A15	NC	D18	VCC	M3	EOKB	U6	NC
A16	VCC	E1	NC	M16	SysAD21	U7	EReqB
A17	VSS	E2	JTDO	M17	ByPassPLLB	U8	NC
A18	VSS	E3	SysAD4	M18	VSS	U9	EValidB
B1	VSS	E16	NC	N1	VSS	U10	NC
B2	NC	E17	NC	N2	NC	U11	SysCmd3
B3	NC	E18	SysAD17	N3	NC	U12	NC
B4	NC	F1	VCC	N16	SysAD22	U13	SysCmd4
B5	NC	F2	NC	N17	NC	U14	SysAD24
B6	SysAD6	F3	SysAD3	N18	VCC	U15	
B7	NC	F16	IntB4	P1	SysAD29	U16	NC
B8	JTMS	F17	SysAD18	P2	SysAD28	U17	NC
B9	SysAD8	F18	VSS	P3	SysAD27	U18	VSS
B10	IntB0	G1	VSS	P16	NC	V1	VSS
B11	SysAD10	G2	SysAD1	P17	NC	V2	VSS
B12	SysAD12	G3	SysAD2	P18	VSS	V3	VCC
B13	SysAD14	G16	SyncIn	R1	VCC	V4	VSS
B14	SysAD15	G17	NC	R2	IntB2	V5	SysAD25
B15	NC	G18	NC	R3	NC	V6	VCC
B16	ResetB	H1	VCC	R16	NC	V7	VSS
B17	NC	H2	SysAD0	R17	NC	V8	VCC
B18	VCC	H3	NC	R18	VSS	V9	VSS
C1	VCC	H16	SysAD19	T1	VSS	V10	VCC
C2	NC	H17	SyncOut	T2	NC	V11	VSS
C3	NC	H18	VSS	T3	NC	V12	VCC
C4	NC	J1	VSS	T4	NC	V13	VSS
C5	NC	J2	NC	T5	NMIB	V14	NC
C6	IntB1	J3	PReqB	T6	SysAD26	V15	SysAD23
C7	SysAD5	J16	TClock	T7	SysCmd0	V16	VSS
C8	NC	J17	MasterClock	T8	SysCmd1	V17	VCC
C9	SysAD7	J18	VCC	T9	NC	V18	VSS

179-Pin PGA Physical Pin Location

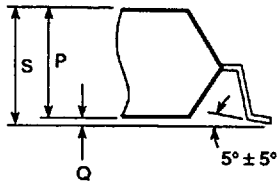


120-Pin Plastic QFP (Quad Flat Package)

Item	Millimeters	Inches
A	32.0 ±0.3	1.260 ±.012
B	28.0 ±0.2	1.102 $^{+.009}_{-.008}$
C	28.0 ±0.2	1.102 $^{+.009}_{-.008}$
D	32.0 ±0.3	1.260 ±.012
F	2.4	.094
G	2.4	.094
H	0.35 ±0.10	.014 $^{+.004}_{-.005}$
I	0.15	.006
J	0.8 (TP)	.031 (TP)
K	2.0 ±0.2	.079 $^{+.009}_{-.008}$
L	0.8 ±0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.10	.004
P	3.4	.134
Q	0.1 ±0.1	.004 ±.004
S	3.5 max	.138 max



Enlarged detail of lead end



P120GD-80-LBB,MBB

95CL-0585B (4/95)