OKI Semiconductor 1998.6

MS52C1162A Preliminary

65,536-Word X 16-Bit or 131,072-Word X 8-Bit STATIC RAM +
1,048,576-Word X 16-Bit or 2,097,152-Word X 8-Bit One Time PROM

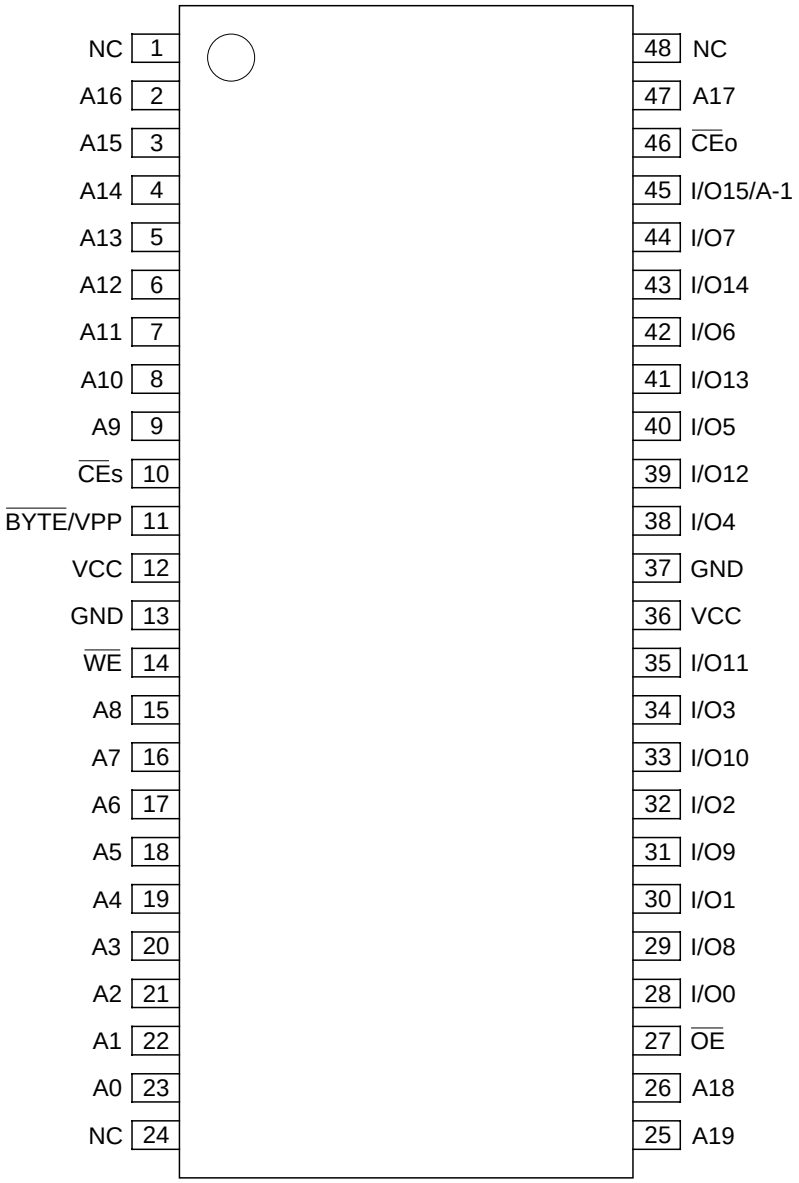
DESCRIPTION

The MS52C1162A is a 65,536 -word by 16 -bit / 131,072-word by 8-bit electrically switchable 1Mb static RAM and 1,048,576-word by 16-bit / 2,097,152-word by 8-bit electrically switchable 16Mb One Time PROM featuring 2.7V to 3.6V power supply operation and direct LVTTL input / output compatibility. Since the circuitry is completely static,external clocks are unnecessary, making this device very easy to use.
The MS52C1162A is packaged in 48-pin plastic TSOP and 48-pin FBGA (9mmx13mm) ,suited for use in handy terminal and other application which required small space.

FEATURES

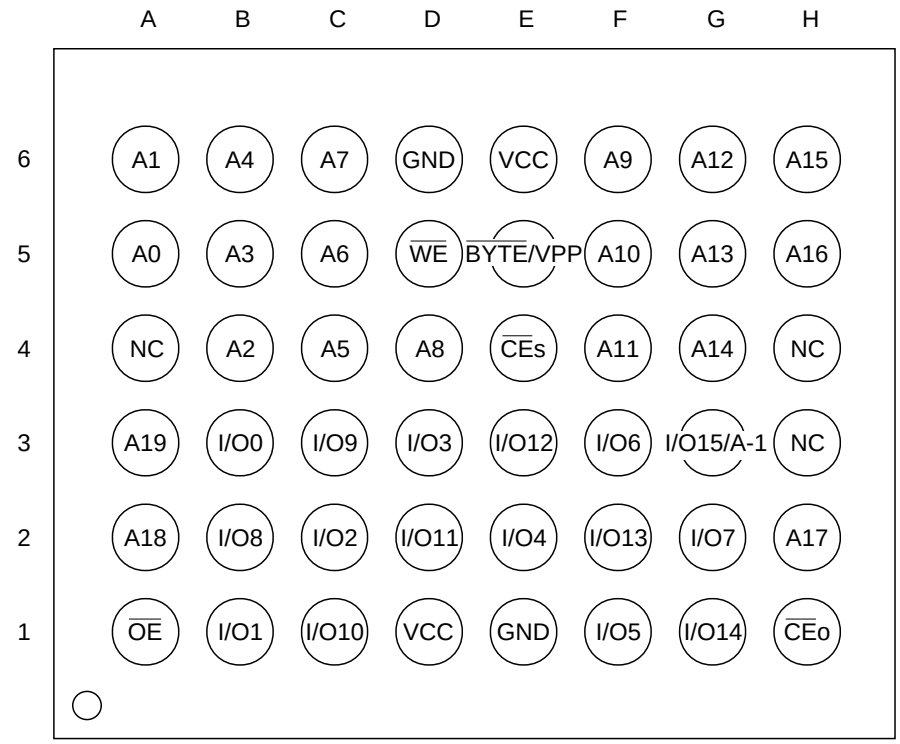
- 65,536-word x 16-bit / 131,072-word x 8-bit configuration SRAM and 1,048,576-word x 16-bit / 2,097,152-word x 8-bit configuration OTP
- Power supply voltage : 2.7 to 3.6V
- Fully static operation
- Operating temperature range : Ta= -20 to 70°C
- Access time : 100nS MAX (Vcc=2.7V)
  80nS MAX (Vcc=3.0V)
- Common address inputs and data inputs / outputs for SRAM and OTP
- Input / Output LVTTL compatible
- 3-state output
- Data retention available at power supply voltage 1.5V for SRAM
- Package options :
  48-pin plastic TSOP (Type II) (TSOP48-P-550-0.8) (Product : MS52C1162ATA)
  48-pin plastic FBGA (FBGA48-P-0913-0.8) (Product : MS52C1162ALA)

PIN CONFIGURATION (TOP VIEW)



48-pin TSOP (II)

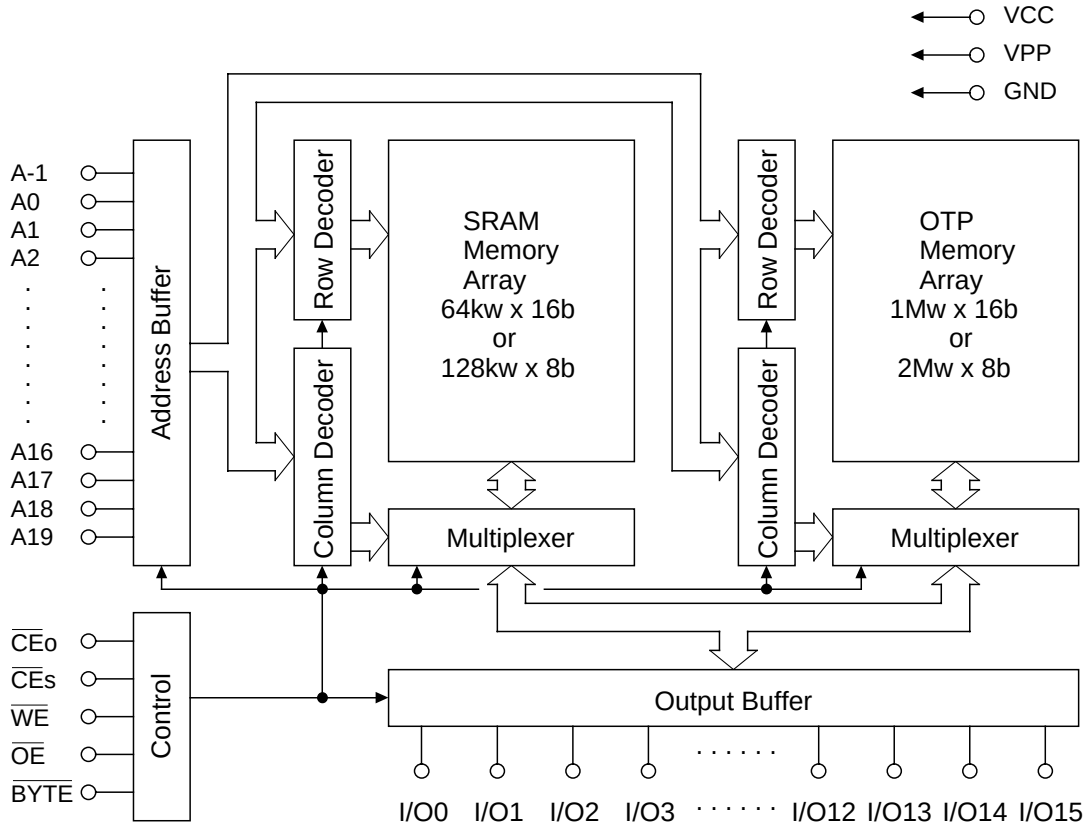
PIN CONFIGURATION (TOP VIEW)



48-pin FBGA

Pin Name	Function
A -1 - A15	Common Address Inputs
A16 - A19	Address Inputs for OTP
$\overline{CE}$s	Chip Enable for SRAM
$\overline{CE}$o	Chip Enable for OTP
$\overline{WE}$	Write Enable for SRAM
$\overline{OE}$	Common Output Enable
I/O0 - I/O15	Common Data Inputs / Outputs
VCC	Common Power Supply
$\overline{BYTE}$/VPP	Common Mode Switch & Program Power Supply for OTP
GND	Common Ground
NC	No Connection

BLOCK DIAGRAM



FUNCTION TABLE

Operating Mode		$\overline{CEo}$	$\overline{CEs}$	$\overline{WE}$	$\overline{OE}$	$\overline{BYTE}$ / VPP	VCC	I/O0 - I/O7	I/O8 - I/O14	I/O15 / A-1
Standby		H	H	*	*	H	2.7V to 3.6V	High-Z	High-Z	High-Z
		H	H	*	*	L		High-Z	High-Z	*
SRAM Read	16-Bit	H	L	H	H	H		High-Z	High-Z	High-Z
		H	L	H	L	H		DOUT	DOUT	DOUT
	8-Bit	H	L	H	H	L		High-Z	High-Z	*
		H	L	H	L	L		DOUT	High-Z	L / H
SRAM Write	16-Bit	H	L	L	*	H		DIN	DIN	DIN
	8-Bit	H	L	L	*	L		DIN	High-Z	L / H
OTP Read	16-Bit	L	H	*	H	H		High-Z	High-Z	High-Z
		L	H	*	L	H		DOUT	DOUT	DOUT
	8-Bit	L	H	*	H	L		High-Z	High-Z	*
		L	H	*	L	L		DOUT	High-Z	L / H

Note : 1. * = Don't Care ("H" or "L")

2. It is forbidden to apply $\overline{CEo}$="L" and $\overline{CEs}$="L" simultaneously.

FUNCTION TABLE (Continued)

Operating Mode	$\overline{CE}$o	$\overline{CE}$s	$\overline{WE}$	$\overline{OE}$	$\overline{BYTE}$ / VPP	VCC	I/O0 - I/O7	I/O8 - I/O14	I/O15 / A-1
OTP Program	L	H	*	H	9.75V	4.0V	DIN	DIN	DIN
OTP Program Inhibit	H	H	*	H			High-Z	High-Z	High-Z
OTP Program Verify	H	H	*	L			DOUT	DOUT	DOUT

Note : 1. * = Don't Care ("H" or "L")

2. It is forbidden to apply $\overline{CE}$o="L" and $\overline{CE}$s="L" simultaneously.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	VCC	Respect to GND	-0.5 to 5.0	V
	VPP		-0.5 to 11.5	V
Input Voltage	VI		-0.5* to Vcc+0.5	V
Output Voltage	VO		-0.5* to Vcc+0.5	V
Power Dissipation	PD	Ta=25°C	0.7	W
Operating Temperature	Topr	—	-20 to 70	°C
Storage Temperature	Tstg	—	-55 to 125	°C

* -1.2VMin. for pulse width less than 30nS.

Recommended Operating Conditions

(Ta= -20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	VCC	—	2.7	—	3.6	V
	VPP		-0.5	—	Vcc+0.5	V
	GND		0	0	0	V
SRAM Data Retention Voltage	VCCH	—	1.5	—	3.6	V
Input High Voltage	VIH	Vcc=2.7 to 3.6	2.2	—	Vcc+0.5	V
Input Low Voltage	VIL		-0.5*	—	0.4	V

* -1.2VMin. for pulse width less than 30nS.

DC Characteristics (1)

(Vcc=3.0V±0.3V,Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	-1.0	—	1.0	μA
Output Leakage Current	I_{LO}	$\overline{CE}_O$=V_{IH} , $\overline{CE}_S$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=0 to V_{CC}	-1.0	—	1.0	μA
Output High Voltage	V_{OH}	I_{OH}=-500μA	Vcc-0.5	—	—	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Standby Power Supply Current	ICCS	$\overline{CE}_O$≥VCC-0.2V $\overline{CE}_S$≥VCC-0.2V V_{IN}=0 to V_{CC}	—	—	10	μA
	ICCS1	$\overline{CE}_O$=V_{IH} $\overline{CE}_S$=V_{IH} V_{IN}=V_{IH} or V_{IL}	—	—	0.3	mA
Operating Power Supply Current	I_{CCA} (SRAM)	$\overline{CE}_O$=V_{IH} $\overline{CE}_S$=V_{IL} $\overline{OE}$=V_{IH} V_{IN}=V_{IH}/V_{IL} T_{CYC}=100nS	—	—	35	mA
		$\overline{CE}_O$≥VCC-0.2V $\overline{CE}_S$≤0.2V $\overline{OE}$≥VCC-0.2V V_{IH}≥VCC-0.2V V_{IL}≤0.2V T_{CYC}=1μS	—	—	10	mA
	I_{CCA}* (OTP)	$\overline{CE}_O$=V_{IL} $\overline{CE}_S$=V_{IH} $\overline{OE}$=V_{IH} V_{IN}=V_{IH}/V_{IL} T_{CYC}=100nS	—	—	35	mA
		$\overline{CE}_O$≤0.2V $\overline{CE}_S$≥VCC-0.2V $\overline{OE}$≥VCC-0.2V V_{IH}≥VCC-0.2V V_{IL}≤0.2V T_{CYC}=1μS	—	—	20	mA
V_{PP} Power Supply Current	I_{PP}	$\overline{BYTE}$/V_{PP}=V_{CC}	—	—	10	μA

* Read Current

DC Characteristics (2)

(Vcc=3.3V±0.3V,Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC}	-1.0	—	1.0	μA
Output Leakage Current	I_{LO}	$\overline{CE}_O$=V_{IH} , $\overline{CE}_S$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=0 to V_{CC}	-1.0	—	1.0	μA
Output High Voltage	V_{OH}	I_{OH}=-500μA	Vcc-0.5	—	—	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Standby Power Supply Current	ICCS	$\overline{CE}_O$≥VCC-0.2V $\overline{CE}_S$≥VCC-0.2V V_{IN}=0 to V_{CC}	—	—	10	μA
	ICCS1	$\overline{CE}_O$=V_{IH} $\overline{CE}_S$=V_{IH} V_{IN}=V_{IH} or V_{IL}	—	—	0.3	mA
Operating Power Supply Current	I_{CCA} (SRAM)	$\overline{CE}_O$=V_{IH} $\overline{CE}_S$=V_{IL} $\overline{OE}$=V_{IH} V_{IN}=V_{IH}/V_{IL} T_{CYC}=80nS	—	—	40	mA
		$\overline{CE}_O$≥VCC-0.2V $\overline{CE}_S$≤0.2V $\overline{OE}$≥VCC-0.2V V_{IH}≥VCC-0.2V V_{IL}≤0.2V T_{CYC}=1μS	—	—	15	mA
	I_{CCA}* (OTP)	$\overline{CE}_O$=V_{IL} $\overline{CE}_S$=V_{IH} $\overline{OE}$=V_{IH} V_{IN}=V_{IH}/V_{IL} T_{CYC}=80nS	—	—	40	mA
		$\overline{CE}_O$≤0.2V $\overline{CE}_S$≥VCC-0.2V $\overline{OE}$≥VCC-0.2V V_{IH}≥VCC-0.2V V_{IL}≤0.2V T_{CYC}=1μS	—	—	25	mA
V_{PP} Power Supply Current	I_{PP}	$\overline{BYTE}$/V_{PP}=V_{CC}	—	—	10	μA

* Read Current

SRAM AC Characteristics

SRAM Read Cycle (1)

(Vcc=3.0V±0.3V,Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t_{RC}	—	100	—	nS
Address Access Time	t_{AA}	—	—	100	nS
$\overline{CE}$s Access Time	t_{CO}	—	—	100	nS
$\overline{OE}$ Access Time	t_{OE}	—	—	50	nS
$\overline{CE}$s to Output in Low-Z	t_{CLZ}	—	10	—	nS
$\overline{OE}$ to Output in Low-Z	t_{OLZ}	—	5	—	nS
Output Hold from Address Change	t_{OH}	—	10	—	nS
$\overline{CE}$s to Output in High-Z	t_{CHZ}	—	—	35	nS
$\overline{OE}$ to Output in High-Z	t_{OHZ}	—	—	35	nS

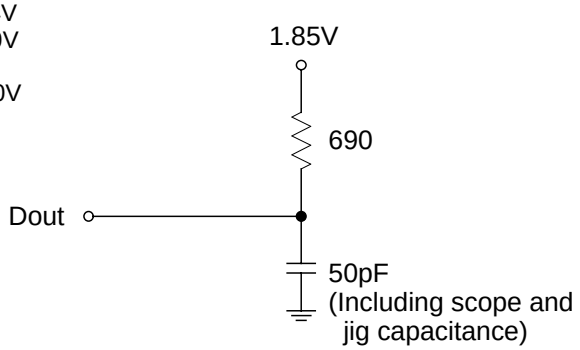
SRAM Write Cycle (1)

(Vcc=3.0V±0.3V,Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Write Cycle Time	t_{WC}	—	100	—	nS
Address Setup Time	t_{AS}	—	0	—	nS
Write Pulse Width	t_{WP}	—	75	—	nS
Write Recovery Time	t_{WR}	—	0	—	nS
Data Setup Time	t_{DS}	—	40	—	nS
Data Hold Time	t_{DH}	—	0	—	nS
$\overline{WE}$ to Output in High-Z	t_{WHZ}	—	—	35	nS
$\overline{CE}$s to End of Write	t_{CW}	—	90	—	nS
Address Valid to End of Write	t_{AW}	—	90	—	nS
Output Active from End of Write	t_{WLZ}		5	—	nS

Test Condition

Input Pulse Levels ---------- 0.4V/2.4V
Input Timing Reference Levels --------- 0.8V/2.0V
Output Load ---------- 50pF
Output Timing Reference Levels ------- 0.8V/2.0V
Input Rise and Fall Time ---------- 5nS



SRAM Read Cycle (2)

(Vcc=3.3V±0.3V,Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t_{RC}	—	80	—	nS
Address Access Time	t_{AA}	—	—	80	nS
$\overline{CE}$s Access Time	t_{CO}	—	—	80	nS
$\overline{OE}$ Access Time	t_{OE}	—	—	40	nS
$\overline{CE}$s to Output in Low-Z	t_{CLZ}	—	10	—	nS
$\overline{OE}$ to Output in Low-Z	t_{OLZ}	—	5	—	nS
Output Hold from Address Change	t_{OH}	—	10	—	nS
$\overline{CE}$s to Output in High-Z	t_{CHZ}	—	—	30	nS
$\overline{OE}$ to Output in High-Z	t_{OHZ}	—	—	30	nS

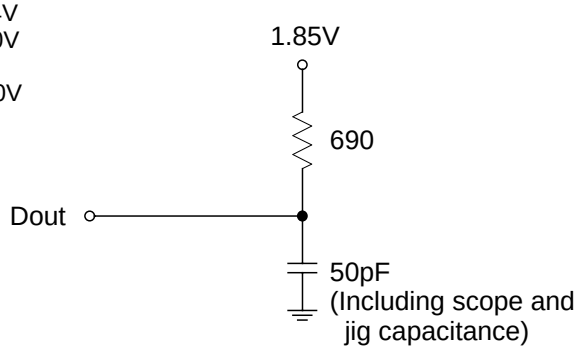
SRAM Write Cycle (2)

(Vcc=3.3V±0.3V,Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Write Cycle Time	t_{WC}	—	80	—	nS
Address Setup Time	t_{AS}	—	0	—	nS
Write Pulse Width	t_{WP}	—	60	—	nS
Write Recovery Time	t_{WR}	—	0	—	nS
Data Setup Time	t_{DS}	—	35	—	nS
Data Hold Time	t_{DH}	—	0	—	nS
$\overline{WE}$ to Output in High-Z	t_{WHZ}	—	—	30	nS
$\overline{CE}$s to End of Write	t_{CW}	—	70	—	nS
Address Valid to End of Write	t_{AW}	—	70	—	nS
Output Active from End of Write	t_{WLZ}		5	—	nS

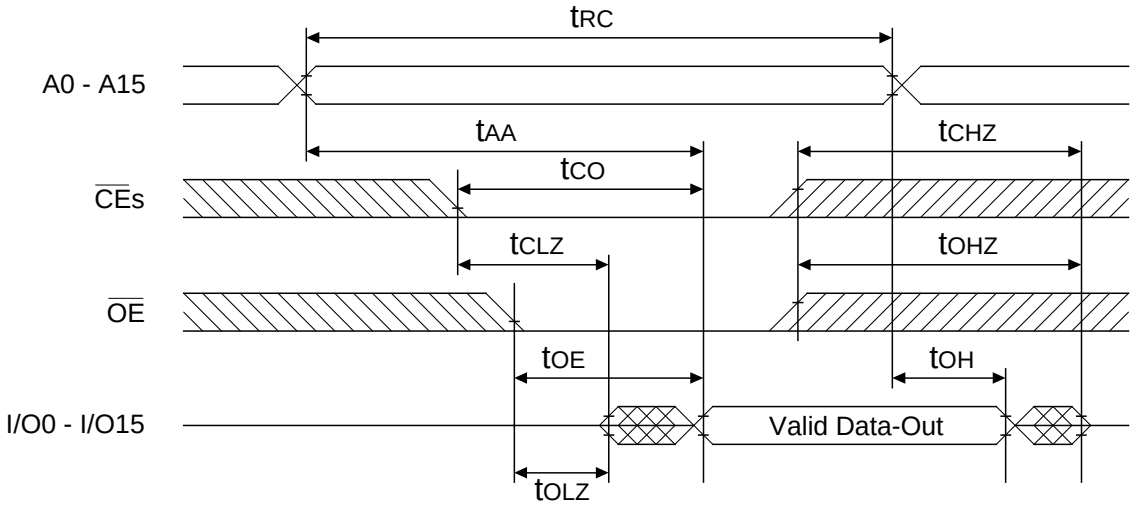
Test Condition

Input Pulse Levels ---------- 0.4V/2.4V
Input Timing Reference Levels --------- 0.8V/2.0V
Output Load ---------- 50pF
Output Timing Reference Levels ------- 0.8V/2.0V
Input Rise and Fall Time ---------- 5nS

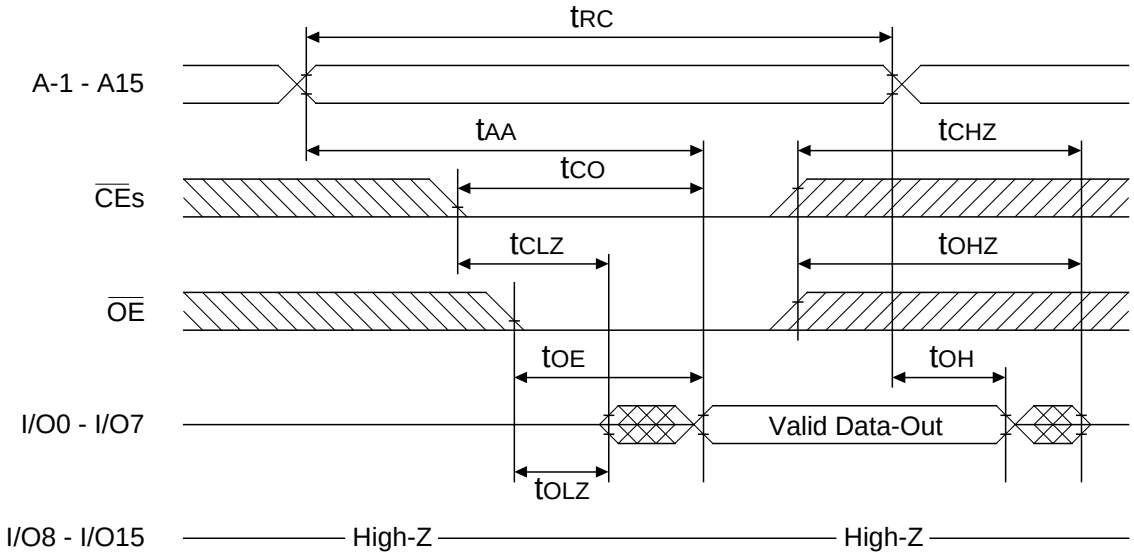


SRAM Timing Diagrams

SRAM Read Cycle (1)
16-bit Read Mode ($\overline{BYTE}$=VIH)



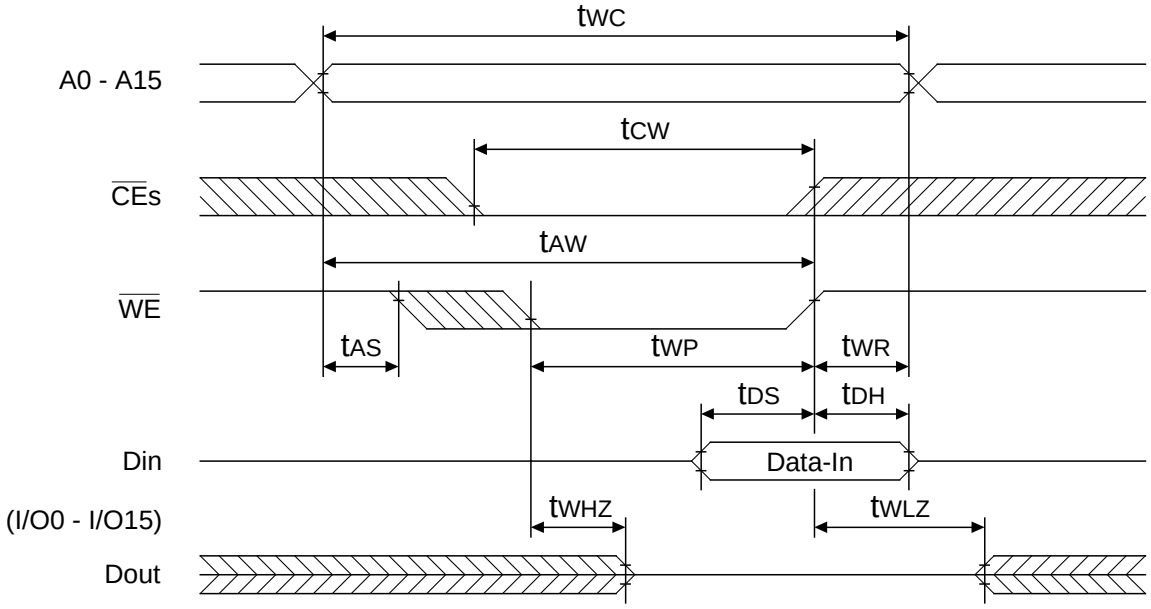
SRAM Read Cycle (2)
8-bit Read Mode ($\overline{BYTE}$=VIL)



Notes : 1. A read cycle of SRAM occurs during the overlap of $\overline{CE}$o="H", $\overline{CE}$s="L", $\overline{OE}$="L" and $\overline{WE}$="H".
2. tOHZ , tCHZ are specified by the time when DATA is floating , not defined by the output level.

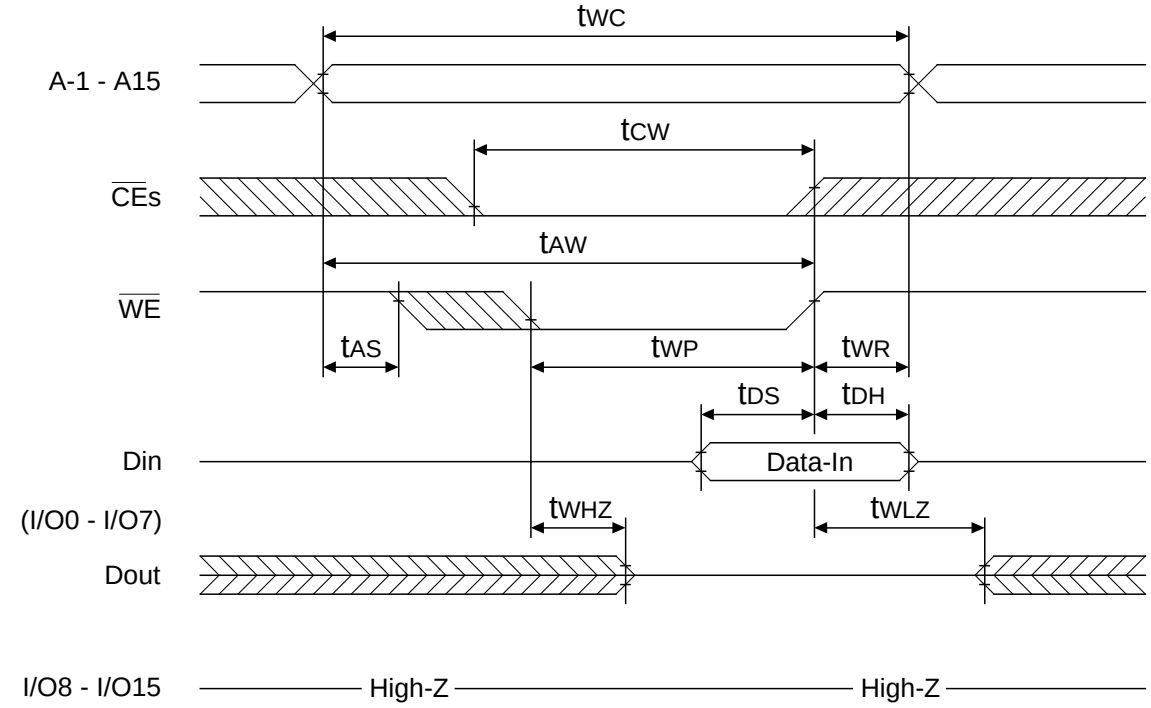
SRAM Write Cycle (1)

16-bit Write Mode ($\overline{BYTE}$=VIH)



SRAM Write Cycle (2)

8-bit Write Mode ($\overline{BYTE}$=VIL)

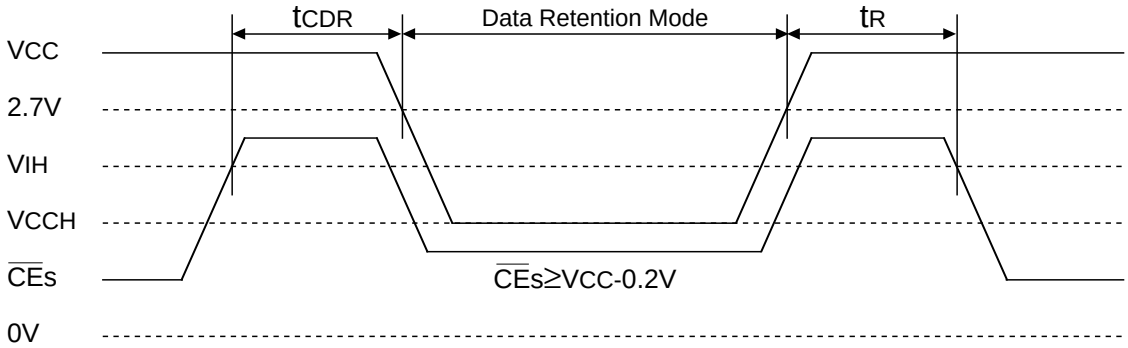


Notes : 1. A write cycle of SRAM occurs during the overlap of $\overline{CE}$o="H" , $\overline{CE}$s="L" and $\overline{WE}$="L".
2. $\overline{OE}$ may be either of "H" or "L" in the write cycle of SRAM.
3. t_{AS} is specified from $\overline{CE}$s="L" or $\overline{WE}$="L" , whichever occurs last.
4. t_{WP} is an overlap time of $\overline{CE}$s="L" and $\overline{WE}$="L".
5. t_{WR} , t_{DS} , t_{DH} are specified from $\overline{CE}$s="H" or $\overline{WE}$="H" , whichever occurs first.
6. t_{WHZ} is specified by the time when DATA output is floating , not defined by the output level.
7. When I/O pins are in the output mode , don't apply the inverted input signal to the output pins.

SRAM Data Retention Characteristics

(Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	VCCH	$\overline{CE}$o≥VCC-0.2V $\overline{CE}$s≥VCC-0.2V VIN=0 to VCC	1.5	—	—	V
Data Retention Power Supply Current	ICCH	VCC=1.5V $\overline{CE}$o≥VCC-0.2V $\overline{CE}$s≥VCC-0.2V VIN=0 to VCC	—	—	3	μA
Chip Deselect to Data Retention Time	t_{CDR}	—	0	—	—	nS
Operation Recovery Time	t_R	—	5	—	—	mS



OTP AC Characteristics (1)

OTP Read Cycle (1)

(Vcc=3.0V±0.3V,Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t_{RC}	—	100	—	nS
Address Access Time	t_{AA}	$\overline{CE}_O$=$\overline{OE}$=V_{IL}	—	100	nS
$\overline{CE}_O$ Access Time	t_{CO}	$\overline{OE}$=V_{IL}	—	100	nS
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}_O$=V_{IL}	—	50	nS
$\overline{CE}_O$ to Output in High-Z	t_{CHZ}	$\overline{OE}$=V_{IL}	0	40	nS
$\overline{OE}$ to Output in High-Z	t_{OHZ}	$\overline{CE}_O$=V_{IL}	0	35	nS
Output Hold from Address Change	t_{OH}	$\overline{CE}_O$=$\overline{OE}$=V_{IL}	0	—	nS

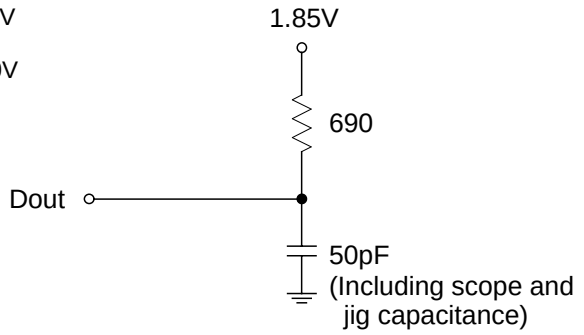
OTP Read Cycle (2)

(Vcc=3.3V±0.3V,Ta=-20 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Read Cycle Time	t_{RC}	—	80	—	nS
Address Access Time	t_{AA}	$\overline{CE}_O$=$\overline{OE}$=V_{IL}	—	80	nS
$\overline{CE}_O$ Access Time	t_{CO}	$\overline{OE}$=V_{IL}	—	80	nS
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}_O$=V_{IL}	—	50	nS
$\overline{CE}_O$ to Output in High-Z	t_{CHZ}	$\overline{OE}$=V_{IL}	0	40	nS
$\overline{OE}$ to Output in High-Z	t_{OHZ}	$\overline{CE}_O$=V_{IL}	0	35	nS
Output Hold from Address Change	t_{OH}	$\overline{CE}_O$=$\overline{OE}$=V_{IL}	0	—	nS

Test Condition

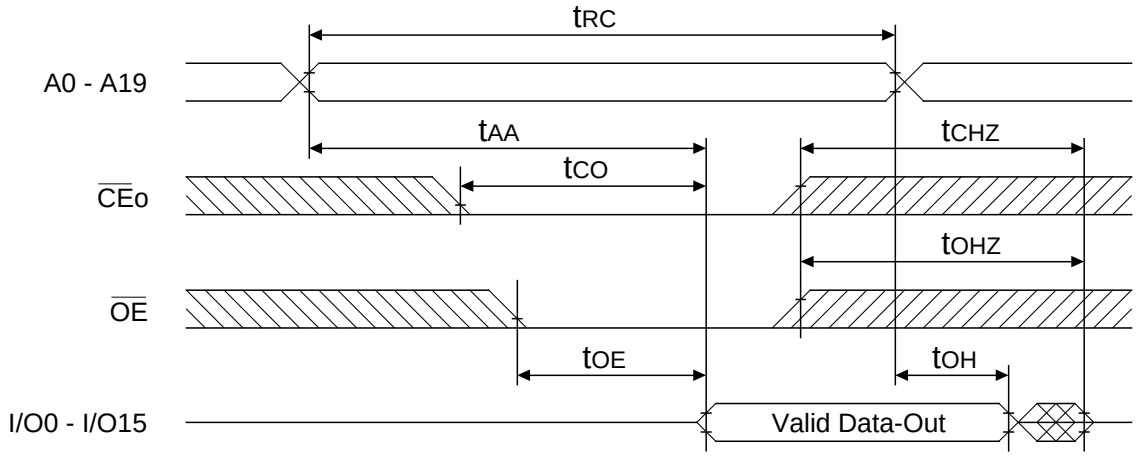
Input Pulse Levels ---------- 0.4V/2.4V
Input Timing Reference Levels --------- 0.8V/2.0V
Output Load ---------- 50pF
Output Timing Reference Levels ------- 0.8V/2.0V
Input Rise and Fall Time ---------- 5nS



OTP Timing Diagrams

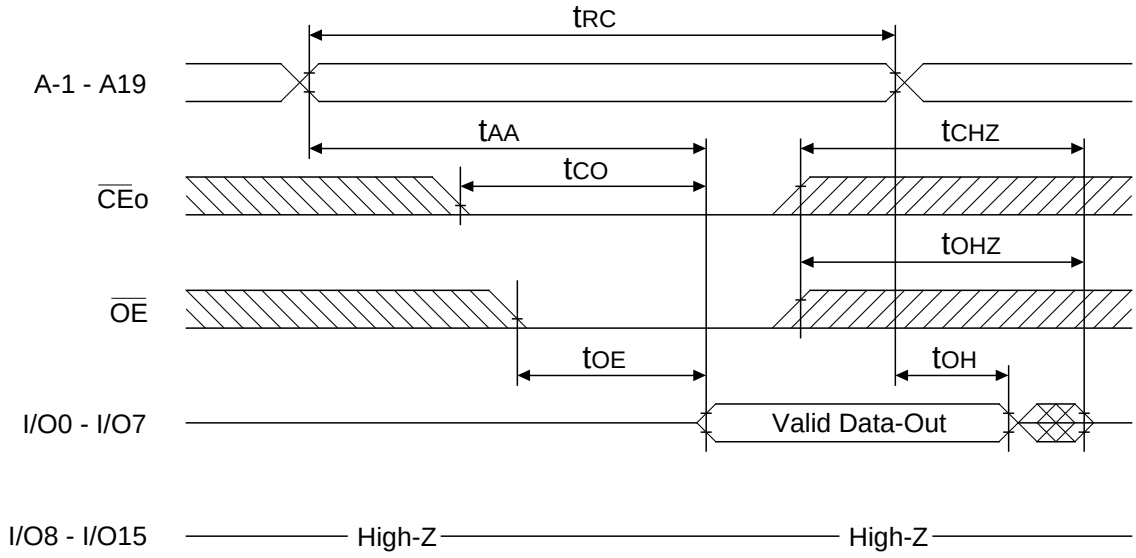
OTP Read Cycle (1)

16-bit Read Mode ($\overline{BYTE}$=VIH)



OTP Read Cycle (2)

8-bit Read Mode ($\overline{BYTE}$=VIL)



Notes : 1. A read cycle of OTP occurs during the overlap of $\overline{CE}$o="L", $\overline{CE}$s="H" and $\overline{OE}$="L".

2. tOHZ , tCHZ are specified by the time when DATA is floating , not defined by the output level.

OTP DC Characteristics

OTP Programming Operation

(Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_I=VCC+0.5V	—	—	10	μA
Program Power Supply Current	I_{PP2}	$\overline{CE}_o$=V_{IL}	—	—	50	mA
Power Supply Current	I_{CC}	—	—	—	50	mA
Input High Voltage	V_{IH}	—	3.0	—	VCC+0.5	V
Input Low Voltage	V_{IH}	—	-0.5	—	0.8	V
Output High Voltage	V_{OH}	I_{OH}=-500μA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Program Voltage	V_{PP}	—	9.5	9.75	10.0	V
VCC Voltage	V_{CC}	—	3.9	4.0	4.1	V

OTP AC Characteristics (2)

OTP Programming Operation

(Vcc=4.0V±0.1V,V_{PP}=9.75V±0.25V,Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address Setup Time	t_{AS}	—	2	—	—	μS
$\overline{OE}$ Setup Time	t_{OES}	—	2	—	—	μS
Data Setup Time	t_{DS}	—	2	—	—	μS
Address Hold Time	t_{AH}	—	0	—	—	μS
Data Hold Time	t_{DH}	—	2	—	—	μS
$\overline{OE}$ to Output in High-Z	t_{DFP}	—	0	—	130	nS
V_{PP} Power Setup Time	t_{VS}	—	2	—	—	μS
Program Pulse Width	t_{PW}	—	9	10	11	μS
Data Valid from $\overline{OE}$	t_{OE}	—	—	—	150	nS

Pin Check Function

Pin Check Function is to check contact between each device-pin and each socket-lead with EPROM programmer.

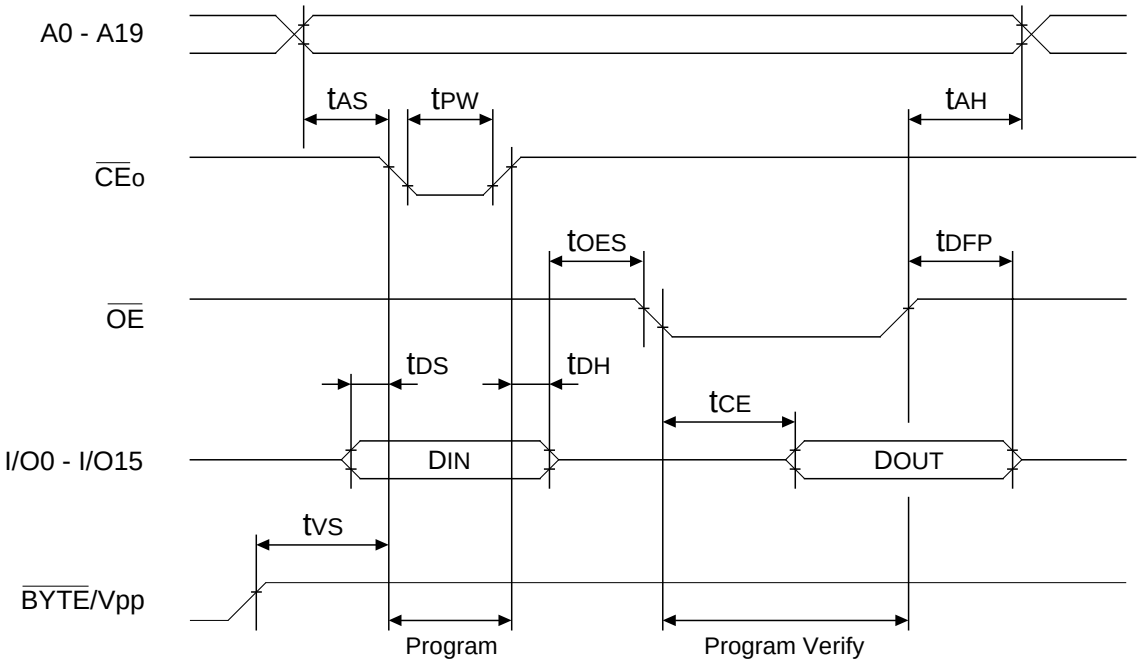
Setting up address as the following condition call the preprogrammed codes on device outputs.

(V_{cc}=3.3V±0.3V,$\overline{CE}_o$=V_{IL},$\overline{BYTE}$/V_{pp}=V_{IH},Ta=25°C±5°C)

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	DATA
0	1	0	1	0	1	0	1	0	VH*	0	1	0	1	0	1	0	0	1	1	FF00
1	0	1	0	1	0	1	0	1	VH*	1	0	1	0	1	0	1	1	0	0	00FF

* :VH=8V

OTP Programming Waveform



Note : When OTP is programming mode , CEs should be "H" level.

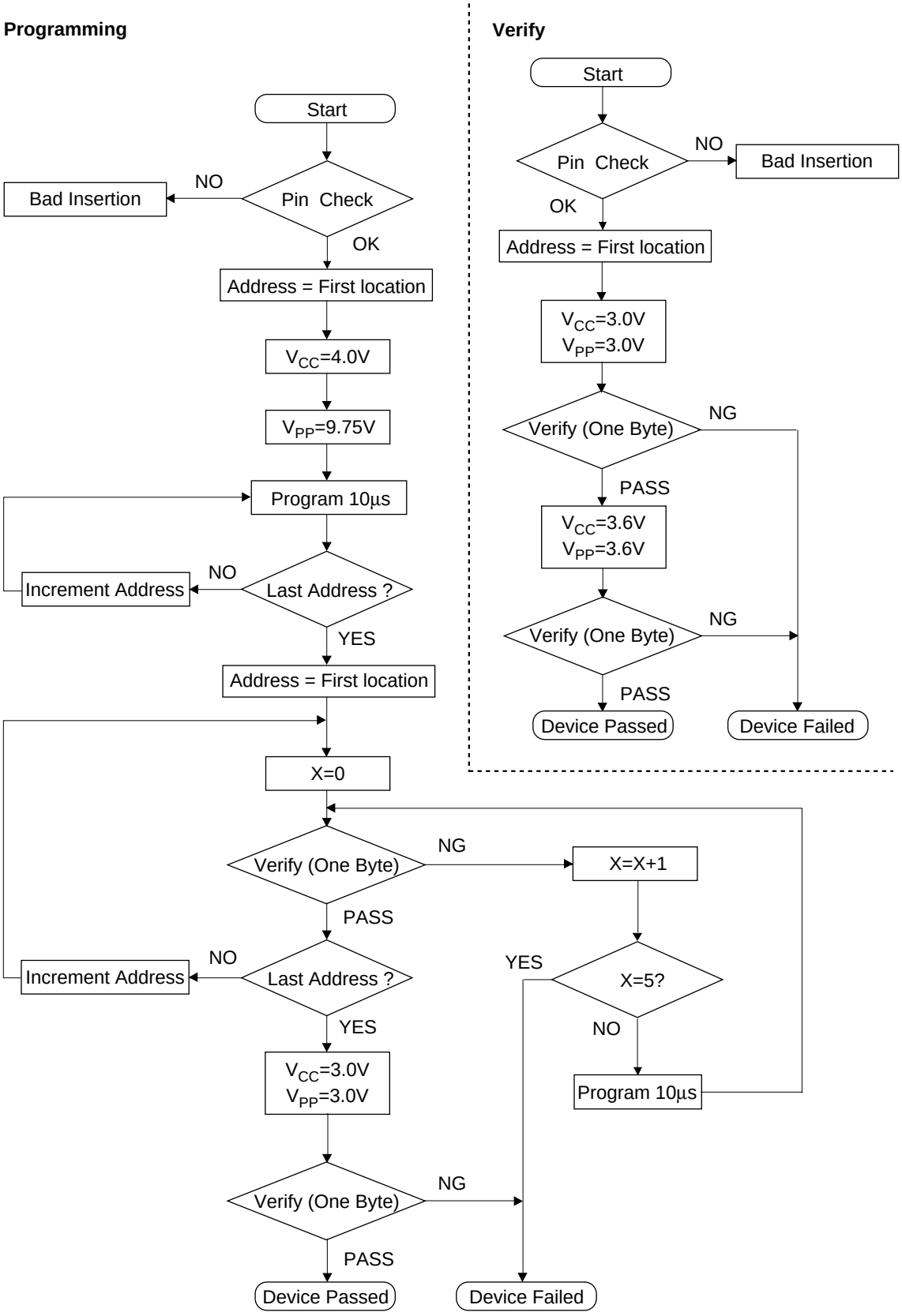
Capacitance

(Vcc=3.3V , Ta=25°C , f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	CIN1	V I=0V	—	—	10	pF
BYTE/VPP Capacitance	CIN2		—	—	60	pF
Input/Output Capacitance	CI/O	VO=0V	—	—	10	pF

Note : This parameter is periodically sampled and not 100% tested.

OTP Programming / Verify Flow Chart



NOTICE

The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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ADDRESSES & SEMICONDUCTOR WEB SITES

OKI Electric Industry Co., Ltd.,
Device Business Group,
10-3, Shibaura, 4-chome,
Minato-ku, Tokyo 108, Japan,
Tel.: +81-(0)3-5445-6327,
Fax.: +81-(0)3-5445-6328,
http://www.oki.co.jp/OKI/DBG/english/index.htm
(NOTE: URL is case sensitive)

OKI Semiconductor Group,
785 North Mary Avenue,
Sunnyvale, CA 94086, U.S.A.,
Tel.: +1-408-720-1900,
Fax.: +1-408-720-1918,
http://www.okisemi.com/

OKI Electric Europe GmbH,
Head Office Europe,
Hellersbergstrasse 2,
D-41460 Neuss, Germany,
Tel: +49-2131-15960,
Fax: +49-2131-103539,
http://www.oki-europe.de/

OKI Electronics (Hong Kong) Ltd.,
Suite 1901-1&19, Tower 3,
China Hong Kong City,
33 Canton Road, Tsimshatsui,
Kowloon, Hong Kong,
Tel.: +852-2-736-2336,
Fax.: +852-2-736-2395

OKI Semiconductor (Asia) Pte. Ltd.,
78 Shenton Way 09-01,
Singapore 0207,
Tel.: +65-221-3722,
Fax.: +65-323-5376

OKI Semiconductor (Asia) Pte. Ltd.,
Taipei Branch,
7th Fl. No.260, Tun Hwa North Road,
Taipei, Taiwan, R.O.C.,
Sumitomo-Flysun Building,
Tel.: +886-2-2719-2561,
Fax.: +886-2-2715-2892
http://www.oki.net.tw/

For further information, please contact:

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