HB56D25609A/B-85A/10A/12A

262,144-Word × 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A25609 is a 256K × 9 dynamic RAM module, mounted two 1-Mbit DRAM (HM514256A) sealed in SOJ package and 256Kbit DRAM (HM51256) sealed in PLCC package. An outline of the HB56A25609 is 30-pin single in-line package having Lead types (HB56A25609A), Socket type (HB56A25609B). Therefore, the HB56A25609 makes high density mounting possible without surface mount technology. The HB56A25609 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ and PLCC.

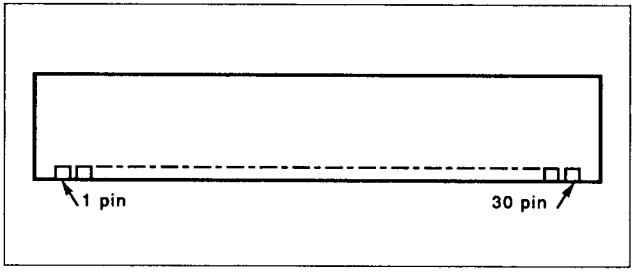
■ FEATURES

- 30-Pin Single In-Line Package
  - Lead Pitch 2.54mm
- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . 85/100/120ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . 1.11/0.94/0.79mW (max.)
  - Standby Mode . . . . . 33mW (max.)
- Fast Page Mode Capability
- 512 Refresh Cycle 8ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D25609A-85A HB56D25609A-10A HB56D25609A-12A	85ns 100ns 120ns	30 pin SIP Lead Type
HB56D25609B-85A HB56D25609B-10A HB56D25609B-12A	85ns 100ns 120ns	30 pin SIP Socket Type

■ PIN OUT

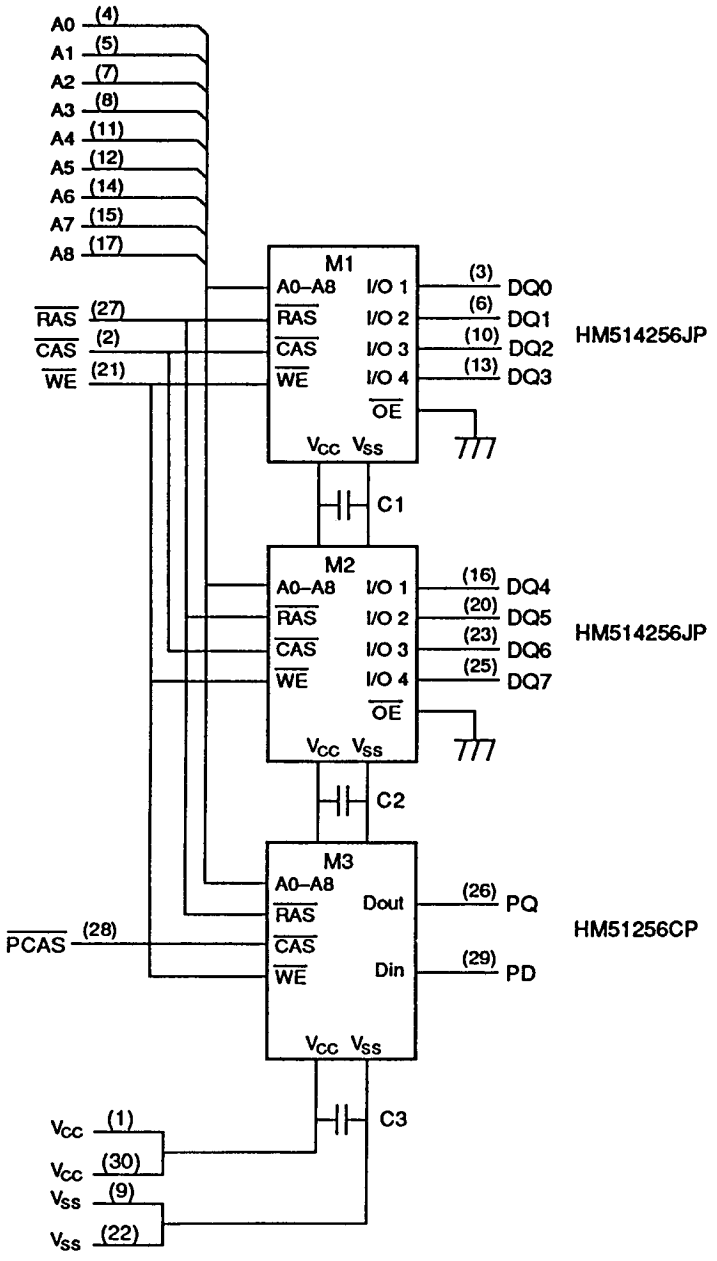


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	NC
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_8	Address Input
A_0 ~ A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0 ~ DQ_7	Data-In/Data-Out
PD	Data-In for Parity
PQ	Data-Out for Parity
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

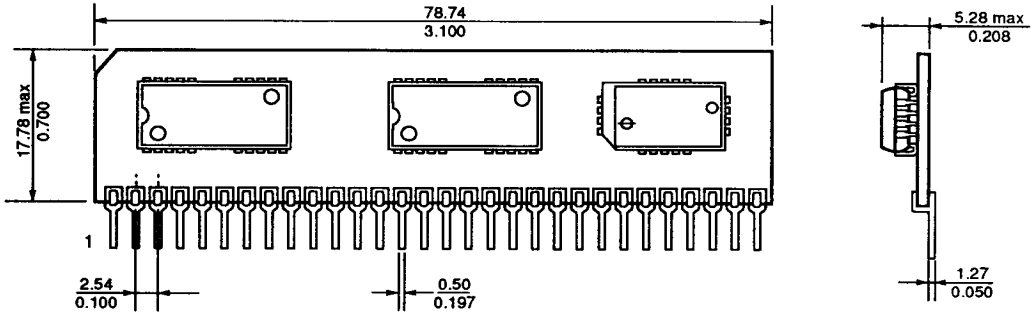
■ BLOCK DIAGRAM



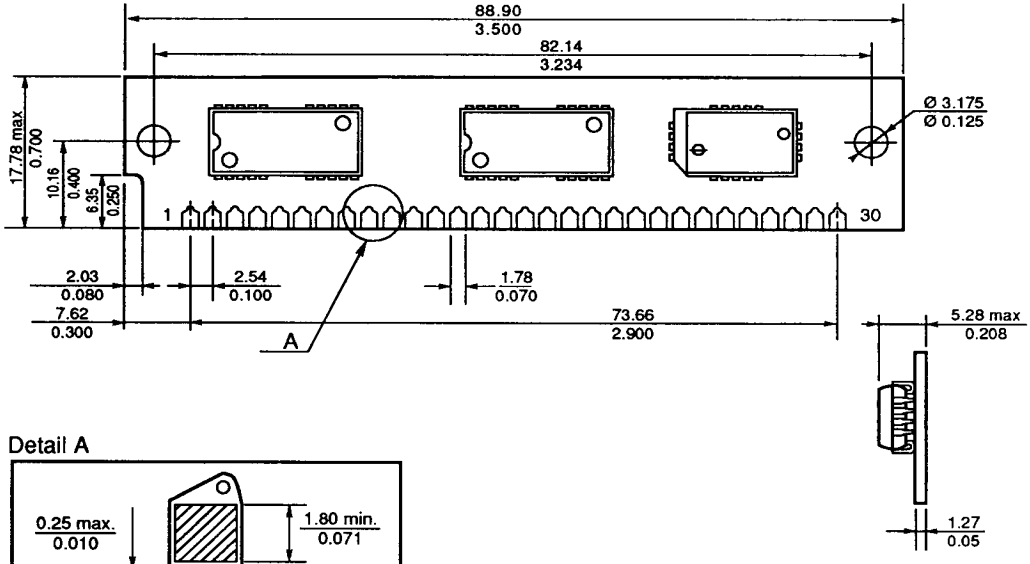
■ PHYSICAL OUTLINE

• HB56D25609A Series

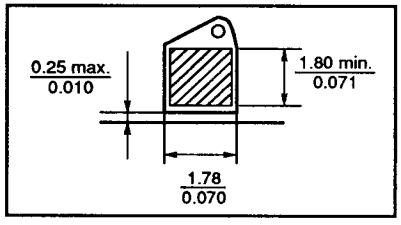
Unit: mm / inch



• HB56D25609B Series



Detail A



NOTE: The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	3	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

NOTE: 1. All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HB56D25609A/B						Unit	Note
			-85A		-10A		-12A			
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	t_{RC} = Min.	—	202	—	170	—	144	mA	1, 2
Standby Current	I_{CC2}	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z	—	6	—	6	—	6	mA	
		CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} −0.2V D_{OUT} = High-Z	—	3	—	3	—	3	mA	
$\overline{RAS}$-Only Refresh Current	I_{CC3}	t_{RC} = Min.	—	202	—	170	—	144	mA	2
Standby Current	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	—	16	—	16	—	16	mA	1
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current	I_{CC6}	t_{RC} = Min.	—	192	—	165	—	139	mA	
Fast Page Mode Current	I_{CC7}	t_{PC} = Min.	—	180	—	170	—	144	mA	1, 3
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 7V	−10	10	−10	10	−10	10	μA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 7V, D_{OUT} = Disable	−10	10	−10	10	−10	10	μA	
Output High Voltage	V_{OH}	I_{OUT} = −5 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OUT} = 4.2mA	0	0.4	0	0.4	0	0.4	V	

NOTES: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

■ CAPACITANCE (T_a = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	—	30	pF	1
Input Capacitance (Clock)	C_{I2}	—	36	pF	1
Input/Output Capacitance (DQ_0-DQ_7)	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1, 2
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

NOTES: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V) [1], [12]

• Read, Write and Refresh Cycle (Common Parameter)

Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	15

• Read Cycle

Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF}	0	20	0	25	0	30	ns	6

• Write Cycle

Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-In Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-In Hold Time	t_{DH}	20	—	20	—	25	—	ns	11
Data-In Hold Time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

• Refresh Cycle

Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

• Fast Page Mode Cycle

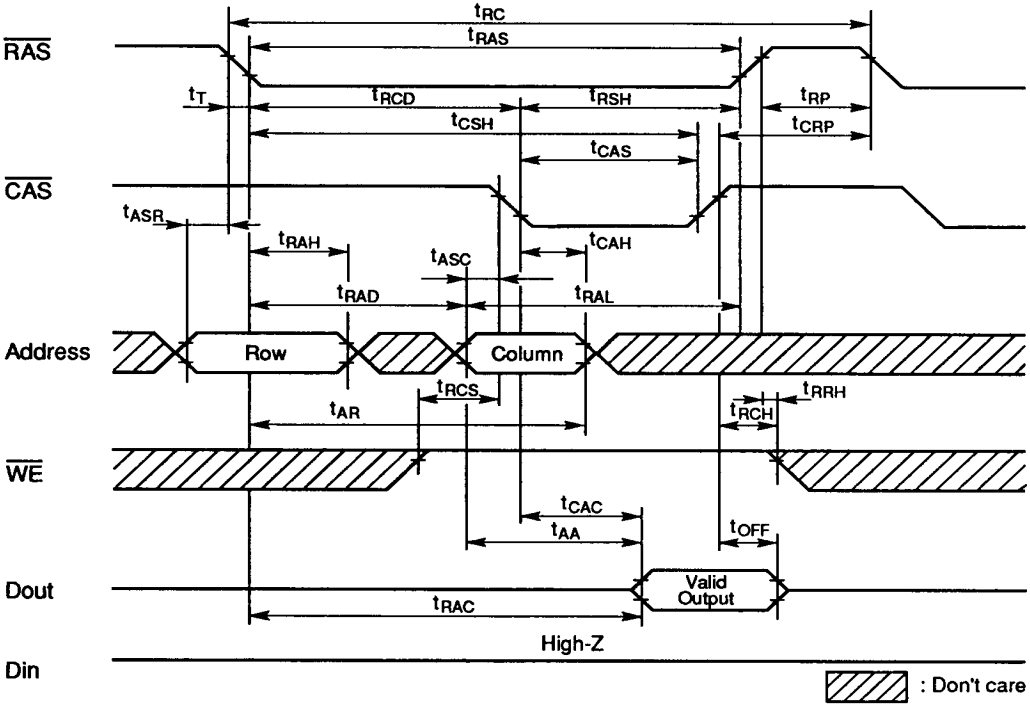
Parameter	Symbol	HB56D25609A/B						Unit	Note
		-85A		-10A		-12A			
		Min.	Max.	Min.	Max.	Min.	Max.		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

NOTES:

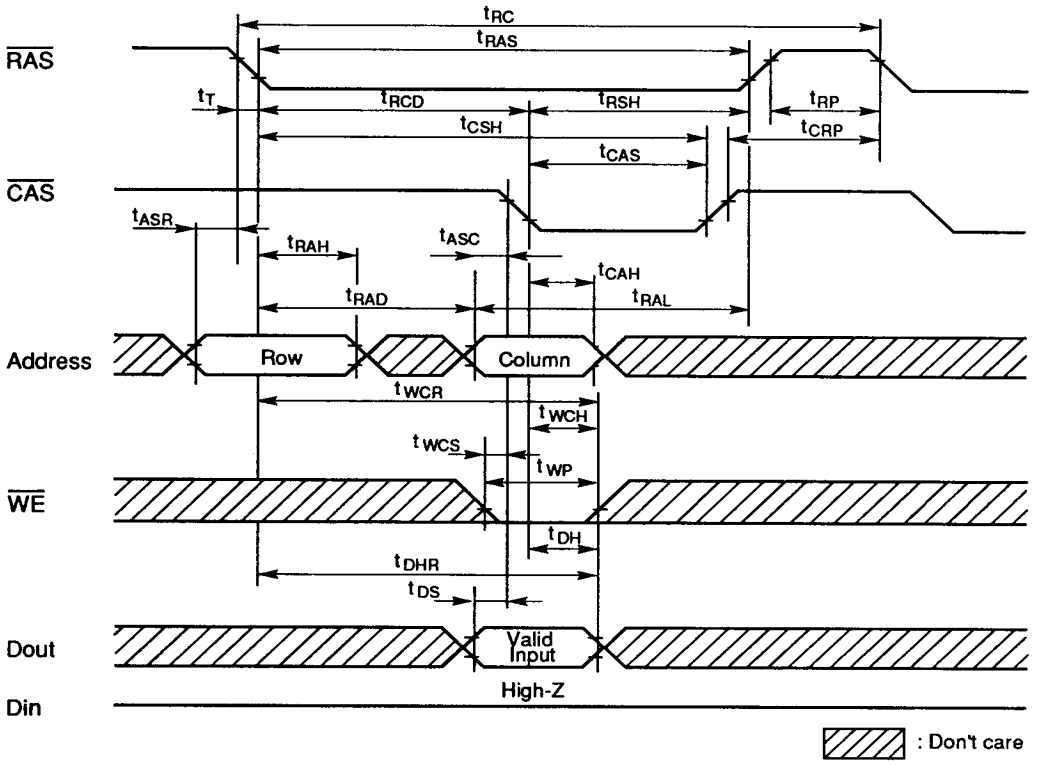
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$(min.))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 512 refresh cycles.

■ TIMING WAVEFORMS

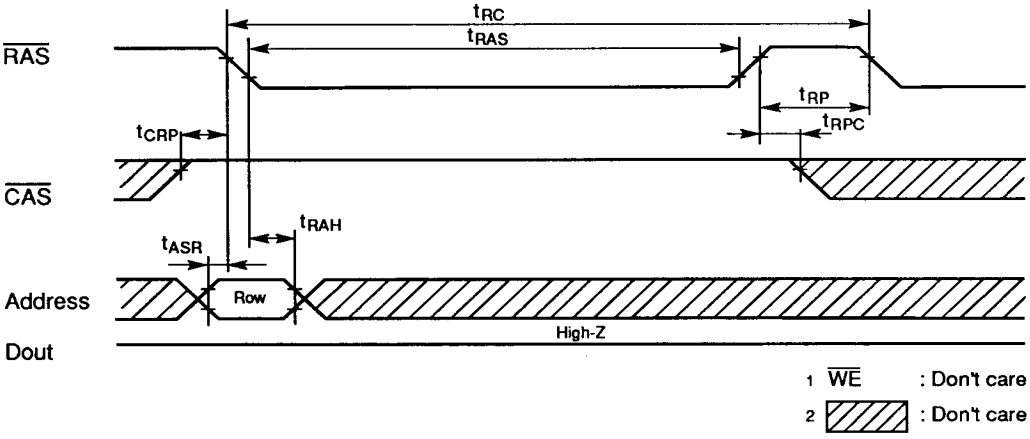
• Read Cycle



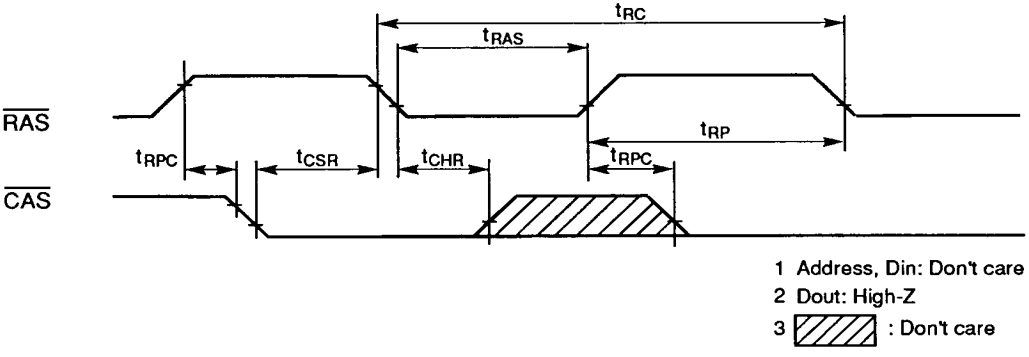
• **Early Write Cycle**



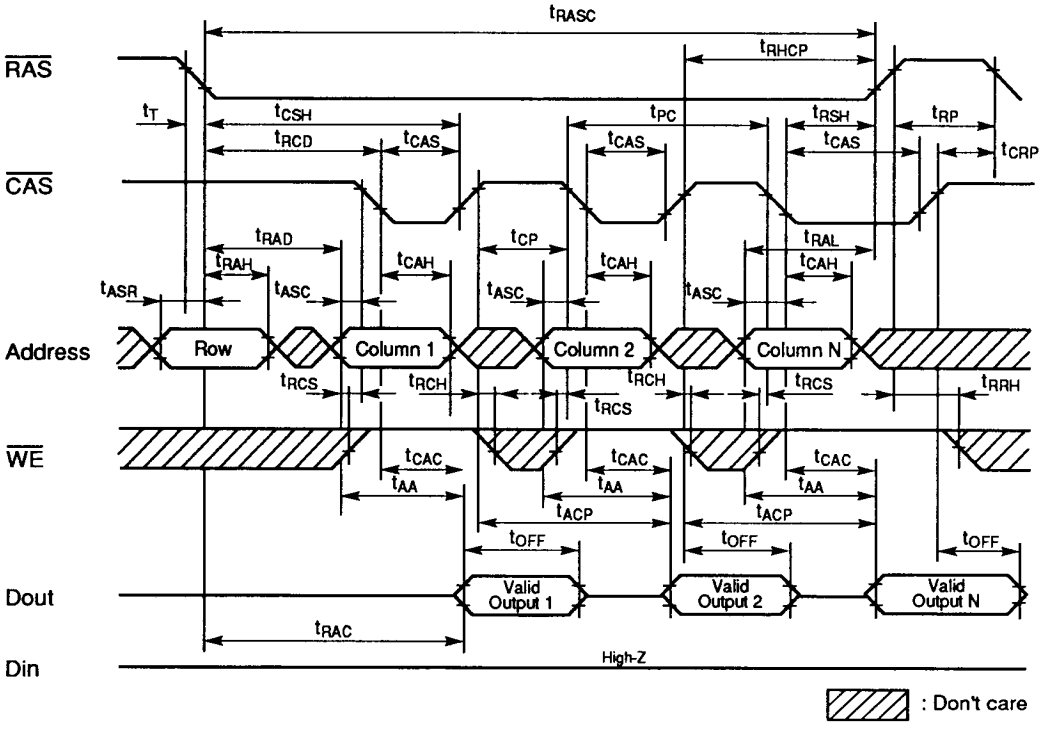
• **$\overline{RAS}$ Only Refresh Cycle**



• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**