REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20														
REV STATUS OF SHEETS	REV																			
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-11-09

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS,
512 X 18 X 2 FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-96509**

SHEET 1 OF 20

DESC FORM 193
JUL 94

5962-E349-95

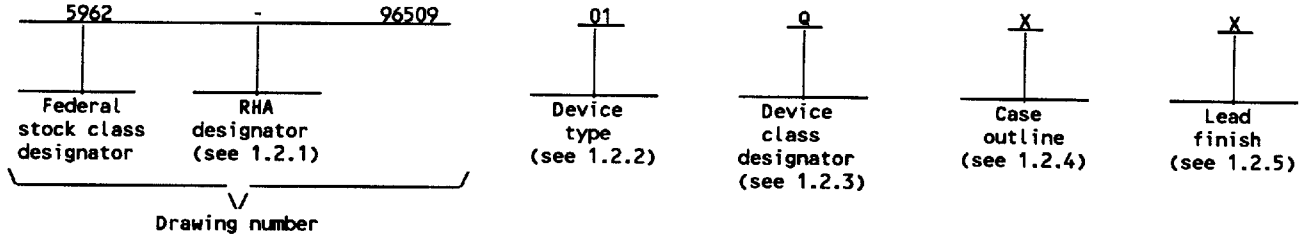
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0014840 T02

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-PRF-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function
01	54ABT7820	512 X 18 X 2 FIFO

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15 - 84	84	Pin grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-PRF-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-BUL-103.

1.3 Absolute maximum ratings. 2/ 3/ 4/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc 5/
DC output voltage range (V_{OUT})	-0.5 V dc to +5.5 V dc 5/
DC output current (I_{OL}) (per output)	+48 mA
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V)	-18 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0 V)	-50 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D)	500 mW

1.4 Recommended operating conditions. 3/ 4/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V
Minimum high level input voltage (V_{IH})	2.0 V
Maximum high level output current (I_{OH})	-12 mA
Maximum low level output current (I_{OL})	+24 mA
Maximum input rise or fall rate ($\Delta t/\Delta V$)	5 ns/V
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Unless otherwise noted, all voltages are referenced to GND.
4/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
5/ The input negative voltage rating may be exceeded provided that the input clamp current rating is observed.
6/ Values will be added when they become available.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC STANDARD No. 17 - A Standard Test Procedure for the characterization of latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-PRF-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$, $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device types	Group A subgroups	Limits 2/ Min	Limits 2/ Max	Unit
High level output voltage	V_{OH}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V	I_{OH} = -3.0 mA, V_{CC} = 4.5 V	All	1, 2, 3	2.5		V
			I_{OH} = -3.0 mA, V_{CC} = 5.0 V	All	1, 2, 3	3.0		
			I_{OH} = -12.0 mA, V_{CC} = 4.5 V	All	1, 2, 3	2.0		
Low level output voltage	V_{OL}	For all inputs affecting output under test, V_{IN} = 2.0 V or 0.8 V, I_{OL} = 24 mA, V_{CC} = 4.5 V		All	1, 2, 3		0.55	V
Negative input clamp voltage	V_{IC-}	For input under test, I_{IN} = -18 mA, V_{CC} = 4.5 V		All	1, 2, 3		-1.2	V
Input current	I_I 3/	For input under test, $V_I = V_{CC}$ or GND, V_{CC} = 5.5 V		All	1, 2, 3		±5	µA
Three-state output leakage current high	I_{OZH} 3/	For control input affecting output under test, V_{IN} = 2.0 V or 0.8 V, V_{OUT} = 2.7 V, V_{CC} = 5.5 V		All	1, 2, 3		50	µA
Three-state output leakage current low	I_{OZL} 3/	For control input affecting output under test, V_{IN} = 2.0 V or 0.8 V, V_{OUT} = 0.5 V, V_{CC} = 5.5 V		All	1, 2, 3		-50	µA
Output current	I_O 4/	V_{OUT} = 2.5 V, V_{CC} = 4.5 V		All	1, 2, 3	-40	-180	mA
Quiescent supply current, outputs high	I_{CCH}	For all inputs, $V_{IN} = V_{CC}$ or GND, I_{OUT} = 0 A, V_{CC} = 5.5 V		All	1, 2, 3		15	mA
Quiescent supply current, outputs low	I_{CCL}			ALl	1, 2, 3		95	mA
Quiescent supply current, outputs disabled	I_{CCZ}			All	1, 2 ,3		15	mA
Control Input capacitance	C_{IN}	T_C = +25°C, See 4.4.1b, V_{CC} = 5.0 V	Control inputs	All	4		10.5	pF
I/O capacitance	$C_{I/O}$		A or B ports	All	4		14.5	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device types	Group A subgroups	Limits 2/		Unit
						Min	Max	
Functional test 5/		V_{IH} = 2.0 V, V_{IL} = 0.8 V Verify output V_O See 4.4.1c, V_{CC} = 4.5 V and 5.5 V		All	7, 8A, 8B	L	H	
					7, 8A, 8B	L	H	
Pulse duration	t_{w1}	C_L = 50 pF minimum, R_L = 500Ω V_{CC} = 4.5 V and 5.5 V See figure 3 as applicable	LDCKA, LDCKB high	All	9, 10, 11	9		ns
	t_{w2}		LDCKA, LDCKB low	All	9, 10, 11	9		
	t_{w3}		UNCKA, UNCKB high	All	9, 10, 11	9		
	t_{w4}		UNCKA, UNCKB low	All	9, 10, 11	9		
	t_{w5}		$\overline{RSTA}$, $\overline{RSTB}$ low	All	9, 10, 11	10		
Setup time	t_{su1}		A0-A17 before LDCKA↑ and B0-B17 before LDCKB↑	All	9, 10, 11	4		
	t_{su2}		$\overline{PENA}$ before LDCKA↑ and $\overline{PENB}$ before LDCKB↑	All	9, 10, 11	6		
	t_{su3}		LDCKA inactive before $\overline{RSTA}$ high and LDCKB inactive before $\overline{RSTB}$ high	All	9, 10, 11	4		
Hold time	t_{h1}		A0-A17 after LDCKA↑ and B0-B17 after LDCKB↑	All	9, 10, 11	0		
	t_{h2}		$\overline{PENA}$ after LDCKA low and $\overline{PENB}$ after LDCKB low	All	9, 10, 11	3		
	t_{h3}		LDCKA inactive after $\overline{RSTA}$ high and LDCKB inactive after $\overline{RSTB}$ high	All	9, 10, 11	4		
Maximum operating frequency	f_{MAX}			All	9, 10, 11	40		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits 2/		Unit
					Min	Max	
Propagation delay time, LDCKA↑ or LCDKB↑ to B or A	t_{pd1}	C_L = 50 pF minimum, R_L = 500Ω See figure 3	All	9, 10,11	3	18	ns
Propagation delay time, UNCKA↑ or UNCKB↑ to B or A	t_{pd2}		All	9, 10,11	3	15	
Propagation delay time, LDCKA↑ or LDCKB↑ to $\overline{EMPTYA}$ or $\overline{EMPTYB}$	t_{PLH1}		All	9, 10, 11	3	17	
Propagation delay time, UNCKA↑ or UNCKB↑ to $\overline{EMPTYA}$ or $\overline{EMPTYB}$	t_{PHL1}		All	9, 10, 11	3	16	
Propagation delay time, $\overline{RSTA}$ low or $\overline{RSTB}$ low to $\overline{EMPTYA}$ or $\overline{EMPTYB}$	t_{PHL2}		All	9, 10, 11	5	18	
Propagation delay time, LDCKA↑ or LDCKB↑ to $\overline{FULLA}$ or $\overline{FULLB}$	t_{PHL3}		All	9, 10, 11	5	16	
Propagation delay time, UNCKA↑ or UNCKB↑ to $\overline{FULLA}$ or $\overline{FULLB}$	t_{PLH2}		All	9, 10, 11	5	17	
Propagation delay time, $\overline{RSTA}$ low or $\overline{RSTB}$ low to $\overline{FULLA}$ or $\overline{FULLB}$	t_{PLH3}		All	9, 10, 11	7	22	
Propagation delay time, LDCKA↑ or LDCKB↑ to AF/AEA or AF/AEB	t_{pd3}		All	9, 10, 11	7	18	
Propagation delay time, UNCKA↑ or UNCKB↑ to AF/AEA or AF/AEB	t_{pd4}		All	9, 10, 11	7	18	
Propagation delay time, $\overline{RSTA}$ low or $\overline{RSTB}$ low to AF/AEA or AF/AEB	t_{PLH4}		All	9, 10, 11	1	16	
Propagation delay time, LDCKA↑ or LDCKB↑ to HFA or HFB	t_{PLH5}		All	9, 10, 11	6	17	
Propagation delay time, UNCKA or UNCKB to HFA or HFB	t_{PHL4}		All	9, 10, 11	7	17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits 2/		Unit
					Min	Max	
Propagation delay time, $\overline{RSTA}$ low or $\overline{RSTB}$ low to HFA or HFB	t_{PHL5}	C_L = 50 pF minimum R_L = 500Ω See figure 3	All	9, 10,11	1	16	ns
Propagation delay time, SAB or SBA to B or A	t_{pd5} 6/		All	9, 10,11	1	12	
Propagation delay time, A or B to B or A	t_{pd6}		All	9, 10, 11	1	11	
Propagation delay time, output enable GBA or GAB to A or B	t_{en1}		All	9, 10, 11	1	10	
Propagation delay time, output disable, GBA or GAB to A or B	t_{dis1}		All	9, 10, 11	1	13	

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V_{IN} = GND or $V_{IN} \ge 3.0$ V.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at $4.5\ V \le V_{CC} \le 5.5$ V.

3/ For I/O ports, the limit includes the input leakage current from the input circuitry.

4/ Not more than one output should be tested at one time, and the duration of the test condition should not exceed one second.

5/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

6/ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Device type		01					
Case outlines		X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	$\overline{PENA}$	B11	$\overline{FULLB}$	F9	NC	K2	A11
A2	GBA	C1	GND	F10	B6	K3	GND
A3	SBA	C2	HFA	F11	GND	K4	V_{CC}
A4	LDCKA	C5	UNCKB	G1	A5	K5	GND
A5	V_{CC}	C6	NC	G2	GND	K6	A17
A6	V_{CC}	C7	V_{CC}	G3	A4	K7	GND
A7	V_{CC}	C10	HFB	G9	B4	K8	V_{CC}
A8	LDCKB	C11	GND	G10	GND	K9	GND
A9	SAB	D1	A1	G11	B5	K10	B10
A10	GAB	D2	A0	H1	A7	K11	B9
A11	$\overline{AF/AEB}$	D10	B0	H2	GND	L1	A10
B1	$\overline{FULLA}$	D11	B1	H10	GND	L2	A12
B2	AF/AEA	E1	A3	H11	B7	L3	A13
B3	$\overline{RSTA}$	E2	A2	J1	A8	L4	A14
B4	GND	E3	V_{CC}	J2	V_{CC}	L5	A16
B5	$\overline{EMPTYB}$	E9	V_{CC}	J5	A15	L6	B15
B6	UNCKA	E10	B2	J6	NC	L7	B16
B7	$\overline{EMPTYA}$	E11	B3	J7	B17	L8	B14
B8	GND	F1	A6	J10	V_{CC}	L9	B13
B9	$\overline{RSTB}$	F2	GND	J11	B8	L10	B12
B10	$\overline{PENB}$	F3	NC	K1	A9	L11	B11

FIGURE 1. Terminal connections.

Select-mode control table

All device types			
Control		Operation	
SBA	SAB	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
H	L	FIFO B to A bus	Real-time A to B bus
L	H	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

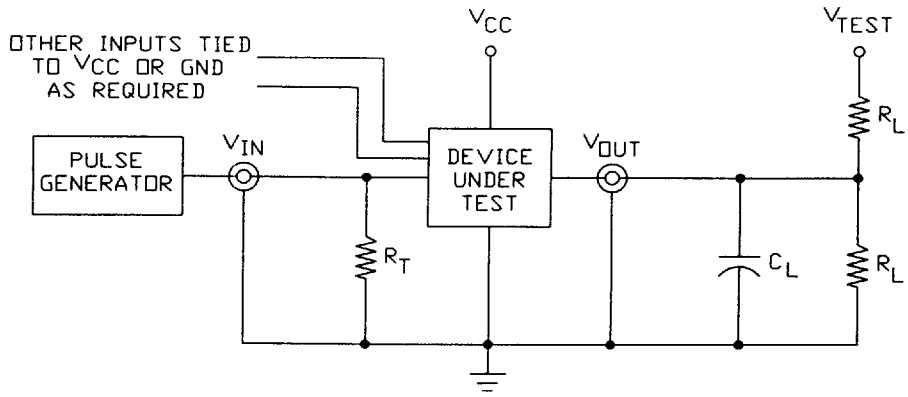
NOTE: H = High voltage level, L = Low voltage level.

Output-enable control table

All device types			
Control		Operation	
GBA	GAB	A BUS	B BUS
L	L	Isolation/Input to A bus	Isolation/input to B bus
H	L	A bus enabled	Isolation/input to B bus
L	H	Isolation/Input to A bus	B bus enabled
H	H	A bus enabled	B bus enabled

NOTE: H = High voltage level, L = Low voltage level.

FIGURE 2. Truth table.



NOTES:
1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 7.0 V.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent.
6. R_T = 50Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

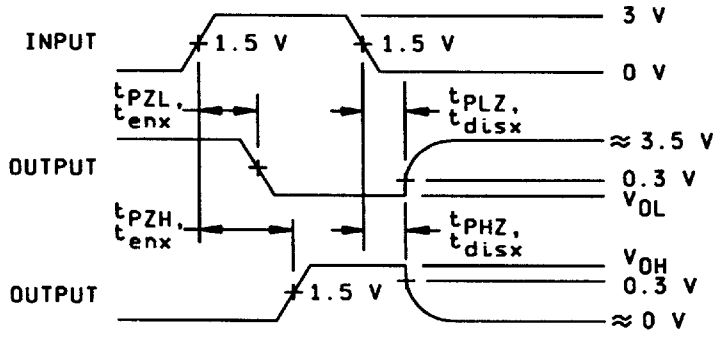
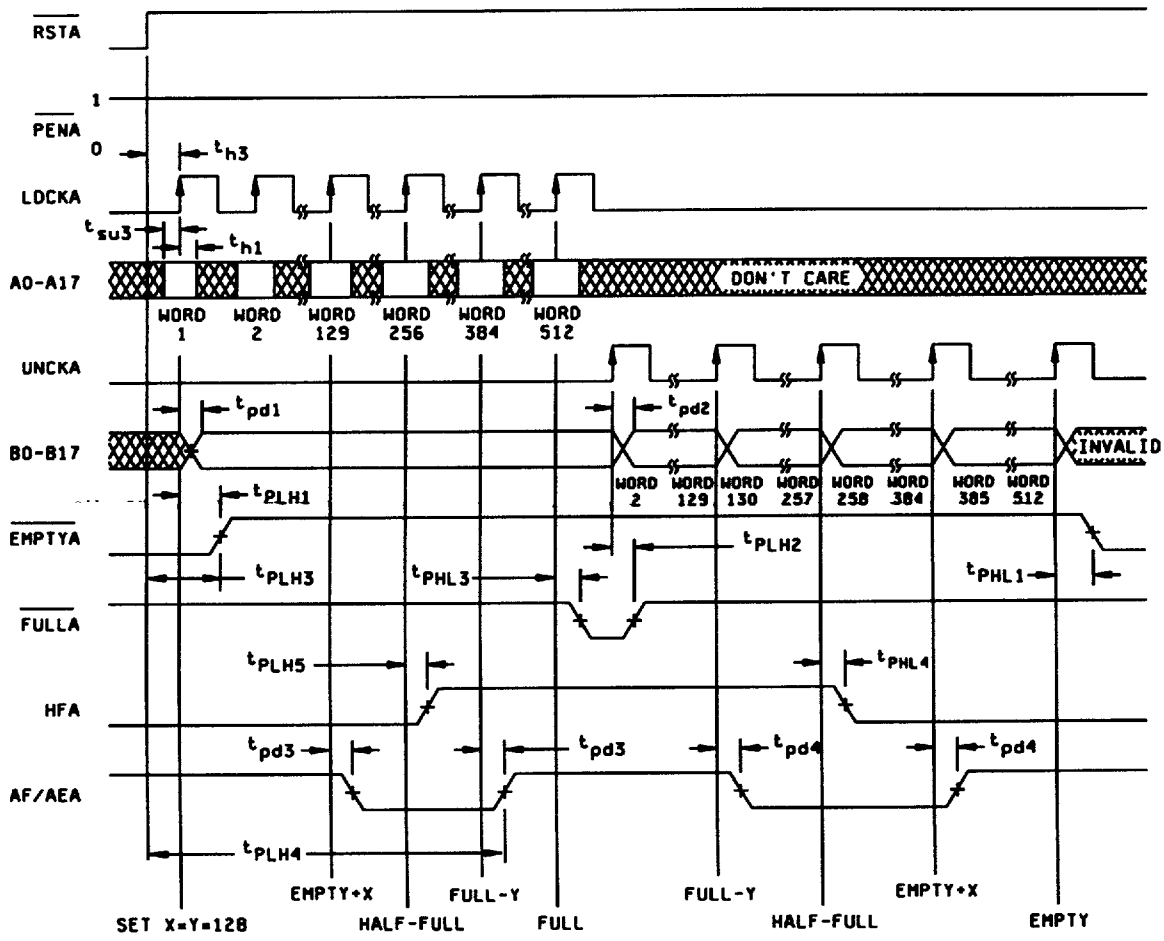


FIGURE 3. Switching waveforms and test circuit.

TIMING DIAGRAM FOR FIFO A 1/



1/ SAB = GAB = H, GBA = L; operation of FIFO B is identical to that of FIFO A.

FIGURE 3. Switching waveforms and test circuit - Continued.

PROGRAMMING X AND Y SEPARATELY FOR AF/AEA

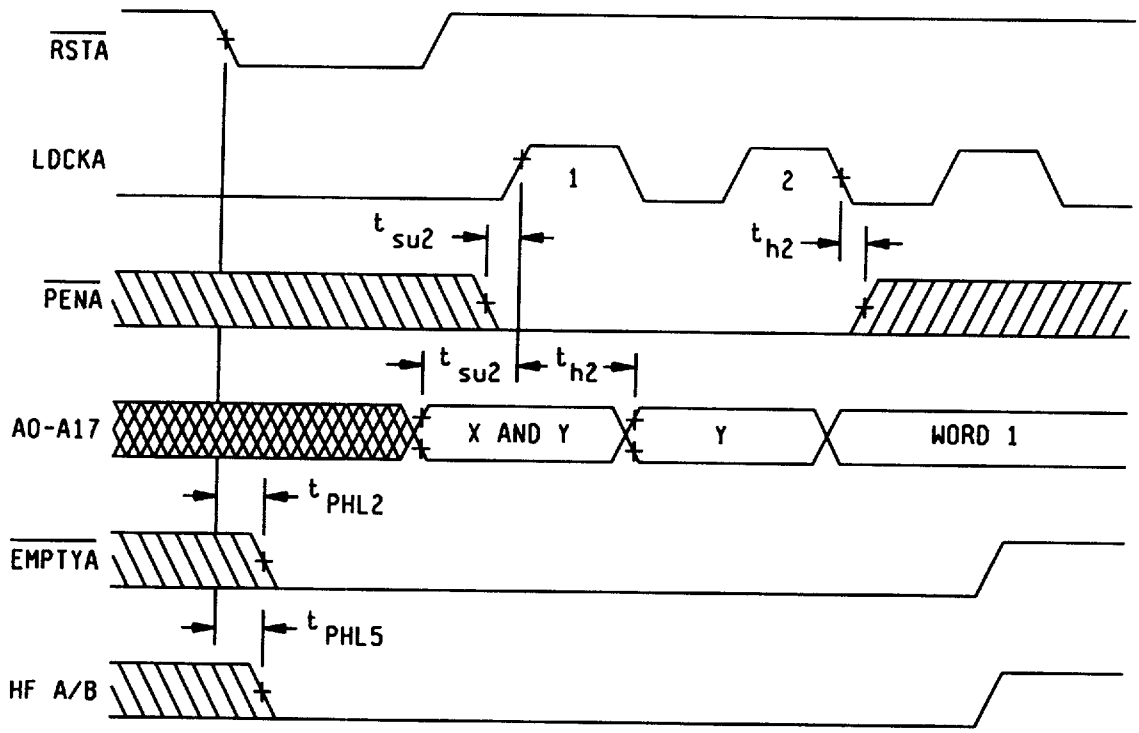


FIGURE 3. Switching waveforms and test circuit - Continued.

PULSE DURATION, SETUP, AND HOLD TIMING

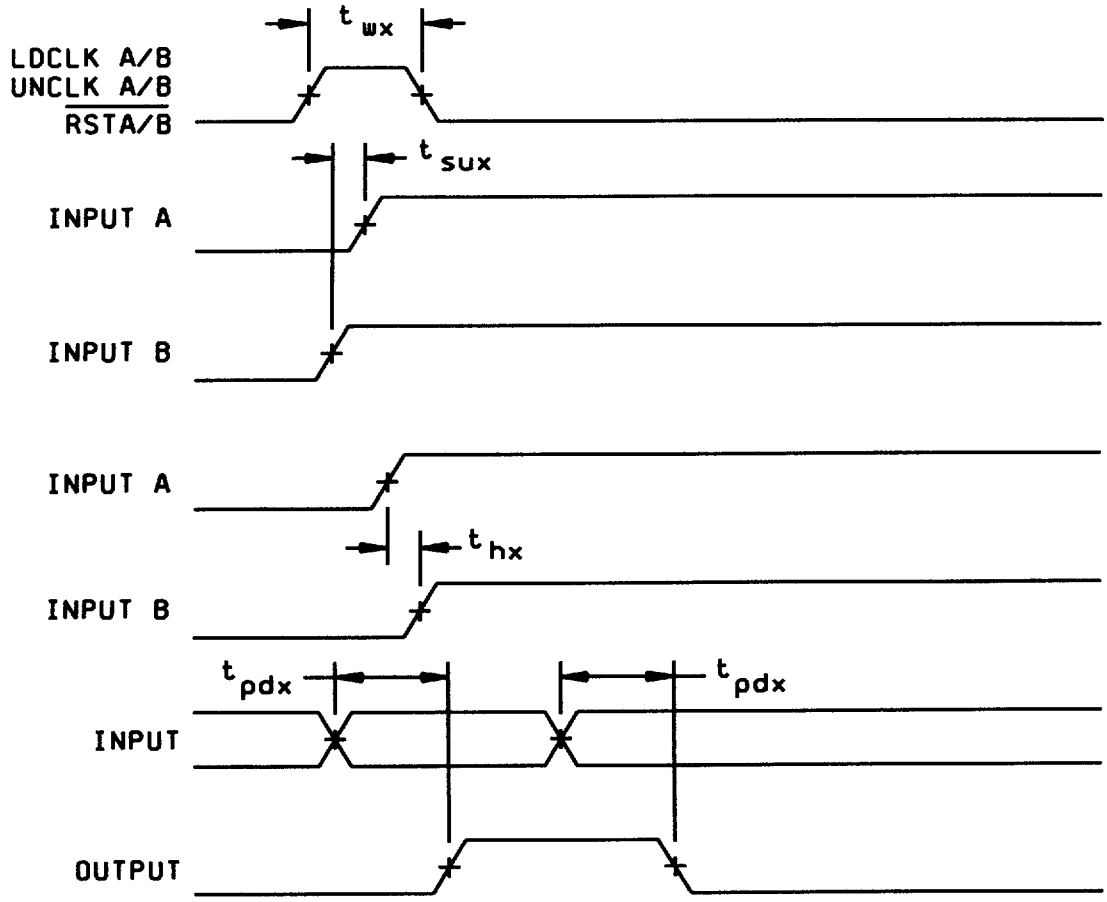


FIGURE 3. Switching waveforms and test circuit - Continued.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF 38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_I	±10%
I_{OZH}, I_{OZL}	±10%

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and $C_{I/O}$) shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and $C_{I/O}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN} and $C_{I/O}$, test all applicable pins on five devices with zero failures.

For C_{IN} and $C_{I/O}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN} and $C_{I/O}$ tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DESC-EC the device functions listed in each functional group and the test results for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and RHA levels for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, and as follows:

Terminal name	I/O	Description
A0-A17	I/O	Port-A data. A 18-bit bidirectional data port for side A.
AF/AEA	O	FIFO A almost-full/almost-empty flag. Depth offset values can be programmed for this flag, or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when FIFO A contains X or less words or (512 - Y) or more words. AF/AEA is set high after FIFO A is reset.
AF/AEB	O	FIFO B almost-full/almost-empty flag. Depth offset values can be programmed for this flag, or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when FIFO B contains X or less words or (512 - Y) or more words. AF/AEB is set high after FIFO B is reset.
B0-B17	I/O	Port-B data. A 18-bit bidirectional data port for side B.
$\overline{\text{EMPTYA}}$	O	FIFO A empty flag. $\overline{\text{EMPTYA}}$ is low when FIFO A is empty and high when FIFO A is not empty. $\overline{\text{EMPTYA}}$ is set low after FIFO A is reset.
$\overline{\text{EMPTYB}}$	O	FIFO B empty flag. $\overline{\text{EMPTYB}}$ is low when FIFO B is empty and high when FIFO B is not empty. $\overline{\text{EMPTYB}}$ is set low after FIFO B is reset.
$\overline{\text{FULLA}}$	O	FIFO A full flag. $\overline{\text{FULLA}}$ is low when FIFO A is full and high when FIFO A is not full. $\overline{\text{FULLA}}$ is set high after FIFO A is reset.
$\overline{\text{FULLB}}$	O	FIFO B full flag. $\overline{\text{FULLB}}$ is low when FIFO B is full and high when FIFO B is not full. $\overline{\text{FULLB}}$ is set high after FIFO B is reset.
GAB	I	Port-B output enable. B0-B17 outputs are active when GAB is high and in the high-impedance state when GAB is low.
GBA	I	Port-A output enable. A0-A17 outputs are active when GBA is high and in the high-impedance state when GBA is low.
HFA	O	FIFO A half-full flag. HFA is high when FIFO A contains 256 or more words and is low when FIFO A contains 255 or less words. HFA is set low after FIFO A is reset.
HFB	O	FIFO B half-full flag. HFB is high when FIFO B contains 256 or more words and is low when FIFO B contains 255 or less words. HFB is set low after FIFO B is reset.
LDCKA	I	FIFO A load clock. Data is written into FIFO A on a low-to-high transition of LDCKA when $\overline{\text{FULLA}}$ is high. The first word written into an empty FIFO A is sent directly to the FIFO A data outputs.
LDCKB	I	FIFO B load clock. Data is written into FIFO B on a low-to-high transition of LDCKB when $\overline{\text{FULLB}}$ is high. The first word written into an empty FIFO B is sent directly to the FIFO B data outputs.
$\overline{\text{PENA}}$	I	FIFO A program enable. After reset and before a word is written into FIFO A, the binary value on A0-A7 is latched as an AF/AEA offset value when $\overline{\text{PENA}}$ is low and LDCKA is high.
$\overline{\text{PENB}}$	I	FIFO B program enable. After reset and before a word is written into FIFO B, the binary value on B0-B7 is latched as an AF/AEB offset value when $\overline{\text{PENB}}$ is low and LDCKB is high.
$\overline{\text{RSTA}}$	I	FIFO A reset. A low level on $\overline{\text{RSTA}}$ resets FIFO A forcing $\overline{\text{EMPTYA}}$ low, HFA low, $\overline{\text{FULLA}}$ high, and AF/AEA high.
$\overline{\text{RSTB}}$	I	FIFO B reset. A low level on $\overline{\text{RSTB}}$ resets FIFO B forcing $\overline{\text{EMPTYB}}$ low, HFB low, $\overline{\text{FULLB}}$ high, and AF/AEB high.
SAB	I	Port-B read select. SAB selects the source of B0-B17 read data. A low level selects real-time data from A0-A17. A high level selects the FIFO A output.
SBA	I	Port-A read select. SBA selects the source of A0-A17 read data. A low level selects real-time data from B0-B17. A high level selects the FIFO B output.
UNCKA	I	FIFO A unload clock. Data is read from FIFO A on a low-to-high transition of UNCKA when $\overline{\text{EMPTYA}}$ is high.
UNCKB	I	FIFO B unload clock. Data is read from FIFO B on a low-to-high transition of UNCKB when $\overline{\text{EMPTYB}}$ is high.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-PRF-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings.	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.