



VTC Inc.
Value the Customer™

VM117/VM117R

6-CHANNEL, FERRITE HEAD READ/WRITE PREAMPLIFIER

July, 1991

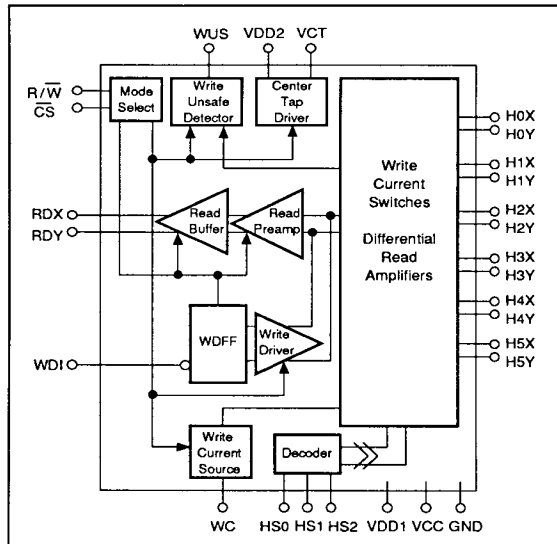
FEATURES

- Power Up/Down Write Protection
- Operates on +5V and +12V Power Supplies
- Programmable Write-Current Source
- TTL-Compatible Control Lines
- Write-Unsafe Detection Circuitry
- Low Input Noise
- For Use With Center-Tapped Ferrite Heads
- Optional Internal Head Damping Resistors
- Available in 2, 4 or 6 Channels

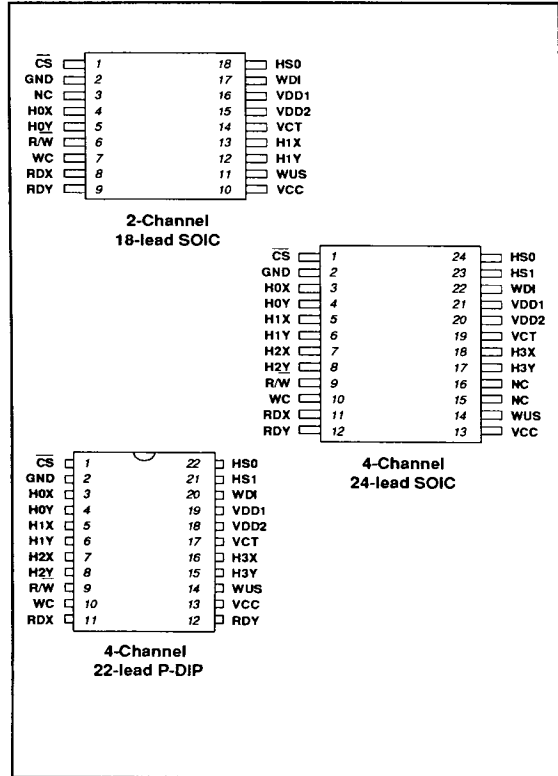
DESCRIPTION

The VM117/VM117R is a bipolar, monolithic read/write preamp circuit, designed for use with center-tapped ferrite recording heads. The circuit provides a low-noise read data path for signals from the disk in the read mode and provides write-current control for data written on the disk in the write mode.

BLOCK DIAGRAM



CONNECTION DIAGRAM



THREE-TERMINAL
READ/WRITE PREAMPS

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:

VDD1	-0.3V to 14V
VDD2	-0.3V to 14V
VCC	-0.3V to 6V

Pin Voltages:

Head Select (HS)	-0.3V to VCC + 0.3V
Write Unsafe (WUS)	-0.3V to VCC + 0.3V
Write Data Input (WDI)	-0.3V to VCC + 0.3V
Read/Write Select (R/W)	-0.3V to VCC + 0.3V

Output Current:

Write Current (IW)	60mA
Read Data (RDX, RDY)	10mA
Center Tap Current (ICT)	60mA
Write Unsafe (WUS)	12mA

Operating Temperature Range

Storage Temperature Range -65 to 150°C

Lead Temperature (Soldering 60 Sec.) 300°C

Junction Temperature 150°C

Thermal Characteristics,

18-lead PDIP	140°C/W
18-lead SOIC	140°C/W
22-lead PDIP	65°C/W
24-lead SOIC	80°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:

VDD1	12V ± 10%
VDD2	7.0V to VDD1
VCC	5V ± 10%

Head Inductance (LH) 10µH typical

Damping Resistance (RD) (Note 1) 750Ω

RCT Resistor (Note 2) 68Ω ± 5%

RDX, RDY Output Current (Read Mode) 0 to 100µA

Write Current 10 to 50mA

Junction Temperature 25° to +125°C

Note 1: VM117R has head damping resists placed on the chip; the standard value is 750Ω ± 20%.

Note 2: Resistor (RCT) used to limit power dissipation.
RCT (Ω) = 3.8/IW (A)

CIRCUIT OPERATION

The VM117/VM117R operates as a write-current switch in the write mode and as a low-noise differential amplifier in the read mode. Channel selection is controlled by HS0, HS1 and HS2 lines and mode select is controlled by the CS and R/W select lines. Both CS and R/W have internal pull-up resistors to prevent accidental write condition. Unsafe conditions are indicated by the WUS line.

Write Mode

In the write mode, the VM117/VM117R operates as a write-current switch. Write current is supplied by an internal current source. The magnitude of the write current is determined by an external resistor connected between WC and ground. The head current is switched between the X and Y side of a selected head by falling transitions on WDI (write data input). When switching to the write mode from the read mode, the write data flip-flop is initialized to pass head current through the X side of the head.

The write unsafe (WUS), open collector output, will give a high level for any of the following unsafe conditions:

- Open Head
- No Write Current
- Read Mode
- Idle Mode
- Write Data Frequency Too Low
- Head Center-Tap Open

After the fault condition is corrected, it takes two negative transitions on WDI to clear the WUS line.

Read Mode

In the read mode the circuit operates as a low-noise differential amplifier. The write-current source is turned off and the write-data flip-flop is set. The selected head provides a differential input. The RDX and RDY pins provide differential emitter follower outputs which are in phase with the X and Y inputs

Write current is deactivated for both the read and idle mode so that external gating is not required.

Head Select

One of the up to six heads may be selected in both the read and write modes. The selected head is determined by the voltage level of the head select inputs as shown in Table 1.

Mode Select

This circuit has three modes of operation: read, write and idle. The state of the chip select (CS) and the read write select (R/W) inputs determine the mode of operation as shown in Table 2.

Table 1: Head Select

HS0	HS1	HS2	HEAD
L	L	L	0
H	L	L	1
L	H	L	2
H	H	L	3
L	L	H	4
H	L	H	5
X	H	H	None

Table 2: Mode Select

CS	R/W	MODE
L	L	Write
L	H	Read
H	X	Idle

Table 3: External Resistor vs. Write Current

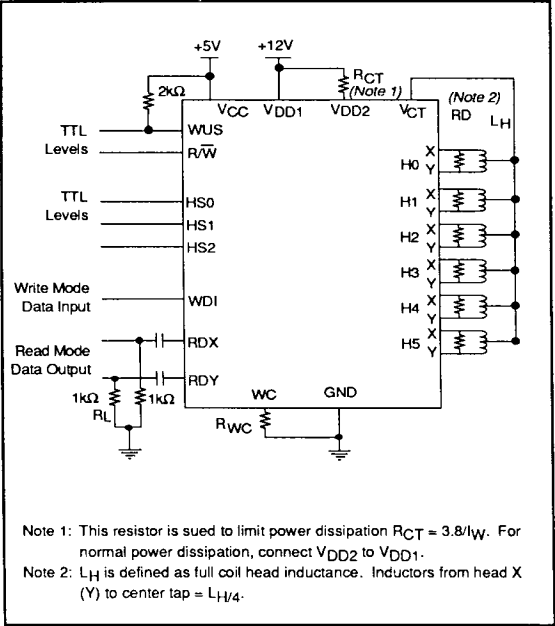
External resistor vs. DC write current I_W into the selected head terminal X or Y with V_{CT} shorted only to the respective X or Y terminal.	
External Resistor $R_{WC} (\Omega)$	Write Current $I_W (mA)$
14.810	10
7.205	20
4.753	30
3.517	40
3.111	45
2.786	50

Note: Effective current I_{FLUX} generated in the magnetic head is related to I_W by the expression:

$$I_{FLUX} = I_W \left(\frac{R_D}{R_H + R_D} \right)$$

Where R_H equals the full coil resistance of a center-tapped ferrite head and R_D is the damping resistor connected internally or externally between the X and Y terminals. Nominal internal resistance on VM117R is 750Ω.

TYPICAL APPLICATION



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DC CHARACTERISTICS Unless otherwise specified, $V_{DD1} = V_{DD2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $T_A = 25^{\circ}C$.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Positive Supply Current	I _{DD}	Read Mode			40	mA
		Write Mode			26 + I _W	
		Idle Mode			25	
	I _{CC}	Read Mode			15	mA
		Write Mode			18	
		Idle Mode			15	
Power Supply Dissipation T _A = 70°C	P _D	Idle Mode		325	610	mV
		Read Mode		200	412	
		Write Mode I _W = 50mA, R _{CT} = 76Ω		675	850	
		Write Mode I _W = 50mA, R _{CT} = 0Ω		850	1100	
DIGITAL TTL INPUTS: CS, R/W, HS, WDI						
Input High Voltage	V _{IH}		2		V _{CC} + 0.3	V
Input Low Voltage	V _{IL}		-0.3		0.8	V
Input High Current	I _{IH}	V _{IH} = 2.0V, V _{CC} = 5.5V	-400		100	μA
Input Low Current	I _{IL}	V _{IL} = 0.4V, V _{CC} = 5.5V	-0.4			mA
WUS OUTPUT						
Low Voltage	V _{OL}	I _{OL} = 8 mA (Safe)			0.5	V
High Current	I _{OH}	V _{OH} = 5V (Unsafe)			100	μA
HEAD CENTER TAP VOLTAGES						
Read Mode	V _{CT}	Read Mode		4.2		V
Write Mode	V _{CT}	Write Mode		6.6		V

THREE-TERMINAL
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READ CHARACTERISTICS Unless otherwise specified, $V_{DD1} = V_{DD2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ C$.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain	A _V	V _{IN} = 1mV _{rms} , f = 500KHz R _L (RDX,RDY) = 1KΩ	80		120	V/V
Dynamic Range	DR	DC input voltage where AC gain falls 10%, V _{IN} = V _{DC} + 0.5mV _{p-p} f = 500KHz	-2		2	mV
Bandwidth (- 3dB)	BW	V _{IN} = 1 mV _{p-p} , Z _S < 5Ω	30			MHz
Input Noise Voltage	e _{in}	L _H = 0, R _H = 0, BW = 15MHz		1.1	1.6	nV/√Hz
Differential Input Capacitance	C _{IN}	f = 5MHz			23	pF
Differential Input Resistance	R _{IN}	VM117	2			KΩ
		VM117R		750		Ω
Input Current (per side)	I _{IN}				45	μA
Common Mode Rejection Ratio	CMRR	V _{CM} = V _{CT} + 100mV _{p-p} , f = 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	V _{DD} or V _{CC} = 100mV _{p-p} , f = 5MHz	45			dB
Channel Separation	CS	V _{IN} = 100mV _{p-p} , f = 5MHz Three channel driven, selected channel measured	45			dB
Output Offset Voltage	V _{OS}		-400		400	mV
Common Mode Output Voltage	V _{OCM}		5		7	V
Head Center Tap Voltage	V _{CT}			4.2		V
Single-Ended Output Resistance	R _{SEO}				30	Ω

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WRITE CHARACTERISTICS Unless otherwise specified, $V_{DD1} = V_{DD2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ C$, I_W = 40mA, L_H = 2.5μH, R_D = 750Ω, f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Write Current Range	I _W	(See table 3)	10		50	mA
Differential Head Voltage	V _{DH}			8		V _{pk}
Unselected Head Current	I _{UH}				2	mA p-p
Current Gain	A _I			20		mA/mA
Head Current Propagation Delay	t _{PD}	L _H = 0μH, R _H = 0, 50% WDI to 50% I _W			30	ns
Rise/Fall Time	t _r , t _f	L _H = 0μH, R _H = 0, 10% to 90%		5	20	ns
Symmetry	S	[(t _r - t _f)/2]		0.5	2	ns
Write Current Tolerance	ΔI _W	R _{WC} = 3111Ω	42.75	45	47.25	mA
Differential Output Resistance	R _{OUT}	VM117	10			KΩ
		VM117R		750		Ω
Differential Output Capacitance	C _{OUT}	f = 5MHz			15	pF

SWITCHING CHARACTERISTICS Unless otherwise specified, $I_W = 40\text{mA}$, $L_H = 2.5\mu\text{H}$, $R_D = 750\Omega$, $f_{\text{DATA}} = 5\text{MHz}$, $C_L (\text{RDX}, \text{RDY}) \leq 20\text{pF}$, $T_A = 25^\circ\text{C}$.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Read-to-Write Switching Delay	t_{RW}	50% of $\overline{\text{R/W}}$ to 90% of write output envelope			1	μs
Write-to-Read Switching Delay	t_{WR}	50% of $\overline{\text{R/W}}$ to 90% of 100mVp-p RDX, RDY envelope			1	μs
Idle-to-Write Switching Delay	t_{IW}	50% of $\overline{\text{CS}}$ to 90% of write output envelope			1	μs
Idle-to-Read Switching Delay	t_{IR}	50% of $\overline{\text{CS}}$ to 90% of 100mVp-p RDX, RDY envelope			1	μs
Write-to-Idle Switching Delay	t_{WI}	50% of $\overline{\text{CS}}$ to 10% of write output envelope			1	μs
Read-to-Idle Switching Delay	t_{RI}	50% of $\overline{\text{CS}}$ to 10% of RDX, RDY envelope			1	μs
Head Select Switching Delay	t_{HS}	50% of HS transition to 90% of 100mVp-p RDX, RDY envelope from selected head			1	μs
Write Unsafe Delay Safe to Unsafe	t_{D1}	Gate WDI. Measure from 50% of last data pulse to 50% WUS. $I_W = 10$ to 40mA	1.6		8	μs
Write Unsafe Delay Unsafe to Safe	t_{D2}	Gate WDI. Measure from 50% of falling edge of first data pulse to 50% WUS, $I_W = 10\text{mA}$			1	μs

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