IRPLLED1

IRPLLED1 High Voltage LED Driver using the IRS2540

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1. Introduction

As the industry becomes more power conscious to compensate for increasing energy costs and to meet governmental regulations, new innovative ways of conserving energy are being developed. For the lighting industry one of these outlets has been LEDs. Due to their longevity, robust design, low maintenance and high efficiency, they have proven to be a viable alternative to less efficient light sources. With their long term projected falling cost and further increased efficiency, the industry has eagerly embraced LEDs and put them in high demand. LEDs require drivers that have specific features such as constant current control over the temperature and manufacturing variations of LEDs, dimming, and appropriate fault protections. The IRS254(0,1) is specifically designed to address these requirements

The IRPLLED1 evaluation board is a high voltage LED driver designed to operate on an input DC voltage of 40 V to 170 V and supply a programmable load current of 350 mA, 700 mA, 1 A, or 1.5 A. The output voltage is also clamped at 30 V by the external open-circuit-protection circuitry, which can easily be disabled or reconfigure as explained in this reference design. However the output voltage should not exceed the ratings of the external components mounted on the board; higher voltage when optimized components are utilized in the design. IRPLLED1 uses the IRS254(0,1), a high voltage, high frequency buck control IC for constant LED current regulation. The IRS254(0,1) controls the average load current by a continuous mode time-delayed hysteretic method using an accurate on chip band gap voltage reference. The 8-pin, 200 V (600 V) rated IRS2540 (IRS2541) inherently provides short-circuit protection, with open-circuit protection incorporated by a simple external circuit and has full dimming capabilities. The IRS254(0,1) allows scalable designs to accommodate series and parallel configurations of LEDs, for today's production LEDs as well as new generation higher current LEDs, and provides high current control accuracy over input and output voltage.

The evaluation board documentation will briefly describe the functionality of IRS254(0,1), discuss the selection of the output stage, of the switching components, and of the surrounding circuitry. This board was tested with a single Lumileds™ flood board for the 350 mA and 700 mA settings, and two Lumileds flood boards in parallel for the 1 A and 1.5 A settings. Lumileds flood boards are available through Future Electronics and have a max nominal current rating of 700 mA with a breakdown voltage between 16 V and 24 V. This demo board can operate off of a 120 V AC rectified line with the addition of a proper rectifying circuit.

2. Constant current control

The IRS254(0,1) is a time-delayed hysteretic buck controller. During normal operating conditions the output current is regulated via the IFB pin voltage, nominal value of 500 mV. This feedback is compared to an internal high precision band gap voltage reference. An on-board dV/dt filter has also been used to prevent erroneous transitioning.

Once the supply to the chip reaches V_{CCUV+}, the LO output is held high and the HO output is low for a predetermined period of time. This initiates the charging of the bootstrap capacitor, establishing the V_{BS} floating supply for the high-side output. Then the chip begins toggling HO and LO outputs as needed to regulate the current. The deadtime of approximately 140 ns between the LO and HO gate drive signals prevents "shoot-through" and reduce switching losses, particularly at higher frequencies.

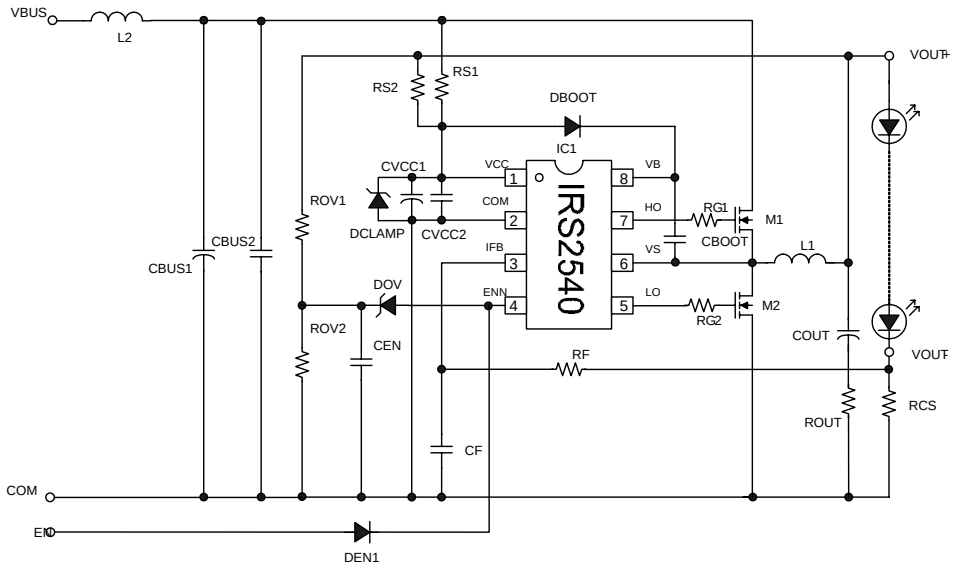


Fig. 1: IRS254(0,1) Constant Current LED Driver Typical Schematic
(see Fig. 16 for evaluation board schematic)
Note: R_{out} is needed only in few applications

Under normal operating conditions, if V_{IFB} is below V_{IFBTH}, HO is on and the load is receiving current from V_{BUS}. This simultaneously stores energy in the output stage, L_1 and C_{OUT}, whilst V_{IFB} begins to increase. Once V_{IFB} crosses V_{IFBTH}, HO switches off after the delay $t_{HO,off}$. Once HO is off, LO will turn on after the deadtime, the inductor and output capacitor release the stored energy into the load and V_{IFB} starts decreasing. When V_{IFB} crosses V_{IFBTH} again, LO switches off after the delay $t_{LO,off}$ and HO switches on after the delay $t_{HO,on}$.

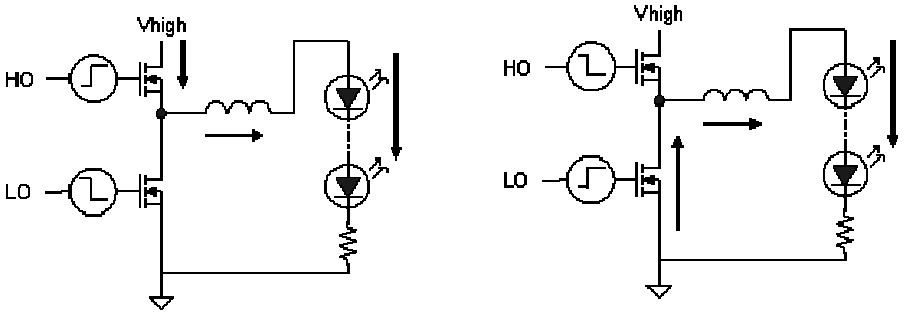


Fig. 2: (A) Storing Energy in Inductor
(B) Releasing Stored Inductor Energy

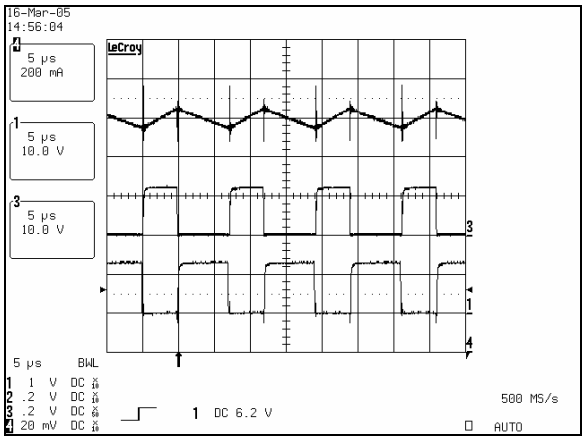


Fig. 3: IRS254(0,1) Control Signals, I_{avg}=1.2 A

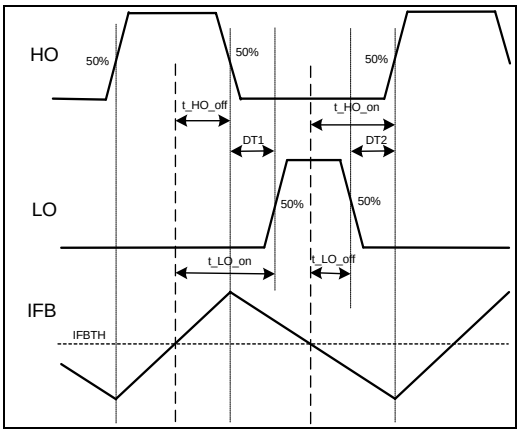


Fig. 4: IRS254(0,1) Time Delayed Hysteresis

The switching continues to regulate the current at an average value determined as follows: when the output combination of L_1 and C_{OUT} is large enough to maintain a low ripple on I_{FB} (approximately less than 100 mV), $I_{out(avg)}$ can be calculated:

$$Iout(avg) = VIFBTH \big/ RCS$$

Having load current programmable from 350 mA to 1.5 A, series and parallel combinations of resistors must be used to properly set the current, as well as distribute power accordingly. Equivalent resistances for each current setting were calculated as follows:

$$R_{350mA} = \frac{0.5\,V}{350\,mA} = 1.43\,\Omega$$

$$R_{700mA} = \frac{0.5\,V}{700\,mA} = 0.71\,\Omega$$

$$R_{1A} = \frac{0.5\,V}{1\,A} = 0.5\,\Omega$$

$$R_{1.5A} = \frac{0.5\,V}{1.5\,A} = 0.33\,\Omega$$

Since some of these equivalent values of resistance are not available, series and parallel combinations are used, and they are specified as follows (all combinations use standard value resistors: 1.43 Ω, 0.56 Ω, and 0.47 Ω):

$$R_{350mA} = 1.43\,\Omega$$

$$R_{700mA} = 0.71\,\Omega \approx (1.43\,\Omega \,||\, 1.43\,\Omega) = 0.715\,\Omega$$

$$R_{1A} = 0.5\,\Omega \approx (0.47\,\Omega + 0.56\,\Omega) \,||\, (0.47\,\Omega + 0.56\,\Omega) = 0.515\,\Omega$$

$$R_{1.5A} = 0.33\,\Omega \approx (0.47\,\Omega + 0.56\,\Omega) \,||\, (0.47\,\Omega + 0.56\,\Omega) \,||\, (0.47\,\Omega + 0.56\,\Omega) = 0.343\,\Omega$$

Although some of the series and parallel combinations do not yield the exact resistance needed, for all tolerance purposes, they are accurate enough. For this evaluation board, an extremely tight current regulation was achieved with a worst case result of ±1.2% for the 350 mA setting as the bus voltage was swept from 40 V to 170 V. Likewise a precise regulation of ±0.25% was maintained for a varying load voltage from 16 V to 24 V for the 350 mA current setting.

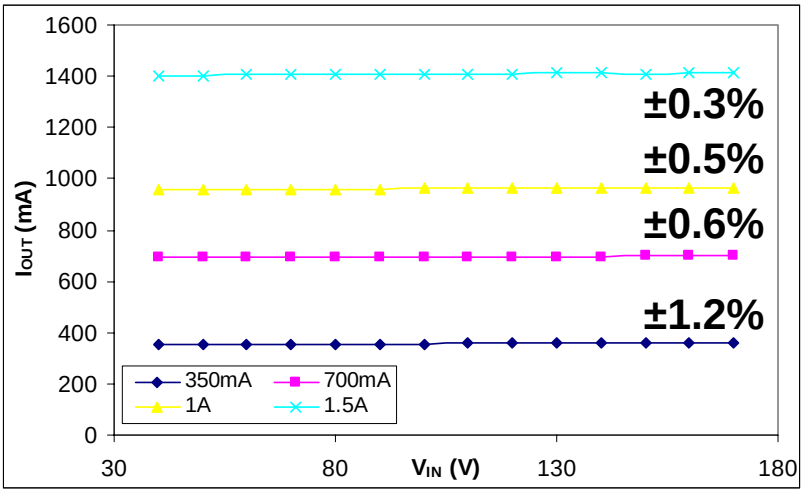


Fig. 5: V_{out} = 16 V, L_1 = 470 µH, C_{OUT} = 33 µF

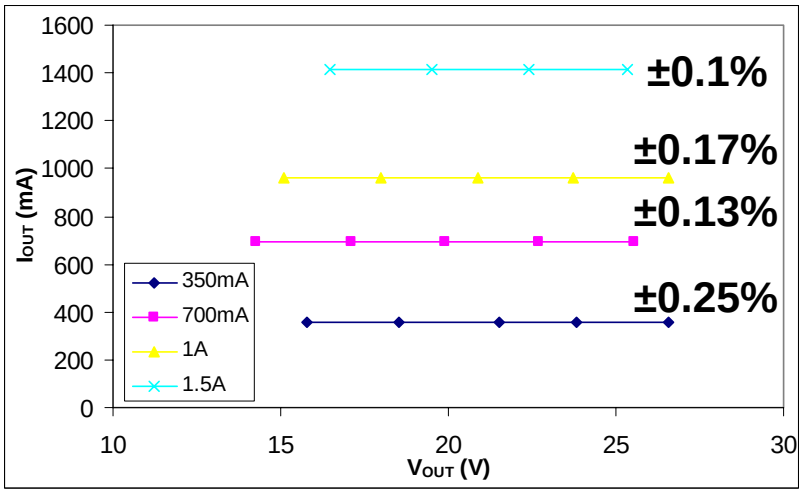


Fig. 6: V_{bus} = 100 V, L_1 = 470 µH, C_{OUT} = 33 µF

3. Frequency selection

The frequency in the IRS254(0,1) is free running and maintains current regulation by quickly adapting to changes in input and output voltages. There is no need for additional external components to set the frequency as seen with most oscillators, resulting in a part reduction. The frequency is determined by L_1 and C_{OUT}, as well as the input/output voltages and load current. The selection of the frequency will be a trade-off between system efficiency, current control regulation, size, and cost.

The higher the frequency, the smaller and lower the cost of L_1 and C_{OUT}, the higher the ripple, the higher the FET switching losses, which becomes the driving factor as V_{BUS} increases to higher voltages, the higher the component stresses and the harder it is to control the output current.

With an input voltage as high as 170 V, the targeted frequency was determined to be between 50 kHz and 75 kHz. Within this operating spectrum all components can easily handle their associated power losses.

4. Output L_1 and C_{OUT} selection

To maintain tight hysteretic current regulation L_1 and C_{OUT} need to be large enough to maintain the supply to the load during $t_{HO,on}$ and avoid significant undershooting of the load current, which in turn causes the average current to fall below the desired value.

First, we are going to look at the effect of the inductor when there is no output capacitor to clearly demonstrate the impact of the inductor. In this case, the load current is identical to the inductor current. Figure 7 shows how the inductor value impacts the frequency over a range of input voltages. As can be seen, the input voltage has a great impact on the frequency and the inductor value has the greatest impact at reducing the frequency for smaller input voltages.

Figure 8 shows how the variation in load current increases over a span of input voltage, as the inductance is decreased. Figure 9 shows the variation of frequency over different output voltages and different inductance values. Finally Fig. 10 shows how the load current variation increases with lower inductance over a range of output voltages.

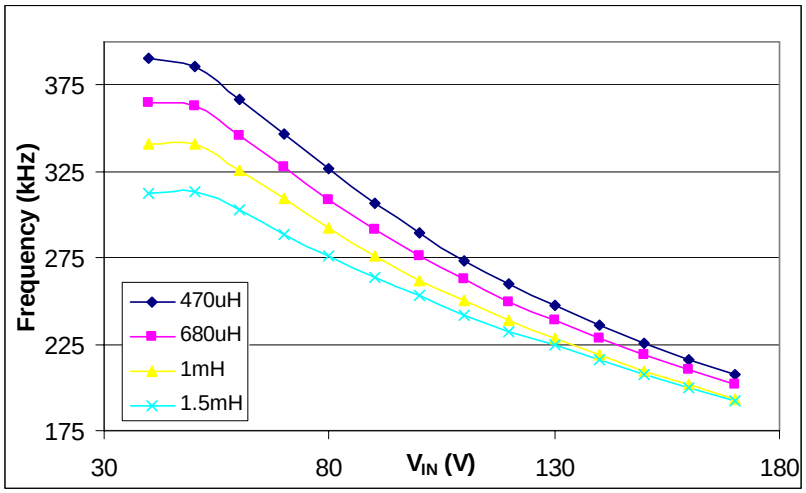


Fig. 7: I_{out} = 350 mA, V_{out} = 16.8 V, C_{OUT} = 0 µF

The output capacitor can be used simultaneously to achieve the target frequency and current control accuracy. Figure 11 shows how the capacitance reduces the frequency over a range of input voltage. A small capacitance of 4.7 µF has a large effect on reducing the frequency. Figure 12 shows how the current regulation is also improved with the output capacitance. There is a point at which continuing to add capacitance no longer has a significant effect on the operating frequency or current regulation, as can be seen in Figs. 12 & 13.

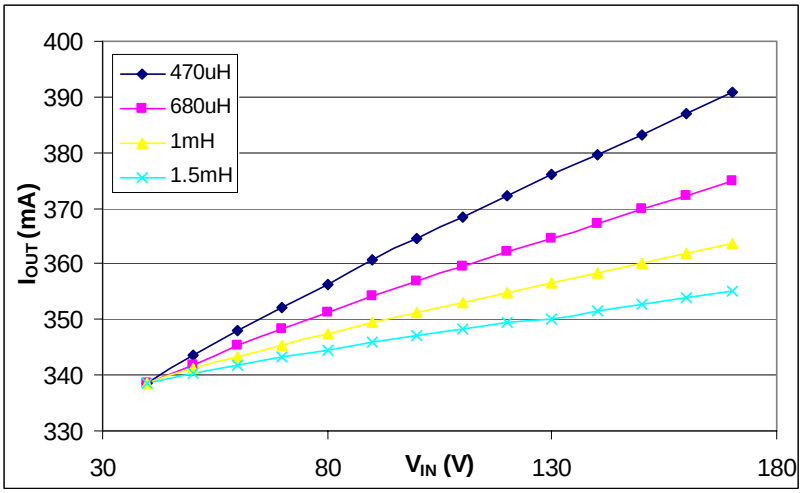


Fig. 8: I_{out} = 350 mA, V_{out} = 16.8 V, C_{OUT} = 0 µF

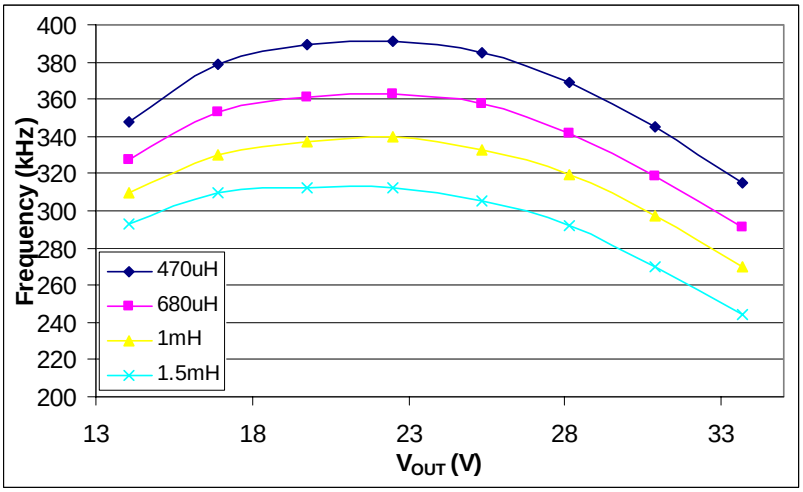


Fig. 9: I_{out} = 350 mA, V_{in} = 50 V, C_{OUT} = 0 µF

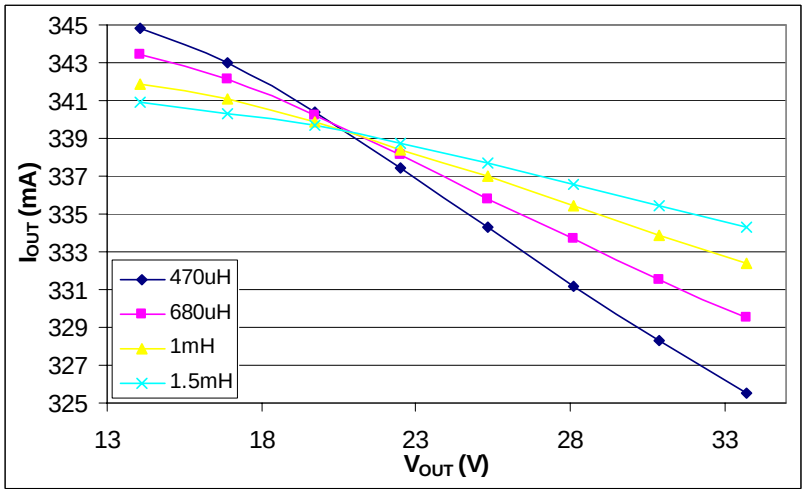


Fig. 10: I_{out} = 350 mA, V_{in} = 50 V, C_{OUT} = 0 µF

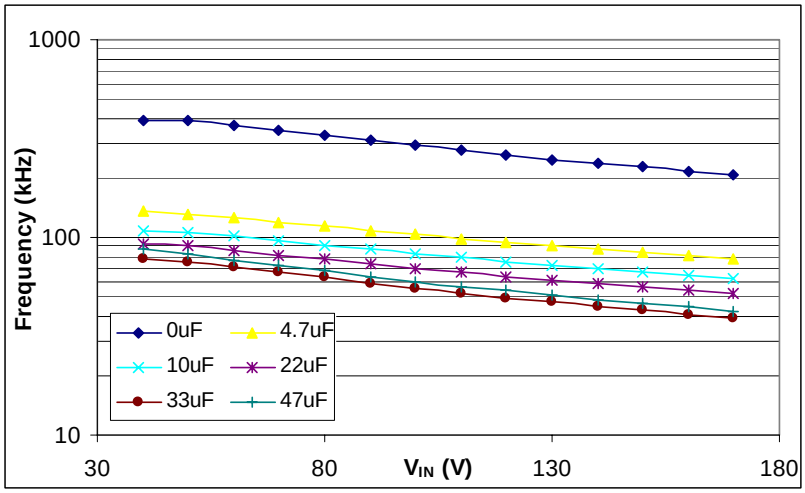


Fig. 11: I_{out} = 350 mA, V_{out} = 16.8 V, L = 470 µH

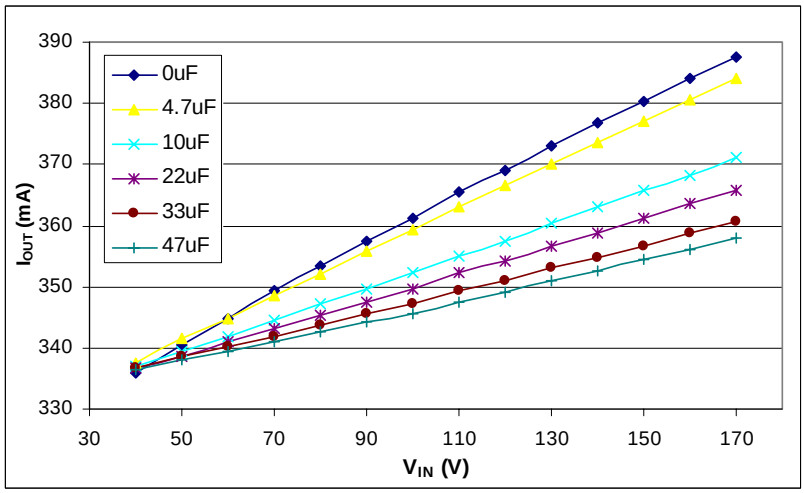


Fig. 12: I_{out} = 350 mA, V_{out} = 16.8 V, L = 470 µH

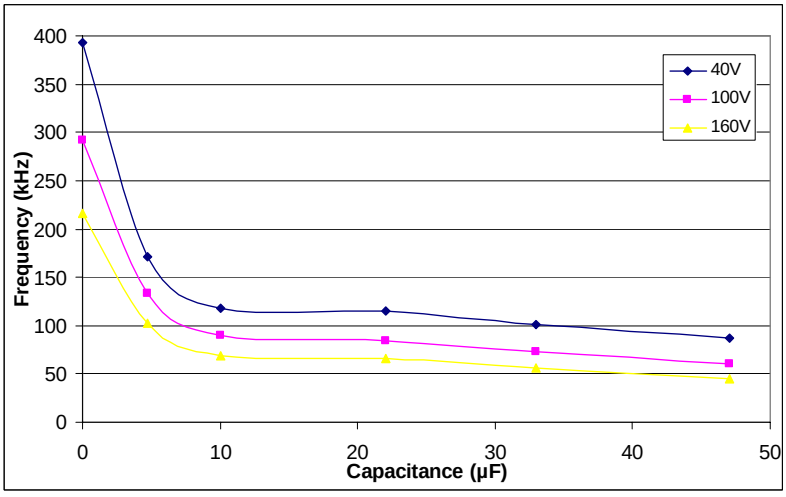


Fig. 13: I_{out} = 350 mA, V_{out} = 16.8 V, L = 470 µH

The addition of the C_{OUT} is essentially increasing the amount of energy that can be stored in the output stage, which also means it can supply current for an increased period of time. Therefore by slowing down the di/dt transients in the load, the frequency is effectively decreased.

With the C_{OUT} capacitor, the inductor current is no longer identical to that seen in the load. The inductor current will still have a perfectly triangular shape, where as the load will see the same basic trend in the current, but all sharp corners will be rounded with all peaks significantly reduced, as can be seen in Figs. 14 & 13.

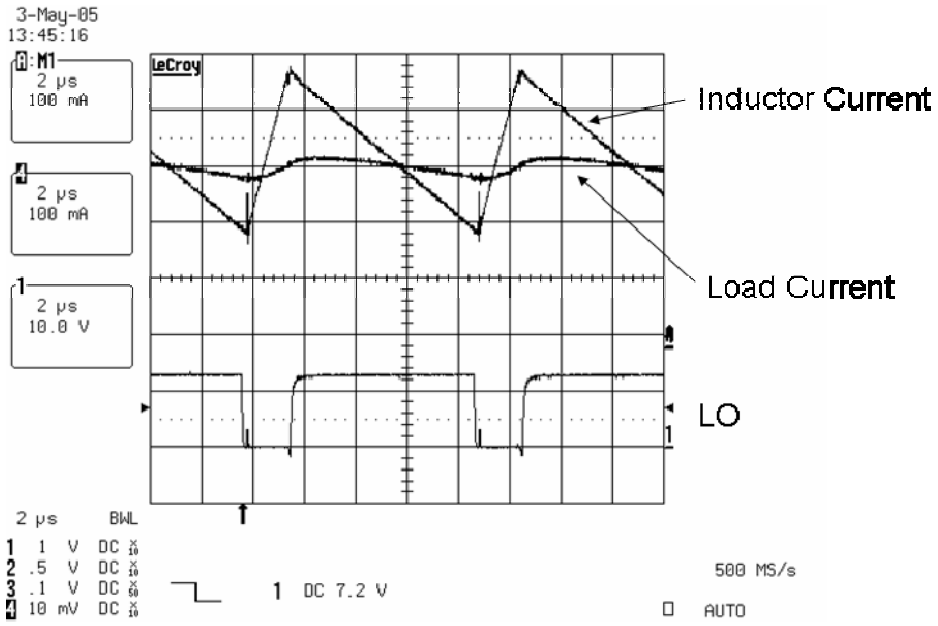


Fig. 14: I_{out} = 350 mA, V_{in} = 100 V, V_{out} = 16.85 V, L = 470 µH, C_{OUT} = 33 µF

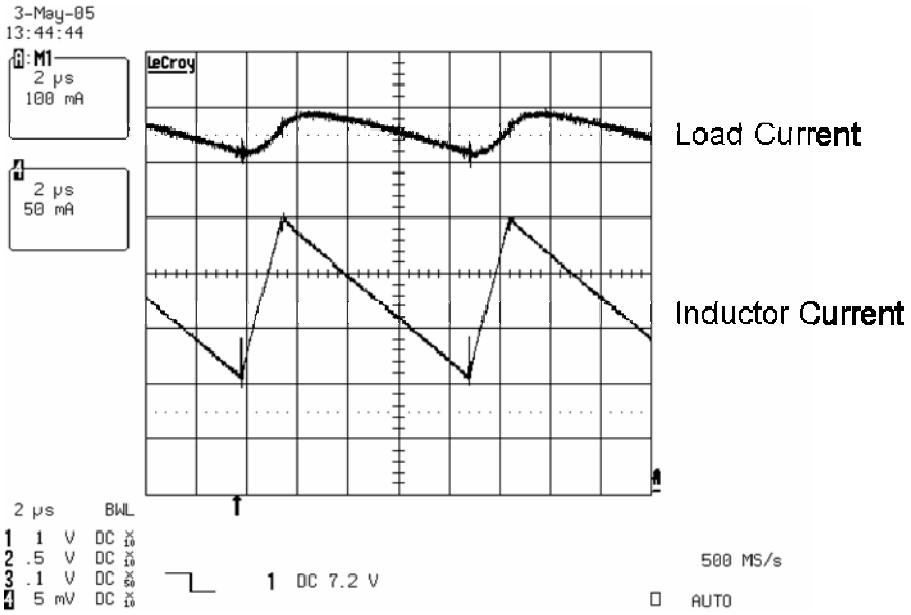


Fig. 15: I_{out} = 350 mA, V_{in} = 100 V, V_{out} = 16.85 V, L = 470 µH, C_{OUT} = 33 µF

L_1 and C_{OUT} need to be chosen so that it stores enough energy to supply the load during $t_{HO,on}$ while maintaining current control accuracy. A lower value of L_1 will require a larger value of C_{OUT}.

Since this evaluation board is designed to handle a load current only as high as 1.5 A, off the shelf inductors are available. Instead, to minimize or eliminate any effects of eddy currents, a custom inductor for this application was designed by VOGT. High value (in the order of 1 mH or more) inductors that can handle this amount of current are not readily available and tend to be bulky and costly. With too small of an inductor (in the order of 100 µH or less), the C_{OUT} capacitor would need to be in the order of hundreds of micro farads to maintain good current regulation. Additionally, with a smaller inductance, the ripple current seen by the capacitor would be quite large, shortening the life of the capacitor, if an electrolytic were used.

Because of these considerations an inductor of 470 µH and an output capacitance of 33 µF were chosen to accommodate the 1.5 A load current. The current ripple associated with 470 µH is relatively small, so the board can be operated with or without output capacitance at the lower current ratings.

5. FET vs. diode for the low-side switch

The IRS254(0,1) has been designed so that it can drive a low-side FET and a high-side FET. If the use of two FETs for the half-bridge proves to be a cost issue, the low-side FET can be replaced by a freewheeling diode as shown in Fig. 16. Of course this may yield a lower cost system, but there are some efficiency tradeoffs to be considered, particularly for higher load currents. The system efficiency is directly influenced by several system parameters including operating frequency, load current, and input voltage.

A major parameter to consider is the reverse recovery time of the diode in comparison to the body diode of the FET it replaces. The diode intrinsically has a much shorter reverse recovery time since the device is specifically designed for this, where as the body diode is a parasitic element that originates from basic processing technology and typically has inferior characteristics, in terms of forward drop, reverse recovery, and power handling capabilities.

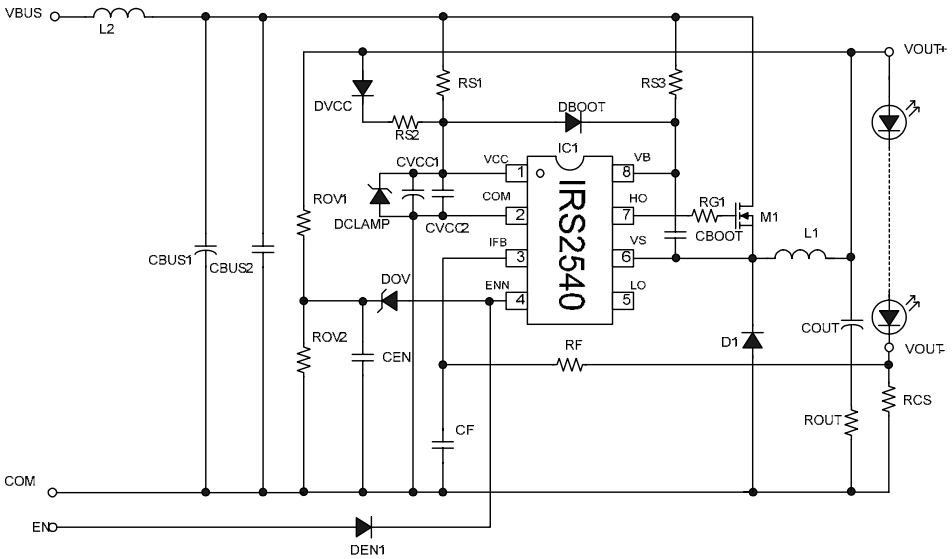


Fig. 16: Alternate IRS254(0,1) Time-Delayed Hysteretic Controlled Evaluation Board Schematic
Note: R_{out} is needed only in few applications

The reverse recovery problem is incurred during the deadtime after the low-side FET has been on and conducting current. During this deadtime the low-side FET is off, but the body diode is freewheeling and providing current to the load. Since the body diode is conducting current, carriers are present and will eventually need to be recombined, leading to reverse recovery. When the high-side FET turns on, the V_S node is almost instantly pulled from COM to V_{BUS} and the low-side FET or the freewheeling diode conducts current from V_S to ground due to the reverse recovery effect, potentially resulting in large power losses, overheating of the low-side switching component and component stress, as can be seen in Figs. 17 & 18. Since the power diode has a much shorter reverse recovery time, the diode will conduct current for a significantly shorter period and have lower power losses. At lower frequency and lower load current, the long recovery time associated with the FET body diode may not be an issue. For higher frequency higher current applications, a diode could provide lower power losses with respect to a FET.

In the evaluation board, the reverse recovery current peaks using a low-side FET would be on the order of 8 A, which puts a lot of stress on the components, not to mention the increased operating temperature. By replacing the low-side FET with an appropriate freewheeling diode, the reverse recovery peaks can be reduced and limited to 4.5 A. The frequency was also selected to keep the diode reverse recovery associated power losses low.

With the inclusion of a freewheeling diode instead of a low-side FET there is a need for R_{S3} and D_{VCC}. Without an initial pulse to come from LO establishing a ground reference for C_{BOOT} to charge, an alternate ground reference must be established. There are two paths that could potentially serve this role, one is through R_{S2} and the other is through the open-circuit components, R_{OV1} and R_{OV2}. The most versatile path is through R_{OV1} and R_{OV2} since there are no constraints along this path tied to the chip's turn on threshold. By making these two resistors, that are already serving function to the circuit, a bit smaller, the capacitor now has a low resistive path for which to charge. R_{S3} allows this charging path to exist without any interference from the chip V_{CC}, likewise D_{VCC} also allows this path to remain isolated. As the bus voltage is increased, the path will allow C_{BOOT} to fully charge and remain charged until the chip comes out of UVLO. At which time the self powering feature will take over after the first pulse from HO, and the ground reference will then be created by the freewheeling diode.

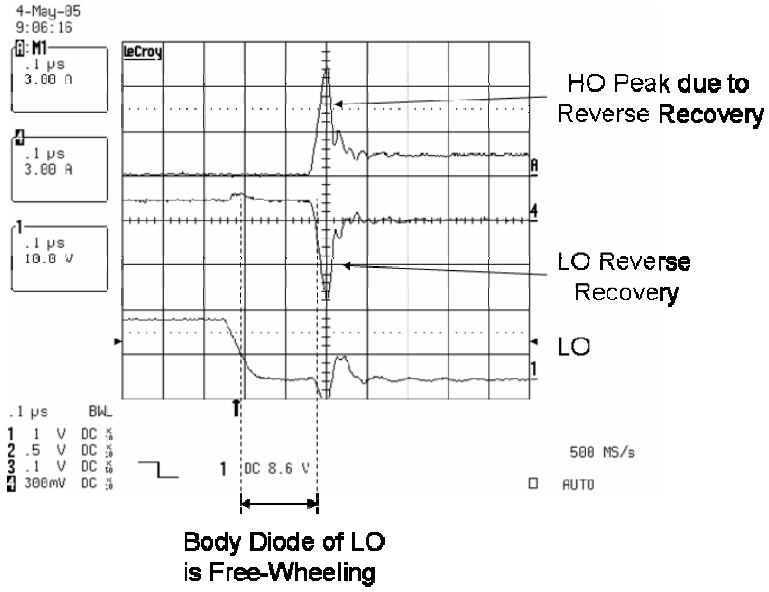


Fig. 17: Using a low-side FET, V_{in} = 100 V, I_{out} = 1.5 A, V_{out} = 17 V

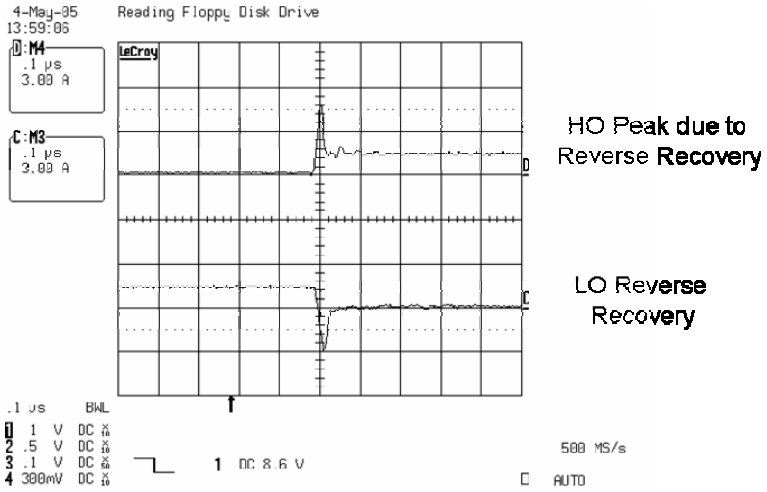


Fig. 18: Using a diode on the low-side, V_{in} = 100 V, I_{out} = 1.5 A, V_{out} = 17 V

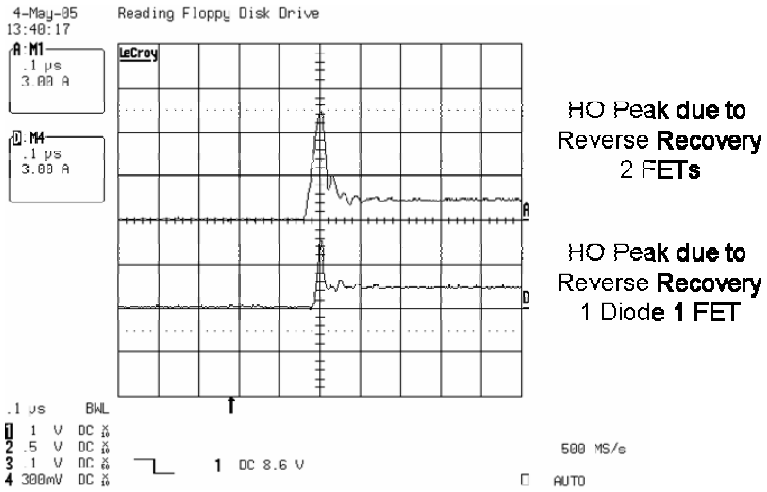


Fig. 19: Low-side FET vs. low-side diode comparison, V_{in} = 100 V, I_{out} = 1.5 A, V_{out} = 17 V

The bus voltage is also of importance since it will determine how long the low-side FET, or the freewheeling diode will be conducting. If the bus voltage is very large in comparison to the output, the low-side FET or diode will be conducting for the majority of the switching period. A FET has much lower on-state losses due to the low $R_{DS,on}$, where as high voltage diodes rarely have forward drops less than 1 V. If the load current is in the order of 1 A or 1.5A, a FET may have low on-state losses, where as the diode may experience larger conduction losses. If the load current is only a few hundred milliamps, the losses observed in the diode may not be a concern, and the cost savings of a diode could be exercised. For system efficiency, the forward conduction losses of a diode can also be compared to the reverse recovery losses with a low-side FET. For this evaluation board, it was found that conduction losses were less than reverse recovery losses when running at 1.5 A and therefore uses and freewheeling diode.

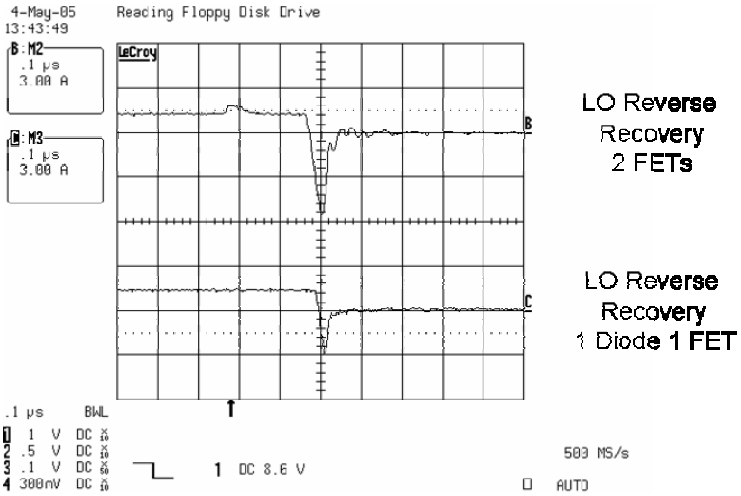


Fig. 20: Low-side FET and low-side diode comparison, V_{in} = 100 V, I_{out} = 1.5 A, V_{out} = 17 V

The most efficient solution would be to put the FET in parallel with the diode in the low-side position. In this case, during the deadtime, instead of the body diode freewheeling, the additional diode would be conducting. This will always be the case as long as the forward drop of the external diode is less than that of the body diode. If costs permit, a diode in parallel with an IGBT could also be an option.

A detailed, evaluation of system needs and cost should be performed prior to choosing a FET or diode for the low-side. Although a diode is cheaper, in certain cases the associated power losses may require a heatsink, nullifying the cost reduction of using a diode. Likewise there are conditions where a FET may prove less efficient, in which case more money will be spent on the FET as well as the heatsink to keep it cool. The evaluation board is provided with a freewheeling diode and the footprint for a low-side FET has been provided to replace the diode with a FET if the application requires it. It is not recommended to replace the diode with a FET for the 1 A and 1.5 A operation because of the associated reverse recovery power losses. If replacing the diode with a FET is a requirement, it might be beneficial to move the diode heatsink to the high-side FET.

In terms of choosing the correct FET, it is best to use a FET rated as low as possible considering what is needed in the application. FET parameters degrade as the voltage ratings go up. Therefore, if a 600 V FET is used in a 200 V application, extra losses may be incurred due to a component that far exceeds the requirements. If using two FETs, the next parameter to be considered is the reverse recovery time. Obviously FETs will not have a reverse recovery time comparable to diodes, but a good FET reverse recovery time will be in the order of 150 ns to 200 ns. The two remaining parameters to consider are direct trade-offs of each other, on resistance and gate charge. If the FET has a rather low gate capacitance, the die size will be small, but this will result in a larger on resistance which could potentially be a problem for high current applications. On the other hand, if the FET has a large gate capacitance, the die will be large and the FET will have a low on resistance, but it will be more difficult to turn on the FET which will also stress the IC. There has to be a direct compromise between the two, typically the best solution is a FET with a relatively low $R_{DS,on}$ and a medium sized gate capacitance, much like the device chosen for this application

6. V_{CC} supply

Since the IRS2540 (IRS2541) is rated for 200 V (600 V), V_{BUS} can reach values of this magnitude. If only a supply resistor to V_{BUS} is used, it will experience high power losses. For higher voltage

applications an alternate V_{CC} supply scheme utilizing a resistor feed-back (R_{S2}) from the output needs to be implemented, as seen in Figs. 1 & 16.

The resistance between V_{BUS} and V_{CC} (R_{S1}) should be large enough to minimize the current sourced directly from the input voltage line; value should be on the order of several kilo ohms. Through this supply resistor a current will flow to charge the V_{CC} capacitor. Once the capacitor is charged up to the V_{CCUV+} threshold, the IRS254(0,1) begins to operate, activating the LO and HO outputs. After the first few cycles of switching, the resistor R_{S2} connected between the output and V_{CC} will take over and source current for the IC. The R_{S2} resistor provided in the evaluation board has been designed for an output of roughly 20 V. If a higher output voltage is desired, R_{S2} will need to be redesigned and adjusted accordingly.

A 10 µF capacitor has been used for stabilizing V_{CC} of the chip. Such a large capacitance makes the chip immune to any large low frequency ripple that may be observed on V_{BUS} due to a rectified waveform. There are also other benefits associated with using such a large capacitance, of which will be discussed later.

With having all input and output voltages defined for the evaluation board, enough information is provided to calculate values for R_{S1}, R_{S2}, and R_{S3} (see Fig. 23 for component definition). All three supply resistors were chosen to be 1 W devices since they source all current to the chip. By making each component 1 W, the work in supplying the chip can be split up equally, making it a more robust solution, instead of baring the entire task on one component. Doing this also allows the chip to turn on at a lower bus voltage. Assuming that a 14 V external zener diode will be used on V_{CC}, exact values of R_{S1}, R_{S2}, and R_{S3} were calculated as follows (values were calculated to operate the components just below half their rated power):

$$P = V^2 / R$$

R_{S1}

$$\tfrac{1}{2} W = \frac{\left(V_{Bus_{\max}} - 14\,V\right)^2}{RS1}$$

$$R_{S1} = \frac{\left(V_{Bus_{\max}} - 14\,V\right)^2}{\tfrac{1}{2} W} = \frac{\left(170\,V - 14\,V\right)^2}{\tfrac{1}{2} W}$$

$$R_{S1} = 48.6\ k\Omega \approx 56\ k\Omega$$

R_{S3}

$$\text{min duty ratio} \approx 10\%$$

$$\tfrac{1}{2} W = \frac{(1-0.1)\cdot\left(V_{Bus_{\max}} - 14\,V\right)^2}{R_{S3}}$$

$$R_{S3} = \frac{(1-0.1)\cdot\left(V_{Bus_{\max}} - 14\,V\right)^2}{\tfrac{1}{2} W} = \frac{(1-0.1)\cdot(170\,V - 14\,V)^2}{\tfrac{1}{2} W}$$

$$R_{S1} = 43.8\ k\Omega \approx 47\ k\Omega$$

R_{S2}

$$\tfrac{1}{2} W = \frac{\left(V_{Out_{\max}} - 14\,V\right)^2}{R_{S2}}$$

$$R_{S2} = \frac{\left(V_{Out_{\max}} - 14\,V\right)^2}{\tfrac{1}{2} W} = \frac{(30\,V - 14\,V)^2}{\tfrac{1}{2} W}$$

$$R_{S1} = 512\ \Omega \approx 1\ k\Omega$$

7. V_{BS} supply

The bootstrap diode (D_{BOOT}) and supply capacitor (C_{BOOT}) comprise the supply voltage for the high-side driver circuitry. To guarantee that the high-side supply is charged up before operation commences, the first pulse from the output drivers comes from the LO pin. During undervoltage lock-out mode, the high- and low-side outputs are both held low.

During an open-circuit condition, without the watchdog timer, the HO output would remain high at all times and the charge stored in C_{BOOT} would slowly leak until reaching zero, thus eliminating the floating power supply for the high-side driver. To maintain sufficient charge on C_{BOOT}, a watchdog timer has been implemented. In the condition where V_{IFB} remains below V_{IFBTH}, the HO output will be forced low roughly after 20 µs and the LO output forced high. This toggling of the outputs will last for 1 µs to maintain and replenish sufficient charge on C_{BOOT}.

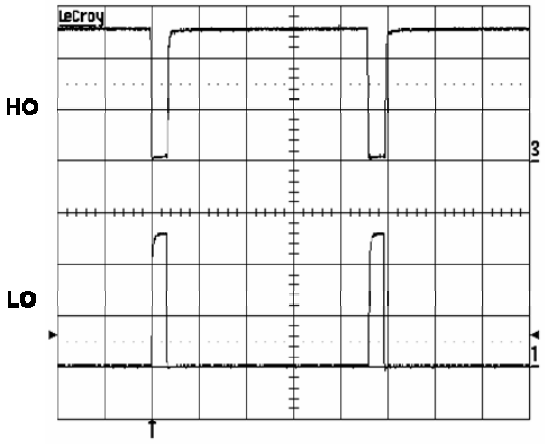


Fig. 21: Illustration of Watchdog Timer

The bootstrap capacitor value needs to be chosen so that it maintains sufficient charge for at least the 20 µs interval until the watchdog timer allows the capacitor to recharge. If the capacitor value is too small, the charge will fully dissipate in less than 20 µs. The bootstrap capacitor should be at least 100 nF. A larger value within reason can be used if preferred.

The bootstrap diode should be a fast recovery, if not an ultrafast recovery component to maintain good efficiency. Since the cathode of the bootstrap diode will be switching between COM and V_{BUS} + 14 V, the reverse recovery time of this diode is of critical importance. For additional information concerning the bootstrap components, refer to the Design Tip (DT 98-2), *"Bootstrap Component Selection For Control ICs"* at www.irf.com under Design Support.

8. Enable pin

The enable pin can be used for dimming and open-circuit protection. When the ENN pin is held low, the chip remains in a fully functional state with no alterations to the operating environment. To disable the control feedback and regulation, a voltage greater than V_{ENTH} (approximately 2.5 V) needs to be applied to the ENN pin. With the chip in a disabled state, HO output will remain low, where as the LO output will remain high to prevent V_S from floating, in addition to maintaining charge on the bootstrap capacitor. The threshold for disabling the IRS254(0,1) has been set to 2.5 V to enhance immunity to any externally generated noise, or application ground noise. This 2.5 V threshold also makes it ideal to receive a drive signal from a local microcontroller.

Dimming mode

To achieve dimming, a signal with constant frequency and set duty cycle can be fed into the EN pin. There is a direct linear relationship between the average load current and duty cycle. If the ratio is 50%, 50% of the maximum set light output will be realized. Likewise if the ratio is 30%, 70% of the maximum set light output will be realized. A sufficiently high frequency of the dimming signal must be chosen to avoid flashing or "strobe light" effect. A signal on the order of a few kHz should be sufficient. For this evaluation board, a fully adjustable (0% to 100% duty cycle) PWM wave generator has been designed but not included in the layout. The following design is a recommended enable signal generator.

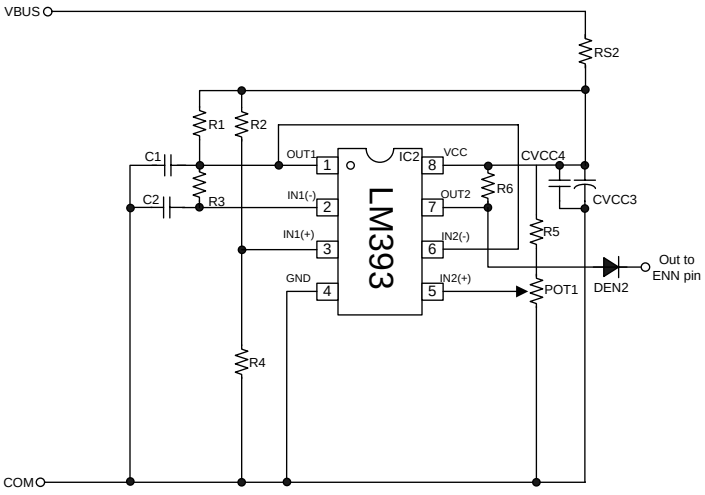


Fig. 22: Suggested PWM Driver (not included in IRPLLED1)

If an external supply for V_{CC} is used, the minimum amount of dimming achievable (light output approaches 0%) will be determined by the "on" time of the HO output, when in a fully functional regulating state. To maintain reliable dimming, it is recommended to keep the "off" time of the enable signal at least 10 times that of the HO "on" time. For example, if the application is running at 75 kHz with an input voltage of 100 V and an output voltage of 20 V, the HO "on" time will be 3.3 µs (one-fourth of the period – see calculations below) according to standard buck topology theory. This will set the minimum "off" time of the enable signal to 33 µs.

$$Duty\ Cycle = \frac{V_{out}}{V_{in}} * 100 = \frac{20\,V}{100\,V} * 100 = 20\%$$

$$HO_{on\ \text{time}} = 20\% * {}^{1}\!\!\diagup\!\!_{75\ kHz} = 3.3\ \mu s$$

If the chip is supplied from the output, a large enough capacitor on V_{CC} is required to maintain sufficient current while in a disabled state. For this evaluation board, where the IC supply comes from the output, a 10 µF capacitor is used to ensure continued proper operation while disabled, the output is capable of dimming down to roughly 10 V. A "strobe light" effect in the LEDs may be observed if V_{CC} drops too much or if the dimming frequency is too low.

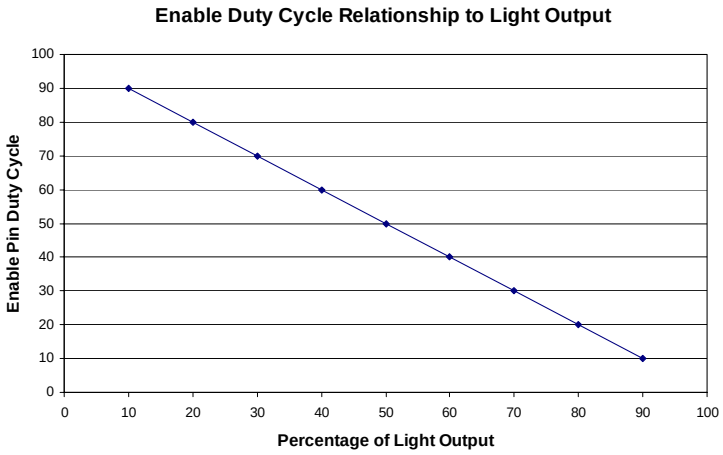


Fig. 23: Light Output vs. Enable Pin Duty Cycle

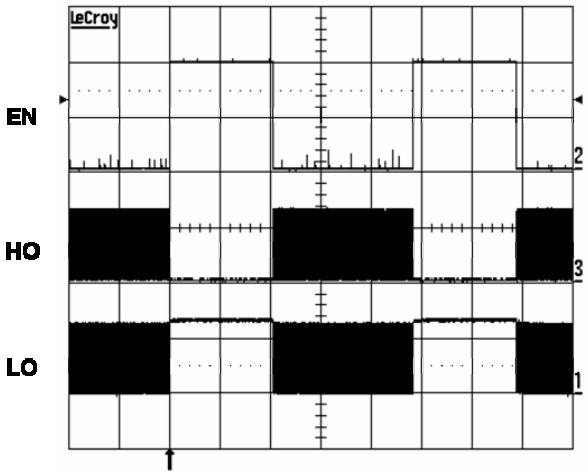


Fig. 24: IRS2540 Dimming Signals

Since the IRS254(0,1) does not include an onboard oscillator, a soft start feature is not possible. This is only a concern when operating in the dimming mode. Since PWM dimming is required of LEDs, the output is essentially turning on and off at a rate of the dimming frequency. In the absence of soft start, a large spike of current would be observed in the load each time the output is turned on. This current spike stresses the load possibly decreasing its overall lifetime. The IRPLLED1 includes a jumper setting to define whether or not the board is being used in the dimming mode. This two position jumper will allow the designer to either include or exclude the resistor R_{out}, which is in series with the output capacitor. The inclusion of this resistor will sufficiently damp the output stage, such that output current spikes are significantly reduced or eliminated. The presence of such current spikes may cause the inductor to hum or buzz, the emitted sound will be that of the dimming frequency. The inrush of current causes mechanical movement in the inductor which can be heard if the PWM signal is within the audible range of the human ear. The effects of adding in R_{out} can be seen in Figs. 25 – 28.

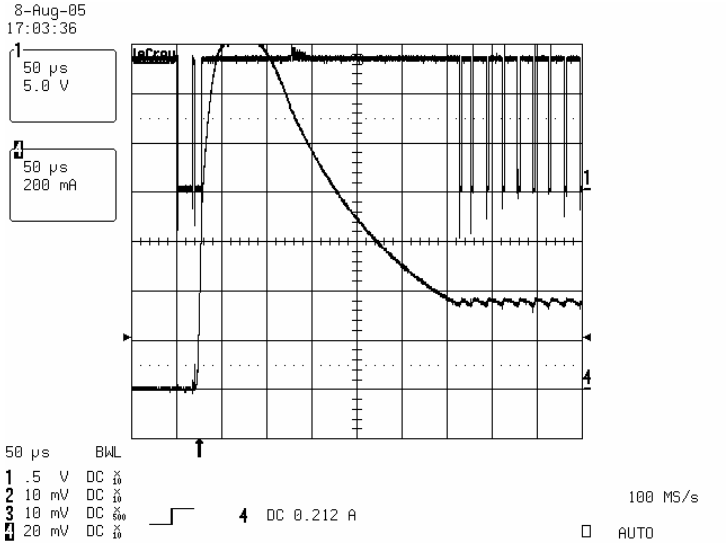


Fig. 25: Load Current Spike Excluding R_{out}
I_{out} = 350 mA, V_{in} = 100 V, V_{out} = 17 V

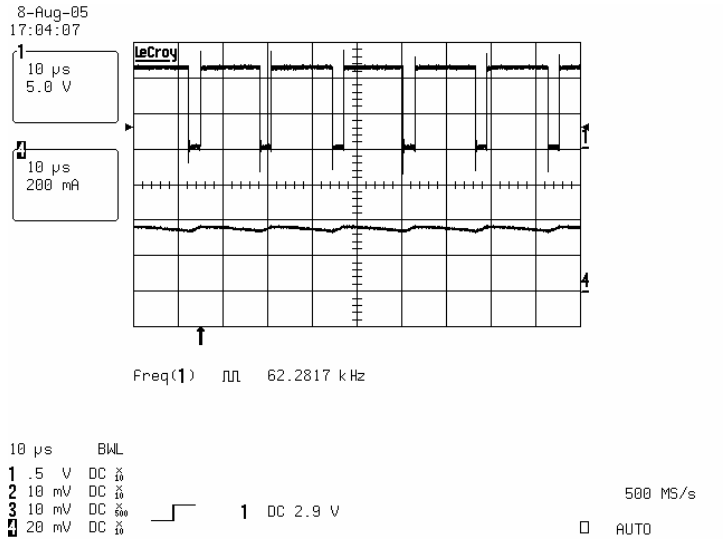


Fig. 26: Load Current Ripple Excluding R_{out}
I_{out} = 350 mA, V_{in} = 100 V, V_{out} = 17 V

Although the inclusion of the resistor will minimize or eliminate the load current spikes, the overall current regulation and operating frequency will be slightly compromised. The resistor will reduce the overall effectiveness of the output capacitor which means the switching frequency will marginally increase. Likewise the output ripple current will also increase, which ultimately leads to a larger current regulation tolerance. Although the overall current regulation capabilities may decrease with the inclusion of this resistor, the actual stability of the PWM dimming signal will still be the dominant factor of the overall output current regulation capabilities.

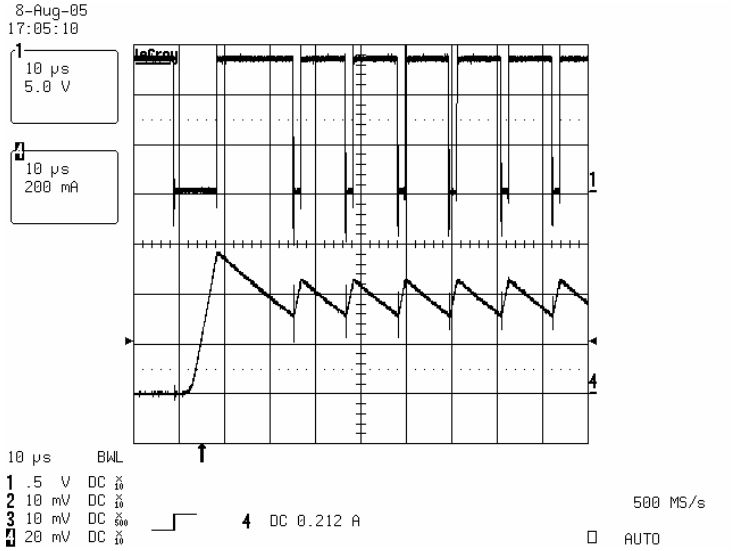


Fig. 27: Load Current Spike Including R_{out} (5 Ω)
I_{out} = 350 mA, V_{in} = 100 V, V_{out} = 17 V

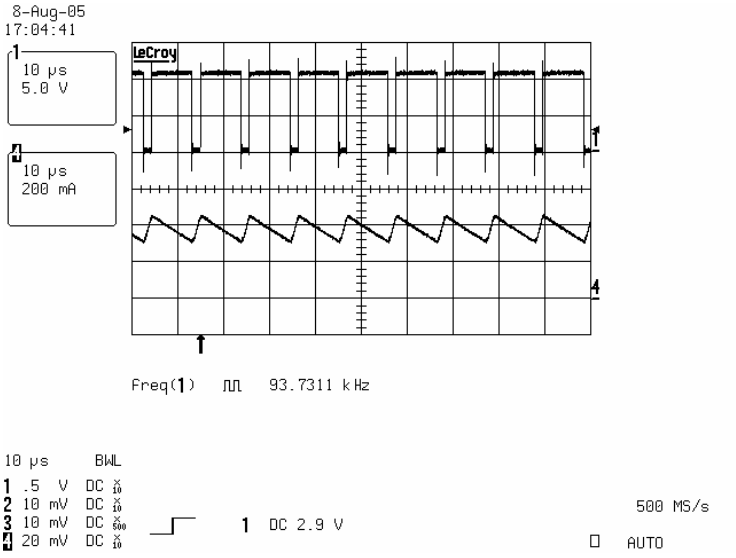


Fig. 28: Load Current Ripple Including R_{out} (5 Ω)
I_{out} = 350 mA, V_{in} = 100 V, V_{out} = 17 V

Open-circuit protection mode

By using the suggested voltage divider, capacitor, and zener diode, the designer can virtually clamp the output voltage at any desired value. If there is no load and the output clamp is not utilized, the positive output terminal will float at the high-side input voltage. The open load clamp is recommended if the load is disconnected and then reconnected without shutting down the driver. When the load is reconnected with power on, the load would see the entire bus voltage for a short period of time. The

open-circuit clamp minimizes the amount of stress seen by the load under such circumstances by clamping the voltage much lower than V_{BUS}.

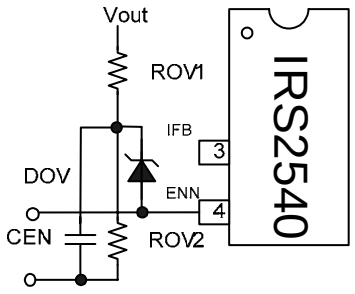


Fig. 29: Open-Circuit Protection Scheme

In open-circuit condition, switching will still occur between the HO and LO outputs, whether due to the output voltage clamp or to the watchdog timer. In this state, rather than regulating the current with the feedback pin, the output voltage will be loosely regulated via the enable pin. Transients and switching will be observed at the positive output terminal as seen in Fig. 30. The difference in signal shape, between the output voltage and the I_{FB}, is due to the capacitor C_{EN} used to form the voltage clamp. The repetition of the spikes can be reduced by simply increasing the cap size. If V_{BUS} is significantly larger than the desired output voltage clamp, the output voltage will become a function of V_{BUS}. This is because of the intrinsic delays of the chip ($t_{LO,on}$, $t_{LO,off}$, $t_{HO,on}$, and $t_{HO,off}$) along with the minimum HO on time. If the load is removed, the output will clamp at the desired voltage. Then if the bus voltage is increased, there could be a proportional change in the clamped voltage. This is not seen as an issue since the open-circuit clamp is strictly a safety feature to reduce the stress seen by the load, if disconnected and reconnected without a power down.

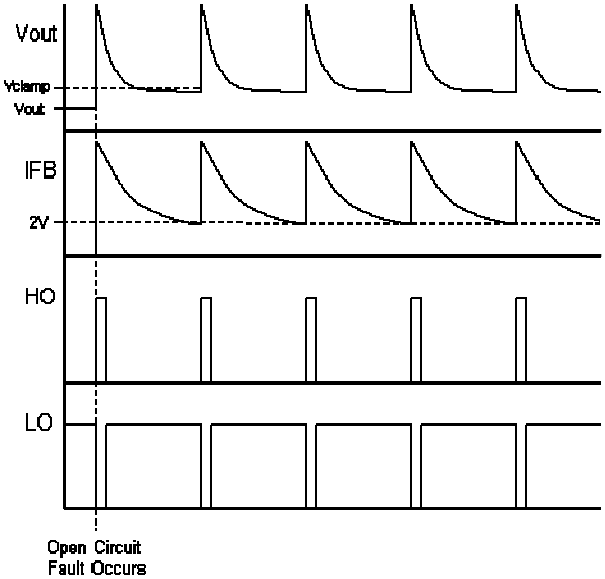


Fig. 30: Open-Circuit Fault Signals, with Clamp

The two resistors R_{OV1} and R_{OV2} form a voltage divider for the output, which is then fed into the cathode of the zener diode D_{OV}. The diode will only conduct, flooding the enable pin, when its nominal voltage is exceeded. The chip will enter a disabled state once the divider network produces a voltage at least 2.5 V greater than the zener rating. The capacitor C_{EN} serves only to filter and slow the transients/switching at the positive output terminal. The clamped output voltage can be determined by the following analysis.

$$V_{out} = \frac{(2.5\,V + DZ)(R_1 + R_2)}{R_2}$$

$$DZ = \text{Zener Diode Nominal Rated Voltage}$$

D_{OV} has been chosen to be a 7.5 V zener diode. R_{OV2} has also been set to 390 Ω to help provide a low resistive charging path for C_{BOOT} as previously discussed. It was also decided to clamp the output voltage at 30 V, this is sufficiently larger than the predefined maximum load voltage of 24 V as to not cause any erroneous shut-down, while it is also well within the specifications of the 100 V rated output stage. Having arbitrarily chosen these parameters, R_{OV1} was calculated as follows:

$$V_{out} = \frac{(2.5\,V + DZ)(R_{OV1} + R_{OV2})}{R_{OV2}}$$

$$R_{OV1} = \frac{V_{out} R_{OV2}}{(2.5\,V + DZ)} - R_{OV2} = \frac{30\,V \cdot 390\,\Omega}{(2.5\,V + 7.5\,V)} - 390\,\Omega = 780\,\Omega$$

$$R_{OV1} \approx 820\,\Omega$$

9. Other design considerations

Filtering

The RC filter on the IFB pin is only used to remove high frequency transients associated with the FET switching. The corner frequency of this filter was left high enough to prevent any further distortion of the feedback.

The input filter is a low-pass filter. Its main objective is to prevent ringing of comparable frequency on V_{bus}. Exact values of capacitance and inductance are not of critical importance, so long as filtering is accomplished. In addition to the electrolytic that is used for filtering on the bus, there is also a small ceramic for high frequency signals. Ceramic capacitors typically have low ESR such that they are more ideal for high frequency filtering.

V_{CC} filtering was accomplished by typical means of using a small 100 nF ceramic, an additional electrolytic was used in case of dimming. The larger electrolytic was placed in event a long enable signal is given. With this larger capacitance, the V_{CC} supply will remain for a prolonged period of time so the outputs will remain disabled, and the chip will not shut down.

The ENN filter capacitor was arbitrarily chosen to be 100 nF, this helps slow the rate of switching during open load conditions.

The IRS254(0,1) was specifically designed to handle low frequency ripples on V_{BUS}. Its capability to handle such ripple makes it ideal for an offline rectified waveform. However if high voltage (on the order of 5 V to 10 V) high frequency oscillations (greater than or close to the operating frequency) are present on V_{BUS}, it is recommended to implement an input filter. If these high frequency signals are present on V_{BUS} the IRS254(0,1) will still continue to regulate the current through the load, but abnormal switching of LO and HO may be observed. This poses a problem in terms of switching losses. As previously discussed, one may need or want to control the operating frequency to control the systems efficiency, but if LO and HO randomly switch, it may negate all attempts to control the frequency. Of course the root of this problem can be significantly contributed through PCB layout, but it is also a function of the load current. If filters on I_{FB} and V_{CC} are not placed correctly these high frequency ripples will couple to the chip and appear within the control loop. Also if the load current is on the order of 1 A or 1.5 A, when HO turns on, the load immediately tries to pull the rated current. Since the circuit supply is not usually close by, the capacitance of the input wire is not enough to compensate for this large pull of current, this will result in oscillations or change in potential on the input line. Since the switching element of the circuit is one cause of these oscillations, it is easy to see how likely the presence of high frequency oscillations are. To alleviate the circuit of such possible problems, it is much easier to implement an input filter. The input filter will also greatly improve the circuits EMC performance.

EMC performance

The IRS254(0,1) demo board has not been EMC tested. Input and output filters can be used to reduce the conducted emissions to below the limits of the applicable EMC standard as needed. All inductors may require a powdered iron core rather than ferrite, it can handle a much larger current before saturating, needs are pending on the load current. If EMC is of critical importance, one may prefer to use one FET and one diode, in contrast to a half-bridge driver. The reverse recovery time for a diode is inherently shorter than that of a FET. This will help in reducing transients observed in the switching elements resulting in better EMC performance.

Layout considerations

It is very important when laying out the PCB for the IRS254(0,1) to consider the following points:

1. C_{VCC2} and C_F must be as close to the IC as possible.
2. The feedback path should be kept to a minimum without crossing any high frequency lines.
3. C_{OUT} should be as close to the main inductor as possible.
4. All traces that form the nodes V_S and V_B should be kept as short as possible.
5. All signal and power grounds should be kept isolated from each other to prevent noise from entering the control environment. It's a general rule of thumb that all components associated with the IC should be connected to the IC ground with the shortest path possible.
6. All traces carrying the load current need to be adjusted accordingly.
7. Gate drive traces should also be kept to a minimum.

10. Design procedure summary

1. Determine the systems requirements: input/output voltage and current needed
2. Calculate current sense resistor
3. Determine the operating frequency required
4. Select L_1 and C_{OUT} so that they maintain supply into the load during $t_{HO,on}$.

5. Select switching components (FET/freewheeling diode) to minimize power losses
6. Determine V_{CC} and V_{BS} supply components
7. Add filtering on the input, I_{FB} and ENN as needed
8. Fine tune components to achieve desired system performance

11. Bill of materials

Careful selection of the components will significantly increase the reliability of the product, particularly for the capacitors. These need to be rated for at least 100 ºC and a proper voltage. As in most electronic power applications, capacitors and resistors are the components most likely to fail due to stress over time and high operating temperatures. All capacitors connected to the output in this evaluation board have only a rating of 100 V. These capacitors may also need to be changed if the load is significantly different from the tested load.

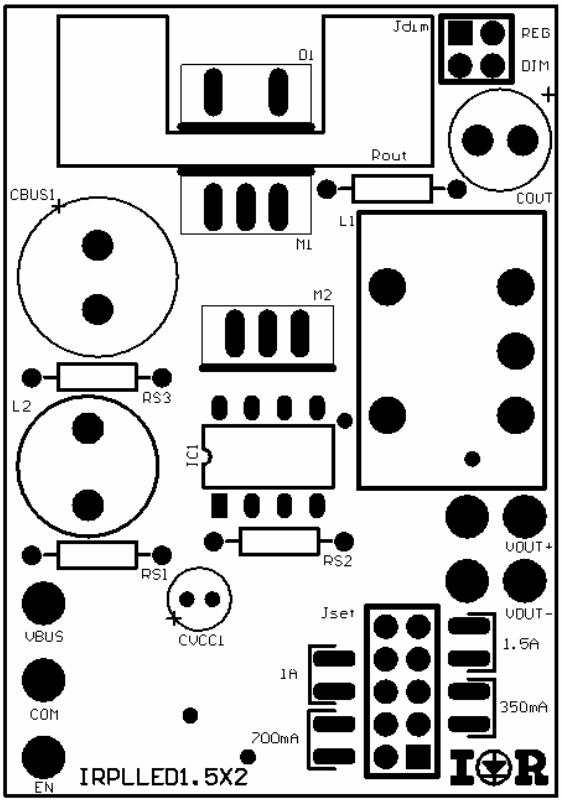
Item	Device Type	Description	Part #	Manufacurer	# of devices	Reference
1	C	10uF, 25V, Radial	UVZ1E100MDD	Nichicon	1	CVCC1
2	C	100nF, 200V, 1812	VJ1812Y104KXCAT	BC Components	1	CBUS2
3	C	100nF, 50V, 0805	VJ0805Y104KXATW1BC	BC Components	3	CVCC2, CBOOT, CEN
4	C	33uF, 100V	UVZ2A330MPD	Nichicon	1	COUT
5	C	1nF, 50V, 0805	VJ0805Y102KXACW1BC	BC Components	1	CF
6	C	47uF, 200V	UVZ2D470MHD	Nichicon	1	CBUS1
7	D	200V, 1A	MUR120T3	On Semi	1	DBOOT
8	D	Mini Melf	LL4148	Diodes Inc	2	DEN1, DVCC
9	D	300V, 8A	8ETH03	IR	1	D1
10	DZ	14V, 0.5W, Mini Melf	ZMM5244B-7	Diodes Inc	1	DCLAMP
11	DZ	7.5V, 0.5W, Mini Melf	ZMM5236B-7	Diodes Inc	1	DOV
12	L	470uH	IL 050 321 31 01	VOGT	1	L1
13	L	470uH	RFB1010-471	Coilcraft	1	L2
14	R	10ohm, 1%, 0805	MCR10EZHF10R0	Rohm	1	RG1
15	R	0.56ohm, 1%, 1206	ERJ-8RQFR56V	Panasonic	3	RCS2, RCS4, RCS6
16	R	0.47ohm, 1%, 1206	ERJ-8RQFR47V	Panasonic	3	RCS1, RCS3, RCS5
17	R	1.43ohm, 1%, 1206	9C12063A1R43FGHFT	Yageo	2	RCS7, RCS8
18	R	100ohm, 1%, 0805	MCR10EZHF1000	Rohm	1	RF
19	R	390ohm, 5%, 1/2W, 2010	ERJ12ZYJ391	Panasonic	1	ROV2
20	R	820ohm, 5%, 1/2W, 2010	ERJ12ZYJ821	Panasonic	1	ROV1
21	R	1k, 5%, 1W	5073NW1K000J12AFX	Phoenix Passive	1	RS2
22	R	47K, 5%, 1W	5073NW47K00J12AFX	Phoenix Passive	1	RS3
23	R	56K, 5%, 1W	5073NW56K00J12AFX	Phoenix Passive	1	RS1
24	R	5ohm, 5%, 1W	5073NW5R100J12AFX	Phoenix Passive	1	Rout
25	IC	IRS2540/1	IRS2540/1	IR	1	In Socket
26	Socket	8 Pin DIP	2-641260-1	Amp	1	IC1
27	M	200V, 16A, TO-220	IRFB17N20D	IR	1	M1
28	T	PC Compact, red	5005	Keystone	2	T1, T4
29	T	PC Compact, black	5006	Keystone	2	T2, T5
30	T	PC Compact, yellow	5009	Keystone	1	T3
31	H	Heatsink	7-340-1PP-BA	IERC	1	
32	B	PCB			1	
33	J	Jumper, 10 Pos.	929836-09-05-ND	3M	1	Jset
34	J	Jumper, 2 Pos.	929836-09-02-ND	3M	1	Jdim
35	SJ	Shorting Jumper	929950-00-ND	3M	3	
36	D	Not Fitted				DIFB
37	R	Not Fitted				RIFB
38	M	Not Fitted				M2
39	TH	TO-220 Insulating Thermal P	SP600-54	Berquist	2	
40	W	Shoulder Washer	3049	Berquist	2	
41	SC	Screw, 4-40, 0.5", Zinc	H346-ND	Building Fasteners	1	
42	N	Nut, 4-40, Hex, Zinc	H216-ND	Building Fasteners	1	

Enable Signal Generator (not included)

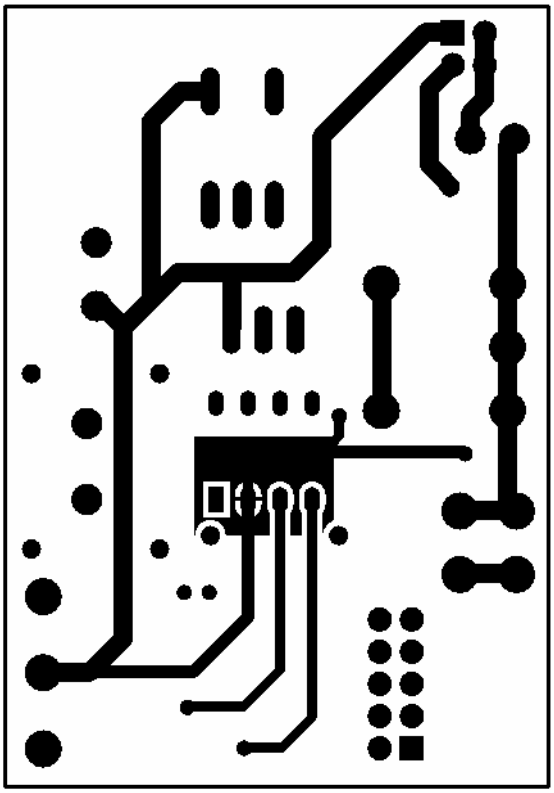
Item	Device Type	Description	Part #	Manufacurer	# of devices	Reference
1	C	10uF, 25V, Radial	ECEA1EKG100	Panasonic	1	CVCC3
2	C	100nF, 50V, 0805	VJ0805Y104KXATW1BC	BC Components	1	CVCC4
3	C	1nF, 50V, 0805	VJ0805Y102KXACW1BC	BC Components	2	C1, C2
4	D	Mini Melf	LL4148	Diodes Inc	1	DEN2
5	R	1k, 1%, 0805	MRC10EZHF1001	Rohm	1	R6
6	R	6.8k, 1%, 0805	MRC10EZHF6801	Rohm	1	R5
7	R	10k, 1%, 0805	MRC10EZHF1002	Rohm	1	R4
8	R	20k	MRC10EZHF2002	Rohm	1	R2
9	R	75k	MRC10EZHF7502	Rohm	2	R1, R3
10	R	100k	MRC10EZHF1003	Rohm	2	RS2
11	POT	10k, 10-turn	M64W103KB40	BC Components	1	POT1
12	IC	Comparator	LM393D	Texas Instruments	1	In Socket
13	Socket	8 Pin DIP	2-641260-1	Amp Tyco Electronics	1	IC2

12. PCB Layout

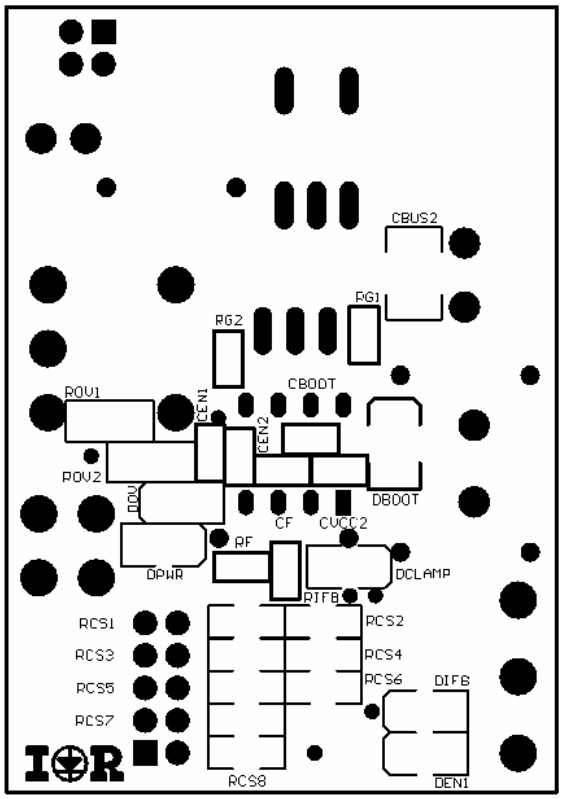
Top Overlay



Top Metal



Bottom Overlay



Bottom Metal