

**32M x 72 1 Bank Registered/Buffered SDRAM Module****Features**

- 168-Pin Registered 8-Byte Dual In-Line Memory Module
- 32Mx72 Synchronous DRAM DIMM
- Performance:

| | -260 CL=2 | | -360 CL=3 | | -360 CL=2 | | Units |
|--------------------------------------|-----------|-------|-----------|-------|-----------|-------|-------|
| | Reg. | Buff. | Reg. | Buff. | Reg. | Buff. | |
| DIMM $\overline{\text{CAS}}$ Latency | 3 | 2 | 4 | 3 | 3 | 2 | |
| f_{CK} Clock Frequency | 100 | 100 | 100 | 100 | 66 | 66 | MHz |
| f_{CK} Clock Cycle | 10 | 10 | 10 | 10 | 15 | 15 | ns |
| t_{AC} Clock Access | 7.2 | 7.2 | 7.2 | 7.2 | 10.2 | 10.2 | ns |

- Intended for 66/100MHz and PC100 applications
- Inputs and outputs are LVTTTL (3.3V) compatible
- Single 3.3V \pm 0.3V Power Supply
- Single Pulsed $\overline{\text{RAS}}$ interface
- SDRAMs have four internal banks
- Module has one physical bank

- Fully Synchronous to positive Clock Edge
- Programmable Operation:
 - DIMM $\overline{\text{CAS}}$ Latency: 3, 4 (Registered mode); 2, 3 (Buffered mode)
 - Burst Type: Sequential or Interleave
 - Burst Length: 1, 2, 4, 8
 - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 12/11/2 Addressing (Row/Column/Bank)
- 4096 refresh cycles distributed across 64ms
- Card size: 5.25" x 0.157" x 1.70"
- Gold contacts
- SDRAMs in TSOP
- Serial Presence Detect with Write protect

Description

IBM13M32734CCA is a registered 168-Pin Synchronous DRAM Dual In-Line Memory Module (DIMM) organized as a 32Mx72 high-speed memory array. The DIMM uses eighteen 32Mx4 SDRAMs in 400 mil TSOP packages. The DIMM achieves high-speed data-transfer rates of up to 100 MHz by employing a prefetch/pipeline hybrid architecture that synchronizes the output data to a system clock.

The DIMM is intended for use in applications operating from 66MHz to 100 MHz, PC100, memory bus speeds, and/or heavily loaded bus applications. All control and address signals are re-driven through registers/buffers to the SDRAM devices. The DIMM can be operated in either registered mode (REGE pin tied high), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin tied low) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. XTK simulation models of the DIMM are available to determine which mode to design for.

A phase-lock loop (PLL) on the DIMM is used to re-drive the clock signals to both the SDRAM devices and the registers to minimize system clock loading.

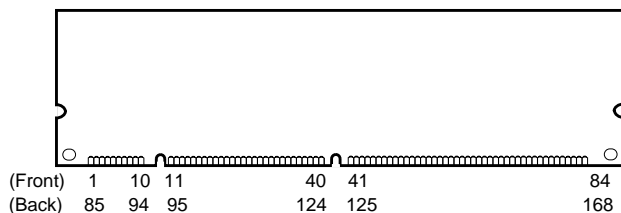
(CK0 is connected to the PLL, and CK1, CK2, and CK3 are terminated on the DIMM.) A single clock enable (CKE0) controls all devices on the DIMM, enabling the use of SDRAM power-down modes.

Prior to any access operation, the device $\overline{\text{CAS}}$ latency and burst type/length/operation type must be programmed into the DIMM by address inputs A0-A9 and A11 using the mode register set cycle. The DIMM $\overline{\text{CAS}}$ latency when operated in buffered mode is the same as the device $\overline{\text{CAS}}$ latency as specified in the SPD EEPROM. The DIMM $\overline{\text{CAS}}$ latency when operated in registered mode is one clock later due to the address and control signals being clocked to the SDRAM devices.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are programmed and locked by the DIMM manufacturer. The last 128 bytes are available to the customer and may be write protected by providing a high level to pin 81 on the DIMM. An on-board pulldown resistor keeps this in the write-enable mode.

All IBM 168-pin DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

Card Outline



Pin Description

| | | | |
|--|-----------------------------|-----------------|--|
| CK0-CK3 | Clock Inputs | DQ0 - DQ63 | Data Input/Output |
| CKE0 | Clock Enable | CB0 - CB7 | Check Bit Data Input/Output |
| $\overline{\text{RAS}}$ | Row Address Strobe | DQMB0 - DQMB7 | Data Mask |
| $\overline{\text{CAS}}$ | Column Address Strobe | V_{DD} | Power (3.3V) |
| $\overline{\text{WE}}$ | Write Enable | V_{SS} | Ground |
| $\overline{\text{S}}_0, \overline{\text{S}}_2$ | Chip Selects | NC | No Connect |
| A0-A9, A11 | Address Inputs | SCL | Serial Presence Detect Clock Input |
| A10/AP | Address Input/Autoprecharge | SDA | Serial Presence Detect Data Input/Output |
| BA0, BA1, (A13,A12) | SDRAM Bank Address Inputs | SA0-2 | Serial Presence Detect Address Inputs |
| WP | SPD Write Protect | REGE | Register Enable |



Pinout

| Pin# | Front Side | Pin# | Back Side | Pin# | Front Side | Pin# | Back Side | Pin# | Front Side | Pin# | Back Side | Pin# | Front Side | Pin# | Back Side |
|------|-----------------|------|-----------------|------|-----------------|------|------------------|------|-----------------|------|-----------------|------|-----------------|------|-----------------|
| 1 | V _{SS} | 85 | V _{SS} | 22 | CB1 | 106 | CB5 | 43 | V _{SS} | 127 | V _{SS} | 64 | V _{SS} | 148 | V _{SS} |
| 2 | DQ0 | 86 | DQ32 | 23 | V _{SS} | 107 | V _{SS} | 44 | NC | 128 | CKE0 | 65 | DQ21 | 149 | DQ53 |
| 3 | DQ1 | 87 | DQ33 | 24 | NC | 108 | NC | 45 | $\overline{S}2$ | 129 | NC | 66 | DQ22 | 150 | DQ54 |
| 4 | DQ2 | 88 | DQ34 | 25 | NC | 109 | NC | 46 | DQMB2 | 130 | DQMB6 | 67 | DQ23 | 151 | DQ55 |
| 5 | DQ3 | 89 | DQ35 | 26 | V _{DD} | 110 | V _{DD} | 47 | DQMB3 | 131 | DQMB7 | 68 | V _{SS} | 152 | V _{SS} |
| 6 | V _{DD} | 90 | V _{DD} | 27 | \overline{WE} | 111 | \overline{CAS} | 48 | NC | 132 | NC | 69 | DQ24 | 153 | DQ56 |
| 7 | DQ4 | 91 | DQ36 | 28 | DQMB0 | 112 | DQMB4 | 49 | V _{DD} | 133 | V _{DD} | 70 | DQ25 | 154 | DQ57 |
| 8 | DQ5 | 92 | DQ37 | 29 | DQMB1 | 113 | DQMB5 | 50 | NC | 134 | NC | 71 | DQ26 | 155 | DQ58 |
| 9 | DQ6 | 93 | DQ38 | 30 | $\overline{S}0$ | 114 | NC | 51 | NC | 135 | NC | 72 | DQ27 | 156 | DQ59 |
| 10 | DQ7 | 94 | DQ39 | 31 | NC | 115 | \overline{RAS} | 52 | CB2 | 136 | CB6 | 73 | V _{DD} | 157 | V _{DD} |
| 11 | DQ8 | 95 | DQ40 | 32 | V _{SS} | 116 | V _{SS} | 53 | CB3 | 137 | CB7 | 74 | DQ28 | 158 | DQ60 |
| 12 | V _{SS} | 96 | V _{SS} | 33 | A0 | 117 | A1 | 54 | V _{SS} | 138 | V _{SS} | 75 | DQ29 | 159 | DQ61 |
| 13 | DQ9 | 97 | DQ41 | 34 | A2 | 118 | A3 | 55 | DQ16 | 139 | DQ48 | 76 | DQ30 | 160 | DQ62 |
| 14 | DQ10 | 98 | DQ42 | 35 | A4 | 119 | A5 | 56 | DQ17 | 140 | DQ49 | 77 | DQ31 | 161 | DQ63 |
| 15 | DQ11 | 99 | DQ43 | 36 | A6 | 120 | A7 | 57 | DQ18 | 141 | DQ50 | 78 | V _{SS} | 162 | V _{SS} |
| 16 | DQ12 | 100 | DQ44 | 37 | A8 | 121 | A9 | 58 | DQ19 | 142 | DQ51 | 79 | CK2 | 163 | CK3 |
| 17 | DQ13 | 101 | DQ45 | 38 | A10/AP | 122 | BA0 | 59 | V _{DD} | 143 | V _{DD} | 80 | NC | 164 | NC |
| 18 | V _{DD} | 102 | V _{DD} | 39 | BA1 | 123 | A11 | 60 | DQ20 | 144 | DQ52 | 81 | WP | 165 | SA0 |
| 19 | DQ14 | 103 | DQ46 | 40 | V _{DD} | 124 | V _{DD} | 61 | NC | 145 | NC | 82 | SDA | 166 | SA1 |
| 20 | DQ15 | 104 | DQ47 | 41 | V _{DD} | 125 | CK1 | 62 | NC | 146 | NC | 83 | SCL | 167 | SA2 |
| 21 | CB0 | 105 | CB4 | 42 | CK0 | 126 | NC | 63 | NC | 147 | REGE | 84 | V _{DD} | 168 | V _{DD} |

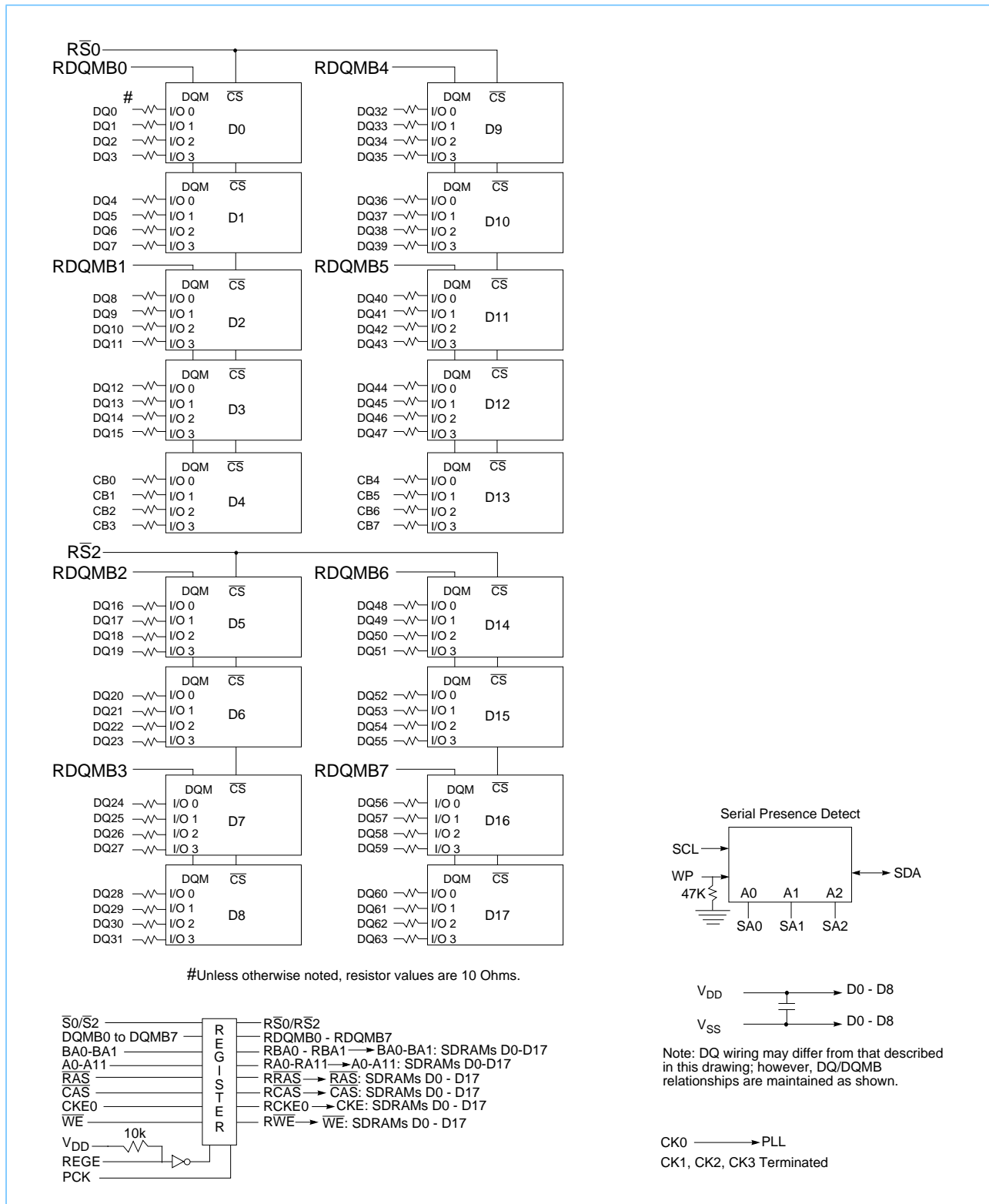
Note: All pin assignments are consistent with all 8-byte unbuffered versions.

Ordering Information

| Part Number | Organization | Device CAS Latency | Device Access Time | Clock Cycle | Leads | Dimension | Power | Note |
|---------------------|--------------|--------------------|--------------------|-------------|-------|------------------------|-------|------|
| IBM13M32734CCA-260T | 32Mx72 | 3, 2 | 6.0ns | 10ns | Gold | 5.25" x 0.157" x 1.70" | 3.3V | 1 |
| IBM13M32734CCA-360T | 32Mx72 | 3 | 6.0ns | | | | | |
| | | 2 | 9.0ns | 15ns | | | | |

1. PC100 applications

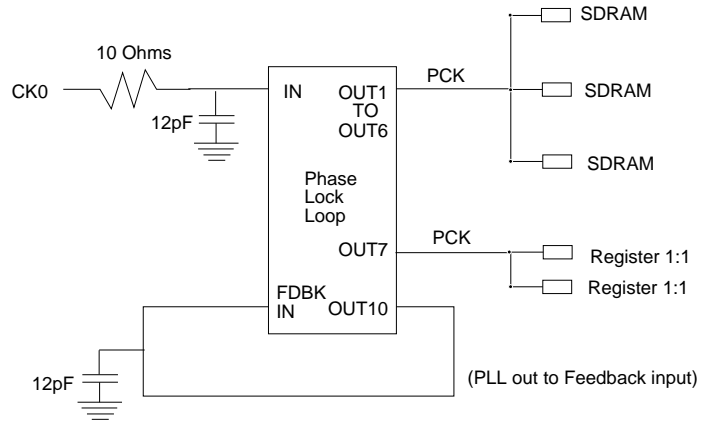
x72 ECC SDRAM DIMM Block Diagram (1 Bank, x4 SDRAMs)



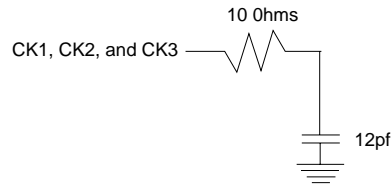
Clock Wiring

Clock Net Wiring (CK0):

One of six SDRAM outputs is shown. All PLL clock SDRAM loads are equal--achieved in part through equal-length wiring.



Terminated Clock Nets (CK1, CK2, CK3):



- Notes:
1. The PLL is programmed via a combination of the feedback path and on-DIMM loading. PLL feedback produces zero phase shift from the delayed CK0 input.
 2. Card wiring and capacitance loading variation: ± 100 ps.
 3. Timing is based on a driver with a 1 Volt/ns rise time.
 4. Feedback Capacitor Value determined by PLL phase characteristics.



Input/Output Functional Description

| Symbol | Type | Signal | Polarity | Function |
|---|-----------------|--------|---------------------------------------|---|
| CK0 - CK3 | Input | Pulse | Positive Edge | The system clock inputs. All the SDRAM inputs are sampled on the rising edge of their associated clock. CK0 drives the PLL. CK1, CK2, and CK3 are terminated. |
| CKE0 | Input | Level | Active High | Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, the Suspend mode, or the Self Refresh mode. |
| $\overline{S0}, \overline{S2}$ | Input | Pulse | Active Low | Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}, \overline{CAS}, \overline{WE}$ | Input | Pulse | Active Low | When sampled at the positive rising edge of the clock, \overline{CAS} , \overline{RAS} , and \overline{WE} define the operation to be executed by the SDRAM. |
| BA0, 1 | Input | Level | — | Selects which SDRAM bank of four is activated. |
| A0 - A9, A11 A10/AP | Input | Level | — | During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 and A11 defines the column address (CA0-CA9, CA11) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge. |
| DQ0 - DQ63, CB0 - CB7 | Input Output | Level | — | Data and Check Bit Input/Output pins |
| DQMB0 - DQMB7 | Input | Pulse | Active High | The Data Input/Output masks, associated with one data byte, place the DQ buffers in a high-impedance state when sampled high. In Read mode, DQMB has a latency of two clock cycles in Buffered mode or three clock cycles in Registered mode, and controls the output buffers like an output enable. In Write mode, DQMB has a zero clock latency in Buffered mode and a latency of one clock cycle in Registered mode. In this case, DQMB operates as a byte mask by allowing input data to be written if it is low but blocking the write operation if it is high. |
| V_{DD}, V_{SS} | Supply | | | Power and ground for the module. |
| REGE | Input | Level | Active High (Register Mode Enable) | The Register Enable pin is used to permit the DIMM to operate in “buffered” mode (inputs re-driven asynchronously) or “registered” mode (signals re-driven to SDRAMs when clock rises, and held valid until next rising clock). |
| SA0 - 2 | Input | Level | — | These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM. |
| SDA | Input Output | Level | — | This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup. |
| SCL | Input | Pulse | — | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup. |
| WP | Input | Level | Active High | This signal is pulled low on the DIMM to enable data to be written into the last 128 bytes of the SPD EEPROM. |



Serial Presence Detect (Part 1 of 2)

| Byte # | Description | SPD Entry Value | Serial PD Data Entry (Hexadecimal) | Notes |
|--------|--|--|------------------------------------|-------|
| 0 | Number of Serial PD Bytes Written during Production | 128 | 80 | |
| 1 | Total Number of Bytes in Serial PD device | 256 | 08 | |
| 2 | Fundamental Memory Type | SDRAM | 04 | |
| 3 | Number of Row Addresses on Assembly | 12 | 0C | |
| 4 | Number of Column Addresses on Assembly | 11 | 0B | |
| 5 | Number of DIMM Banks | 1 | 01 | |
| 6 - 7 | Data Width of Assembly | x72 | 4800 | |
| 8 | Assembly Voltage Interface Levels | LVTTL | 01 | |
| 9 | SDRAM Device Cycle Time (CL = 3) | 10.0ns | A0 | 1, 2 |
| 10 | SDRAM Device Access Time from Clock at CL=3 | 6.0ns | 60 | |
| 11 | Assembly Error Detection/Correction Scheme | ECC | 02 | |
| 12 | Assembly Refresh Rate/Type | SR/1X(15.625us) | 80 | |
| 13 | SDRAM Device Width | x4 | 04 | |
| 14 | Error Checking SDRAM Device Width | x4 | 04 | |
| 15 | SDRAM Device Attr: Min Clk Delay, Random Col Access | 1 Clock | 01 | |
| 16 | SDRAM Device Attributes: Burst Lengths Supported | 1,2,4,8, Full Page | 8F | |
| 17 | SDRAM Device Attributes: Number of Device Banks | 4 | 04 | |
| 18 | SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency | 2, 3 | 06 | |
| 19 | SDRAM Device Attributes: $\overline{\text{CS}}$ Latency | 0 | 01 | |
| 20 | SDRAM Device Attributes: $\overline{\text{WE}}$ Latency | 0 | 01 | |
| 21 | SDRAM Module Attributes | Registered/Buffered with PLL | IF | |
| 22 | SDRAM Device Attributes: General | Write-1/Read Burst, Pre-charge All, Auto-Precharge | 0E | |
| 23 | Minimum Clock Cycle at CLX-1 (CL = 2) | -260 | 10.0ns | 1, 2 |
| | | -360 | 15.0ns | |
| 24 | Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 2) | -260 | 6.0ns | 60 |
| | | -360 | 9.0ns | 90 |
| 25 | Minimum Clock Cycle Time at CLX-2 (CL = 1) | N/A | 00 | |
| 26 | Maximum Data Access Time (t_{AC}) from Clock at CLX-2 (CL = 1) | N/A | 00 | |
| 27 | Minimum Row Precharge Time (t_{RP}) | 20.0ns | 14 | |
| 28 | Minimum Row Active to Row Active delay (t_{RBD}) | 20.0ns | 14 | |
| 29 | Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t_{RCD}) | 20.0ns | 14 | |
| 30 | Minimum $\overline{\text{RAS}}$ Pulse width (t_{RAS}) | 50.0ns | 32 | |

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency).
2. Minimum application clock cycle time is 10ns for -260 CL=2 and for -360 CL=3 and 15ns for -360 CL=2.
3. cc = Checksum Data byte, 00-FF (Hex).
4. "R" = Alphanumeric revision code, A-Z, 0-9.
5. rr = ASCII coded revision code byte "R".
6. ww = Binary coded decimal week code, 01-52 (Decimal) ' 01-34 (Hex).
7. yy = Binary coded decimal year code, 00-99 (Decimal) ' 00-63 (Hex).
8. ss = Serial number data byte, 00-FF (Hex).



Serial Presence Detect (Part 2 of 2)

| Byte # | Description | SPD Entry Value | Serial PD Data Entry (Hexadecimal) | Notes |
|-----------|--|---------------------------------|--------------------------------------|-------|
| 31 | Module Bank Density | 256MB | 40 | |
| 32 | Address and Command Setup Time Before Clock | 2.0ns | 20 | |
| 33 | Address and Command Hold Time After Clock | 1.0ns | 10 | |
| 34 | Data Input Setup Time Before Clock | 2.0ns | 20 | |
| 35 | Data Input Hold Time After Clock | 1.0ns | 10 | |
| 36 - 61 | Reserved | Undefined | 00 | |
| 62 | SPD Revision | PC100 1.2A | 12 | |
| 63 | Checksum for bytes 0 - 62 | Checksum Data | cc | 3 |
| 64 - 71 | Manufacturers' JEDEC ID Code | IBM | A400000000000000 | |
| 72 | Assembly Manufacturing Location | Toronto, Canada | 91 | |
| | | Vimercate, Italy | 53 | |
| 73 - 90 | Assembly Part Number | -260 ASCII '13M32734CC"R"-260T' | 31334D33323733344343rr2D323630542020 | 4, 5 |
| | | -360 ASCII '13M32734CC"R"-360T' | 31334D33323733344343rr2D333630542020 | |
| 91 - 92 | Assembly Revision Code | "R" plus ASCII blank | rr20 | 5 |
| 93 - 94 | Assembly Manufacturing Date | Year/Week Code | yyww | 6, 7 |
| 95 - 98 | Assembly Serial Number | Serial Number | ssssssss | 8 |
| 99 - 125 | Reserved | Undefined | Not Specified | |
| 126 | Module Supports this Clock Frequency | 100MHz | 64 | |
| 127 | Attributes for clock frequency defined in Byte 126 | -260 CLK0, CL=2,3, ConAP | 87 | |
| | | -360 CLK0 CL=3, ConAP | 85 | |
| 128 - 255 | Open for Customer Use | Undefined | 00 | |

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency).
2. Minimum application clock cycle time is 10ns for -260 CL=2 and for -360 CL=3 and 15ns for -360 CL=2.
3. cc = Checksum Data byte, 00-FF (Hex).
4. "R" = Alphanumeric revision code, A-Z, 0-9.
5. rr = ASCII coded revision code byte "R".
6. ww = Binary coded decimal week code, 01-52 (Decimal) ' 01-34 (Hex).
7. yy = Binary coded decimal year code, 00-99 (Decimal) ' 00-63 (Hex).
8. ss = Serial number data byte, 00-FF (Hex).



Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units | Notes |
|-----------|---------------------------------|------------------|--------------|-------|
| V_{DD} | Power Supply Voltage | -0.3 to +4.6 | | |
| V_{IN} | Input Voltage | SDRAM Devices | -1.0 to +4.6 | V 1 |
| | | Serial PD Device | -0.3 to +6.5 | |
| | | Register | 0 - V_{DD} | |
| | | PLL | 0 - V_{DD} | |
| V_{OUT} | Output Voltage | SDRAM Devices | -1.0 to +4.6 | |
| | | Serial PD Device | -0.3 to +6.5 | |
| T_A | Operating Temperature (ambient) | 0 to +70 | °C | 1 |
| T_{STG} | Storage Temperature | -55 to +125 | °C | 1 |
| P_D | Power Dissipation | 11.4 | W | 1, 2 |
| I_{OUT} | Short Circuit Output Current | 50 | mA | 1 |
| F_{MIN} | Minimum Operating Frequency | 66 | MHz | |

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power is calculated assuming the physical bank is in Auto Refresh Mode.

Recommended DC Operating Conditions ($T_A = 0$ to 70°C)

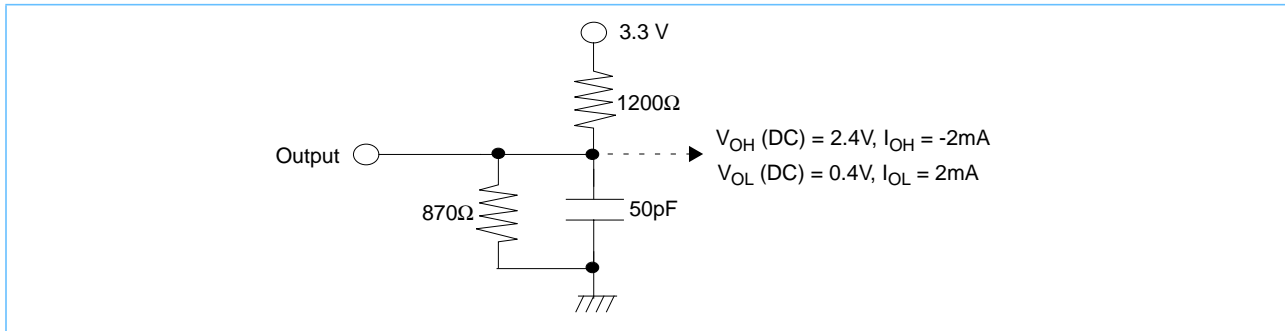
| Symbol | Parameter | Rating | | | Units | Notes |
|----------|--------------------|--------|------|----------------|-------|-------|
| | | Min. | Typ. | Max. | | |
| V_{DD} | Supply Voltage | 3.0 | 3.3 | 3.6 | V | 1 |
| V_{IH} | Input High Voltage | 2.0 | — | $V_{DD} + 0.3$ | V | 1 |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V | 1 |

1. All voltages referenced to V_{SS} .

**Capacitance** ($T_A=25^\circ\text{C}$, $f=1\text{MHz}$, $V_{DD}=3.3\text{V} \pm 0.3\text{V}$)

| Symbol | Parameter | Organization | Units |
|------------------|---|--------------|-------|
| | | x72 Max. | |
| C _{I1} | Input Capacitance (A0 - A9, A10/AP, BA0, BA1, A11) | 10.5 | pF |
| C _{I2} | Input Capacitance ($\overline{\text{RAS}}$) | 9 | pF |
| C _{I3} | Input Capacitance ($\overline{\text{CAS}}$) | 9.5 | pF |
| C _{I4} | Input Capacitance ($\overline{\text{S0}}$, $\overline{\text{S2}}$) | 12 | pF |
| C _{I5} | Input Capacitance (CKE0) | 19 | pF |
| C _{I6} | Input Capacitance (CK0) | 28 | pF |
| C _{I7} | Input Capacitance (DQMB0 - DQMB7) | 11 | pF |
| C _{I8} | Input Capacitance (SA0 - SA2, SCL, WP) | 9 | pF |
| C _{I9} | Input Capacitance (REGE) | 10 | pF |
| C _{I10} | Input Capacitance (CK1 - CK3) | 16 | pF |
| C _{I11} | Input Capacitance (WE) | 11 | pF |
| C _{IO1} | Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7) | 16 | pF |
| C _{IO2} | Input/Output Capacitance (SDA) | 11 | pF |

DC Output Load Circuit



Input/Output Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3V ± 0.3V)

| Symbol | Parameter | x72 | | Units | Notes | |
|-------------------|--|----------------------------|-----------------|-------|-------|----|
| | | Min. | Max. | | | |
| I _{I(L)} | Input Leakage Current, any input (0.0V ≤ V _{IN} ≤ 3.6V), All Other Pins Not Under Test = 0V | Address and Control Inputs | | 10 | 10 | μA |
| | | DQ0-63, CB0 - 7 | | -2 | +2 | |
| I _{O(L)} | Output Leakage Current (D _{OUT} is disabled, 0.0V ≤ V _{OUT} ≤ 3.6V) | DQ0-63, CB0 - 7 | | -2 | +2 | μA |
| | | SDA | | -1 | +1 | |
| V _{OH} | Output Level Output "H" Level Voltage (I _{OUT} = -2.0mA) | 2.4 | V _{DD} | V | 1 | |
| V _{OL} | Output Level Output "L" Level Voltage (I _{OUT} = +2.0mA) | 0.0 | 0.4 | | | |

1. See DC output load circuit.

Operating, Standby, and Refresh Currents ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

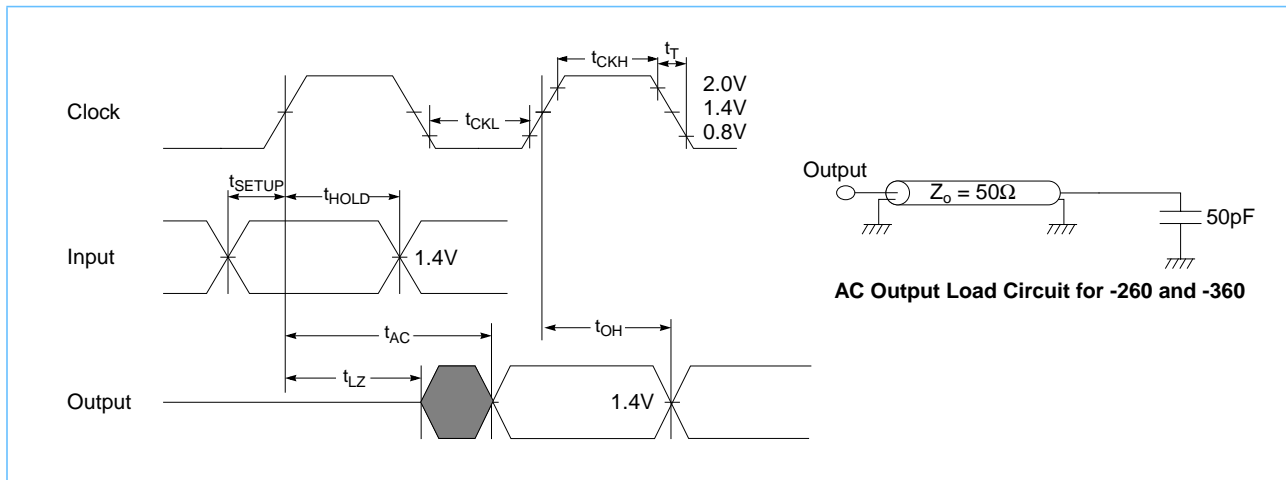
| Parameter | Symbol | Test Condition | Clock Cycle | | Units | Notes |
|--|-------------|---|-------------|------|-------|-------|
| | | | 10ns | 15ns | | |
| Operating Current 1 bank operation | I_{CC1} | $t_{RC} = t_{RC}(\text{min})$, $t_{CK} = \text{min}$ Active-Precharge command cycling without burst operation | 1692 | 1354 | mA | 1 |
| Precharge Standby Current in Power Down Mode | I_{CC2P} | $\text{CKE0} \leq V_{IL}(\text{max})$, $t_{CK} = \text{min}$, $\overline{\text{CS}} = V_{IH}(\text{min})$ | 270 | 202 | mA | 1 |
| | I_{CC2PS} | $\text{CKE0} \leq V_{IL}(\text{max})$, $t_{CK} = \text{Infinity}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$ | 33 | 33 | mA | |
| Precharge Standby Current in Non- Power Down Mode | I_{CC2N} | $\text{CKE0} \geq V_{IH}(\text{min})$, $t_{CK} = \text{min}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$ | 882 | 598 | mA | 1 |
| | I_{CC2NS} | $\text{CKE0} \geq V_{IH}(\text{min})$, $t_{CK} = \text{Infinity}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$ | 195 | 195 | mA | |
| No Operating Current (Active state: 4bank) | I_{CC3N} | $\text{CKE0} \geq V_{IH}(\text{min})$, $t_{CK} = \text{min}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$ | 972 | 904 | mA | 1 |
| | I_{CC3P} | $\text{CKE0} \leq V_{IL}(\text{max})$, $t_{CK} = \text{min}$, $\overline{\text{S0}}, \overline{\text{S2}} = V_{IH}(\text{min})$ (Power Down Mode) | 432 | 364 | mA | 1 |
| Burst Operating Current (Active state: 4bank) | I_{CC4} | $t_{CK} = \text{min}$, Read command cycling | 1872 | 1264 | mA | 1, 2 |
| Auto (CBR) Refresh Current | I_{CC5} | $t_{CK} = \text{min}$, CBR command cycling | 3159 | 2702 | mA | 1 |
| Self Refresh Current | I_{CC6} | $\text{CKE0} \leq 0.2\text{V}$ | 51 | 51 | mA | |

1. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC} . Input signals are changed once during $t_{CK}(\text{min})$. $t_{CK}(\text{min}) = 10\text{ns}$ for -260 CL=2 and for -360 CL=3 and 15ns for -360 CL=2.
2. The specified values are obtained with the DIMM data outputs open.

AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

1. An initial pause of $200\mu\text{s}$, with CKE0 held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. AC timing tests have $V_{IL} = 0.8\text{V}$ and $V_{IH} = 2.0\text{V}$ with the timing referenced to the 1.4V crossover point.
3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume $t_T = 1.2\text{ns}$ (1 Volt/ns rise time).
5. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
6. A 1 ms stabilization time is required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal.

AC Characteristics Diagrams





Clock and Clock Enable Parameters

| Symbol | Parameter | | -260 max. (Device CL, t_{RCD} : t_{RP} = 2, 2, 2) | | -360 max. (Device CL, t_{RCD} : t_{RP} = 3, 2, 2) | | Units | Notes |
|------------------|---|------------|--|------|--|------|-------|-------|
| | | | Min. | Max. | Min. | Max. | | |
| t_{CK4} | Clock Cycle Time, DIMM $\overline{\text{CAS}}$ Latency = 4 | Registered | 10 | 1000 | 10 | 1000 | ns | 1 |
| t_{CK3} | Clock Cycle Time, DIMM $\overline{\text{CAS}}$ Latency = 3 | Registered | 10 | 1000 | 15 | 1000 | ns | 1 |
| | | Buffered | 10 | 1000 | 10 | 1000 | ns | |
| t_{CK2} | Clock Cycle Time, DIMM $\overline{\text{CAS}}$ Latency = 2 | Buffered | 10 | 1000 | 15 | 1000 | ns | 1 |
| t_{AC4} | Clock Access Time, DIMM $\overline{\text{CAS}}$ Latency = 4 | Registered | — | 7.2 | — | 7.2 | ns | 1, 2 |
| t_{AC3} | Clock Access Time, DIMM $\overline{\text{CAS}}$ Latency = 3 | Registered | — | 7.2 | — | 10.2 | ns | 1, 2 |
| | | Buffered | — | 7.2 | — | 7.2 | ns | |
| t_{AC2} | Clock Access Time, DIMM $\overline{\text{CAS}}$ Latency = 2 | Buffered | — | 7.2 | — | 10.2 | ns | 1, 2 |
| t_{CKH} | Clock High Pulse Width | | 3 | — | 3 | — | ns | 3 |
| t_{CKL} | Clock Low Pulse Width | | 3 | — | 3 | — | ns | 3 |
| t_{CES} | Clock Enable Setup Time | Registered | 2.0 | — | 2.0 | — | ns | 1 |
| | | Buffered | 7.2 | — | 7.2 | — | ns | |
| t_{CEH} | Clock Enable Hold Time | Registered | 1.0 | — | 1.0 | — | ns | 1 |
| | | Buffered | 0.2 | — | 0.2 | — | ns | |
| t_{SB} | Power down mode Entry Time | | 0 | 10 | 0 | 10 | ns | |
| t_{T} | Transition Time (Rise and Fall) | | 0.5 | 10 | 0.5 | 10 | ns | |

1. DIMM $\overline{\text{CAS}}$ latency = device CL [clock cycles] + 1 for Register mode; DIMM $\overline{\text{CAS}}$ latency is one clock less for Buffer mode.
2. Access time is measured at 1.4V. See AC output load circuit.
3. t_{CKH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max).



Common Parameters

| Symbol | Parameter | -260 | | -360 | | Units | Notes | |
|------------------|---|------------|--------|------|--------|-------|-------|------|
| | | Min. | Max. | Min. | Max. | | | |
| t _{CS} | Command Setup Time | Registered | 2.0 | — | 2.0 | — | ns | 1, 2 |
| | | Buffered | 7.4 | — | 7.4 | — | ns | |
| t _{CH} | Command Hold Time | Registered | 1.1 | — | 1.0 | — | ns | 1, 2 |
| | | Buffered | 0.0 | — | 0.0 | — | ns | |
| t _{AS} | Address and Bank Select Setup Time | Registered | 2.0 | — | 2.0 | — | ns | 1, 2 |
| | | Buffered | 7.4 | — | 7.4 | — | ns | |
| t _{AH} | Address and Bank Select Hold Time | Registered | 1.0 | — | 1.0 | — | ns | 1, 2 |
| | | Buffered | 0.0 | — | 0.0 | — | ns | |
| t _{RCD} | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay | 20 | — | 20 | — | ns | 1 | |
| t _{RC} | Bank Cycle Time | 70 | — | 70 | — | ns | 1 | |
| t _{RAS} | Active Command Period | 50 | 100000 | 50 | 100000 | ns | 1 | |
| t _{RP} | Precharge Time | 20 | — | 20 | — | ns | 1 | |
| t _{RRD} | Bank to Bank Delay Time | 20 | — | 20 | — | ns | 1 | |
| t _{CCD} | $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay Time (Same Bank) | 1 | — | 1 | — | CLK | | |

1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock as follows: the number of clock cycles = specified value of timing/clock period (count fractions as a whole number).
2. The set up and hold times refer to the addition of the register. Note that although the Buffered set up times appear much greater, there is no additional clock cycle as there is in Registered mode.

Mode Register Set Cycle

| Symbol | Parameter | -260 | | -360 | | Units | Notes |
|------------------|------------------------------|------|------|------|------|-------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t _{RSC} | Mode Register Set Cycle Time | 2 | — | 2 | — | CLK | 1 |

1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock as follows: the number of clock cycles = specified value of timing/clock period (count fractions as a whole number).

Refresh Cycle

| Symbol | Parameter | -260 | | -360 | | Units | Notes |
|------------------|----------------|------|------|------|------|-------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t _{REF} | Refresh Period | — | 64 | — | 64 | ms | 1 |

1. 4096cycles.



Read Cycle

| Symbol | Parameter | -260 | | -360 | | Units | Notes |
|-----------|---------------------------------|------------|------|------|------|-------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t_{OH} | Data Out Hold Time | 3.6 | — | 3.6 | — | ns | |
| t_{LZ} | Data Out to Low Impedance Time | 0.6 | — | 0.6 | — | ns | |
| t_{HZ3} | Data Out to High Impedance Time | 3.6 | 7.2 | 3.5 | 7.2 | ns | 1 |
| t_{HZ2} | Data Out to High Impedance Time | 3.6 | 7.2 | 3.6 | 9.2 | ns | 1 |
| t_{DQZ} | DQM Data Out Disable Latency | Registered | 3 | — | 3 | — | CLK |
| | | Buffered | 2 | — | 2 | — | CLK |

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Write Cycle

| Symbol | Parameter | -260 | | -360 | | Units | |
|------------|------------------------------|------------|------|------|------|-------|-----|
| | | Min. | Max. | Min. | Max. | | |
| t_{DS} | Data In Setup Time | 2.1 | — | 2.1 | — | ns | |
| t_{DH} | Data In Hold Time | 1.6 | — | 1.6 | — | ns | |
| t_{DPL} | Data input to Precharge | Registered | 10 | — | 10 | — | ns |
| | | Buffered | 20 | — | 20 | — | ns |
| t_{DAL3} | Data input to Active, CL = 3 | Registered | 4 | — | 4 | — | CLK |
| | | Buffered | 5 | — | 5 | — | CLK |
| t_{DAL2} | Data input to Active CL = 2 | Registered | 4 | — | 4 | — | CLK |
| | | Buffered | 5 | — | 5 | — | CLK |
| t_{DQW} | DQM Write Mask Latency | Registered | 1 | — | 1 | — | CLK |
| | | Buffered | 0 | — | 0 | — | CLK |

Presence Detect Read and Write Cycle

| Symbol | Parameter | Min. | Max. | Units | Notes |
|--------------|---|------|------|---------|-------|
| f_{SCL} | SCL Clock Frequency | — | 100 | KHz | |
| T_I | Noise Suppression Time Constant at SCL, SDA Inputs | — | 100 | ns | |
| t_{AA} | SCL Low to SDA Data Out Valid | 0.3 | 3.5 | μ s | |
| t_{BUF} | Time the Bus Must Be Free before a New Transmission Can Start | 4.7 | — | μ s | |
| $t_{HD:STA}$ | Start Condition Hold Time | 4.0 | — | μ s | |
| t_{LOW} | Clock Low Period | 4.7 | — | μ s | |
| t_{HIGH} | Clock High Period | 4.0 | — | μ s | |
| $t_{SU:STA}$ | Start Condition Setup Time (for a Repeated Start Condition) | 4.7 | — | μ s | |
| $t_{HD:DAT}$ | Data in Hold Time | 0 | — | μ s | |
| $t_{SU:DAT}$ | Data in Setup Time | 250 | — | ns | |
| t_R | SDA and SCL Rise Time | — | 1 | μ s | |
| t_F | SDA and SCL Fall Time | — | 300 | ns | |
| $t_{SU:STO}$ | Stop Condition Setup Time | 4.7 | — | μ s | |
| t_{DH} | Data Out Hold Time | 300 | — | ns | |
| t_{WR} | Write Cycle Time | — | 15 | ms | 1 |

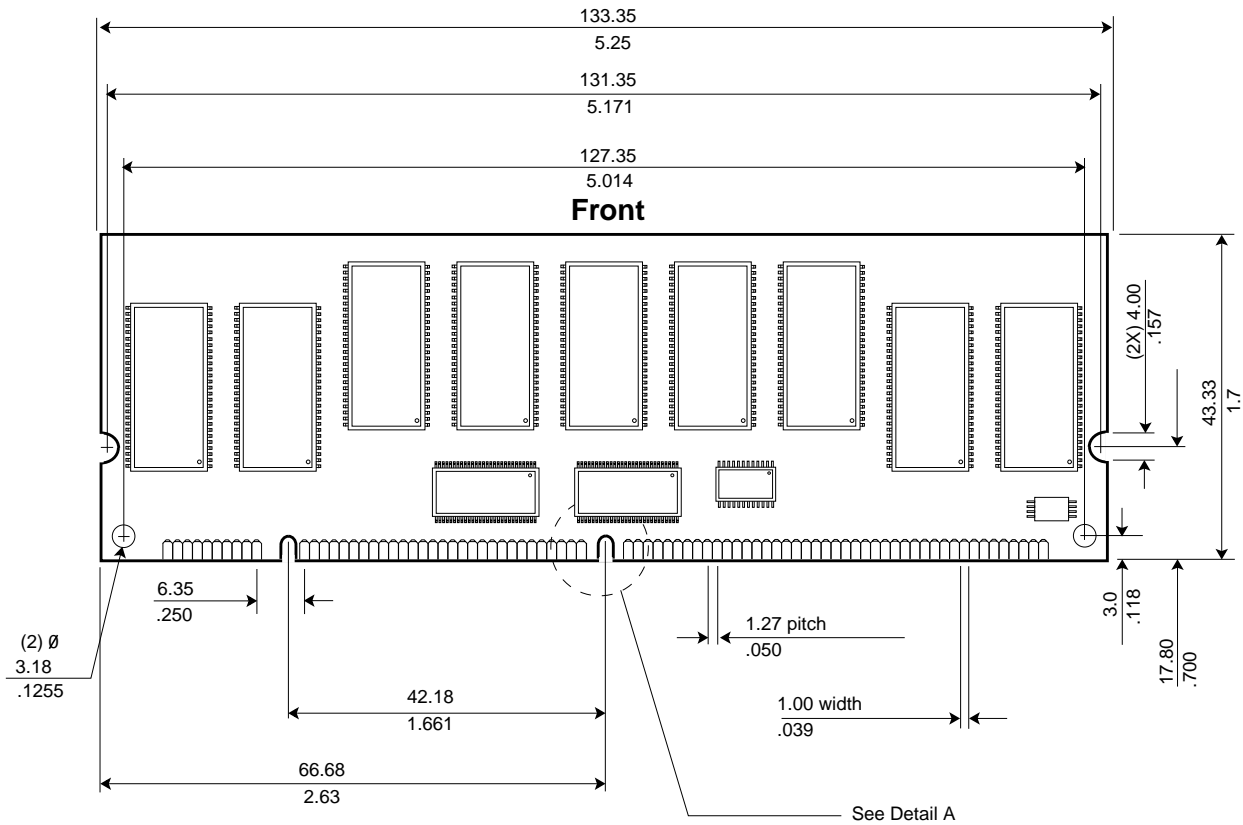
1. The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Functional Description and Timing Diagrams

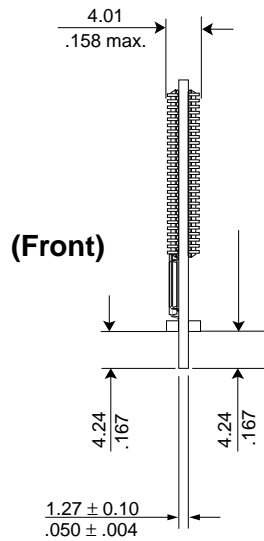
Refer to the IBM 128Mb Synchronous DRAM Die Revision A datasheet (Document 33L8019) for the functional description and timing diagrams for buffered-mode operation.

Refer to the IBM Application Notes *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

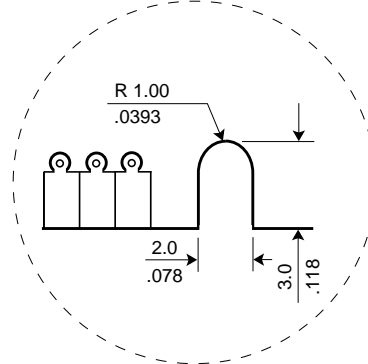
Layout Drawing



Side



Detail A Scale: 4/1



Note: All dimensions are typical unless otherwise stated. $\frac{\text{Millimeters}}{\text{Inches}}$



Revision Log

| Rev | Contents of Modification |
|-------|--------------------------|
| 7/99 | Initial release |
| 10/99 | Made minor updates. |



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