HI-REL DATA SHEET

HM 65262

16 k x 1
VERY LOW POWER CMOS SRAM

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FEATURES

- ACCESS TIME : 70/85 ns
- VERY LOW POWER CONSUMPTION
  ACTIVE : 110 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED

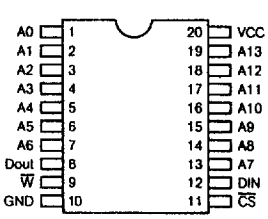
DESCRIPTION

The HM 65262 is a very low power CMOS static RAM organized as 16384 x 1 bit. It is manufactured using the MHS high performance CMOS technology.
The HM 65262 is a "Pure CMOS SRAM" utilizing an array of six transistor (6T) memory cells permitting the lowest possible standby supply current over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise and alpha particles, and in addition improves the tolerance of the RAM to cumulated dose radiation.
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate thus making the HM 65162 "Latch-up immune".
All inputs and outputs of the HM 65262 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65262 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

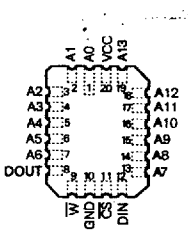
PACKAGES

Ceramic 300 mils, 20 pins, DIL. LCC, 20 pins.

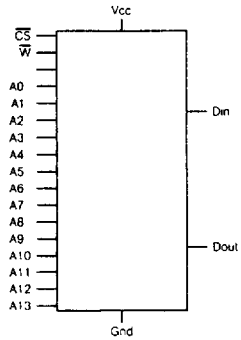
Pinout DIL 20 pins (top view)



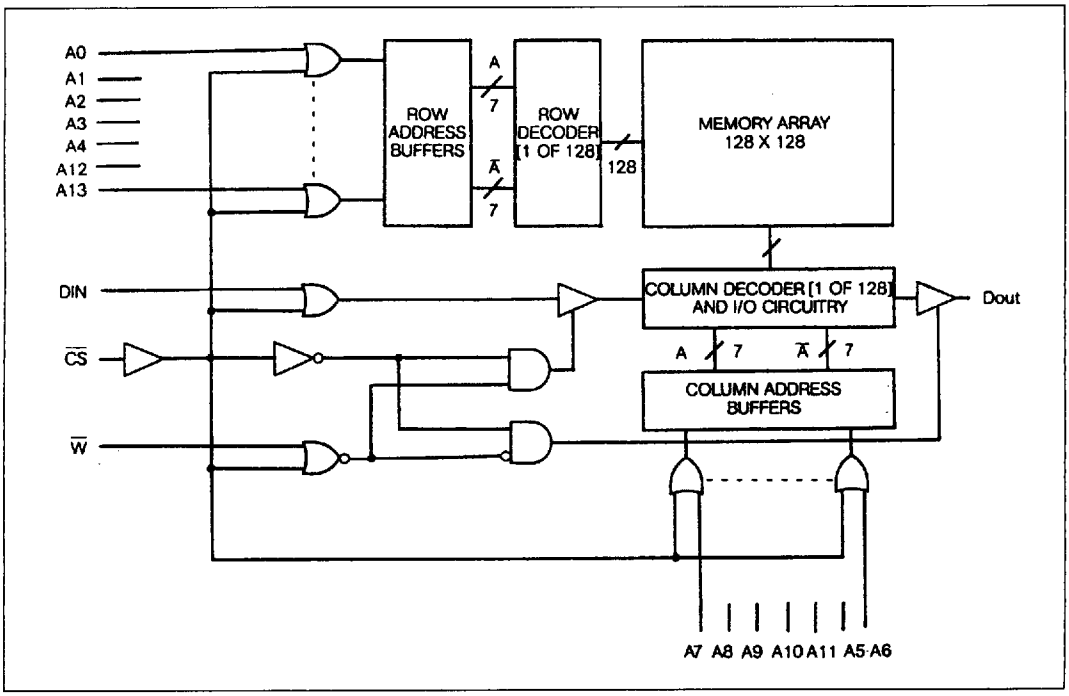
Pinout LCC 20 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A13 : Address inputs	$\overline{W}$: Write enable
Din : Input	VCC : Power
Dout : Output	GND: Ground
$\overline{CS}$: Chip Select	

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect/Power down
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.3 V to + 7.0 V
Input or Output voltage applied : (GND - 0.3 V) to (Vcc + 0.3 V)
Storage temperature : - 65°C to + 150°C
Electro static discharge voltage > 1500 V (MIL STD 883, METHOD 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	Vcc = 5 V ± 10 %	- 55°C to + 125°C
Industrial	Vcc = 5 V ± 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS

DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65262 B	65262	65262 C	Unit	Value	Note 8
ICCSB (1)	Standby supply current (I/M)	3/5	3/5	3/5	mA	Max	M
ICCSB1 (2)	Standby supply current (I/M)	5/50	5/50	100/500	µA	Max	M
ICCOP (3)	Operating supply current	50	50	50	mA	Max	M
ICC (4)	Operating supply current	50	50	50	mA	Max	M
II/O (5)	Input/Output leakage current	+ / - 1	+ / - 1	+ / - 1	µA	Max	M
VIL (6)	Input low voltage	0.8	0.8	0.8	V	Max	T
VIH (6)	Input high voltage	2.2	2.2	2.2	V	Min	T
VOL (7)	Output low voltage	0.4	0.4	0.4	V	Max	M
VOH (7)	Output high voltage	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	8	8	8	pF	Max	G
C OUT	Output capacitance	8	8	8	pF	Max	G

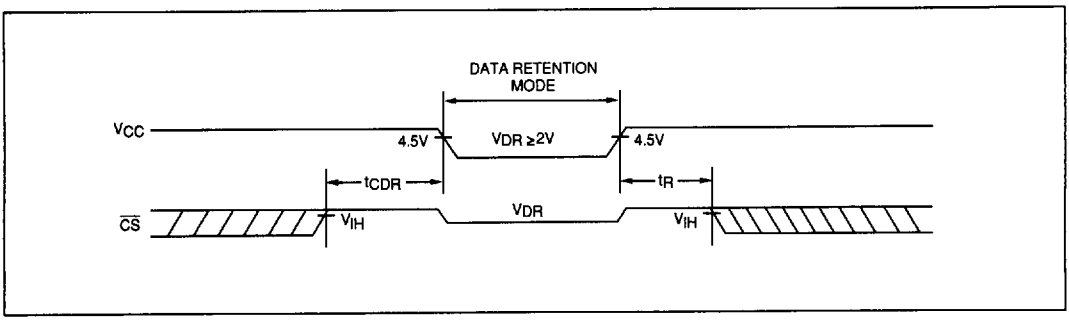
Notes :
1. $\overline{CS}$ > = VIH, I = Industrial temperature range, M = Military temperature range
2. $\overline{CS}$ > = Vcc - 0.3V, Output current = 0 mA
3. Vcc max, Iout = 0 mA, Duty cycle 100 %, F = 1 MHz and 5 mA / MHz, Vin = Vcc / Gnd
4. $\overline{CS}$ ≤ VIL, Iout = 0 mA, Vin = Gnd to Vcc
5. Vcc = 5.5V, Vin = Gnd to Vcc
6. VIH max = Vcc + 0.3V, VIL min = - 0.3V or - 1V pulse width 50 ns.
7. Vcc min, IOL = 8 mA, IOH = - 4 mA
8. Including open/short test or inputs clamp voltage.
   G - Guaranted - Not tested : Parameter measured at design validation and at any design change.
   M - Measured : Parameter measured and data-log capability.
   T - Tested : Parameter verification during testing.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1 . Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2 . $\overline{CS}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
4 . The RAM can begin operation > 70 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



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DATA RETENTION MODE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM (12)	UNIT	NOTE 8
VCCDR	Vcc for data retention	2.0	—	—	V	T
TCDR	Chip deselect to data retention time	0.0	—	—	ns	
TR	Operation recovery time	TAVAV (10)	—	—	ns	
ICCDR1 (11)	Data retention current @ 2.0 V : HM-65262(B)	—	0.1	3/20.0	µA	M
	HM-65262C	—	0.1	30/200.0	µA	M
ICCDR2 (11)	Data retention current @ 3.0 V : HM-65262(B)	—	0.3	3/30	µA	G
	HM-65262C	—	0.3	50/300.0	µA	G

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.
12. I = Industrial, M = Military.

ELECTRICAL CHARACTERISTICS
AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)

Conditions :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
VCC : 5 V ± 10 %

Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 100 pF

WRITE CYCLE : Industrial and military specification

SYMBOL	PARAMETER *	65262 B	65262	65262 C	UNIT	VALUE
TAVAV	Write cycle time	70	85	85	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	55	65	65	ns	min
TDVWH	Data set-up time	40	45	45	ns	min
TELWH	$\overline{CS}$ low to write end	55	65	65	ns	min
TWLQZ (12)	Write low to high Z	50	50	50	ns	max
TWLWH	Write pulse width	55	65	65	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

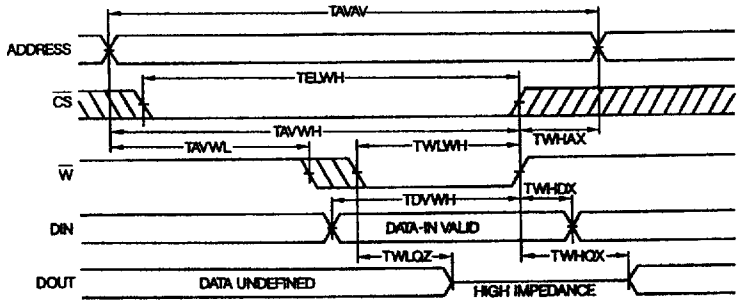
READ CYCLE : Industrial and military specification

SYMBOL	PARAMETER *	65262 B	65262	65262 C	UNIT	VALUE
TAVAV	READ cycle time	70	85	85	ns	min
TAVQV	Address access time	70	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	70	85	85	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	40	40	40	ns	max

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

* : All parameters only tested and screened during full speed functional test.
For subgroups 7 and 8, functional test is performed at 1 MHz with VIL = OV and VIH = 3V.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (note 13)



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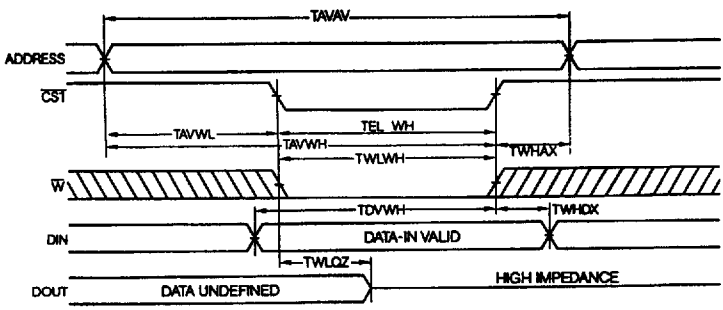
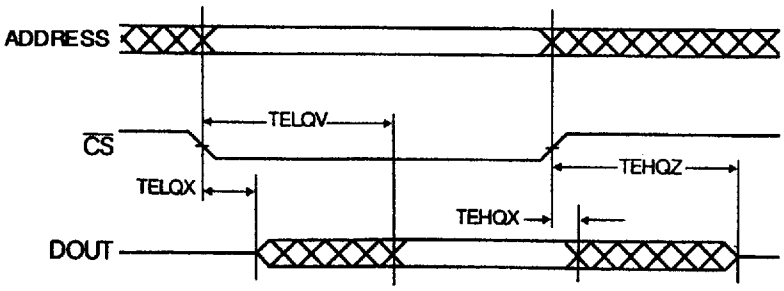
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED) (note 13)

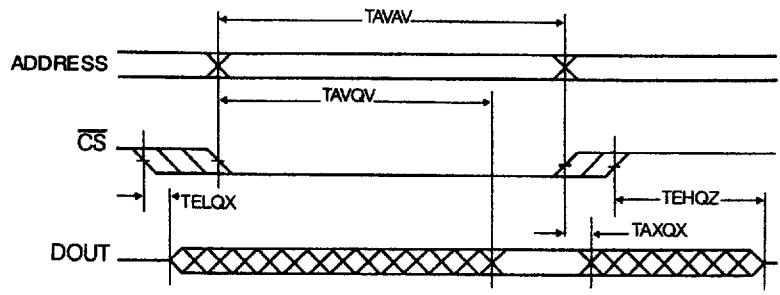


Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

READ CYCLE nb 1



READ CYCLE nb 2



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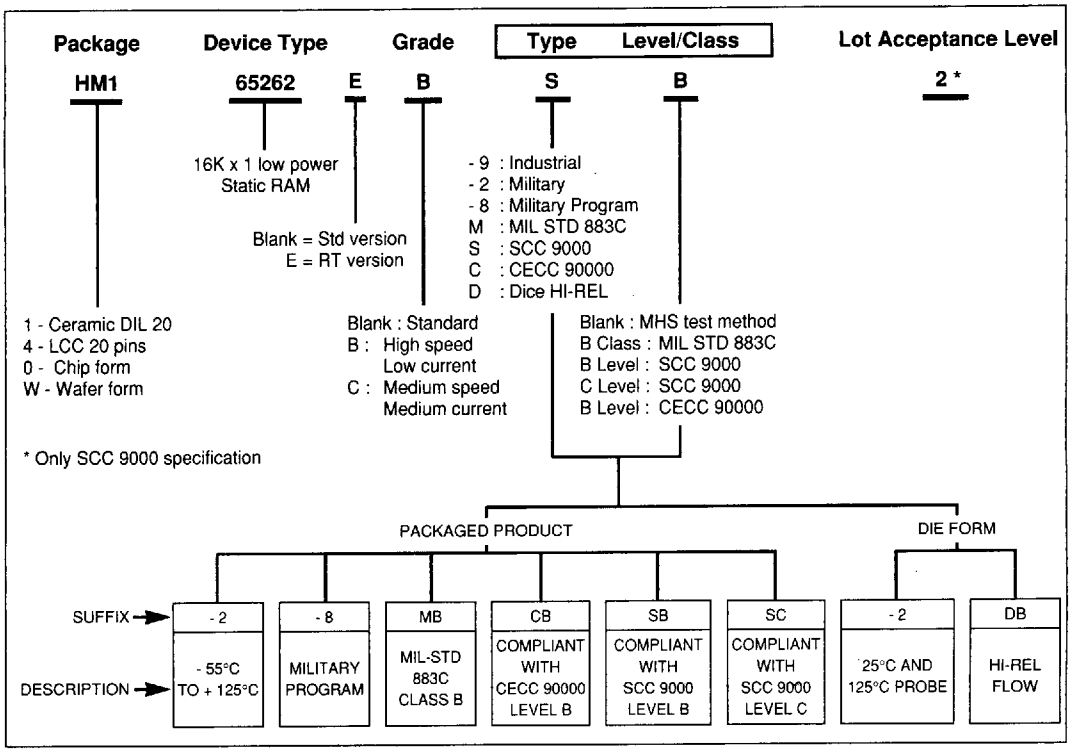
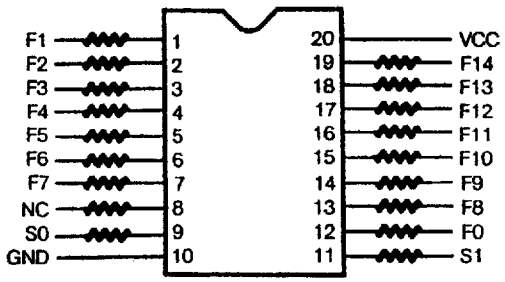
ORDERING INFORMATION



BURN IN SCHEMATICS



R = 1K Ω

Fo = 25 KHz ± 20 %

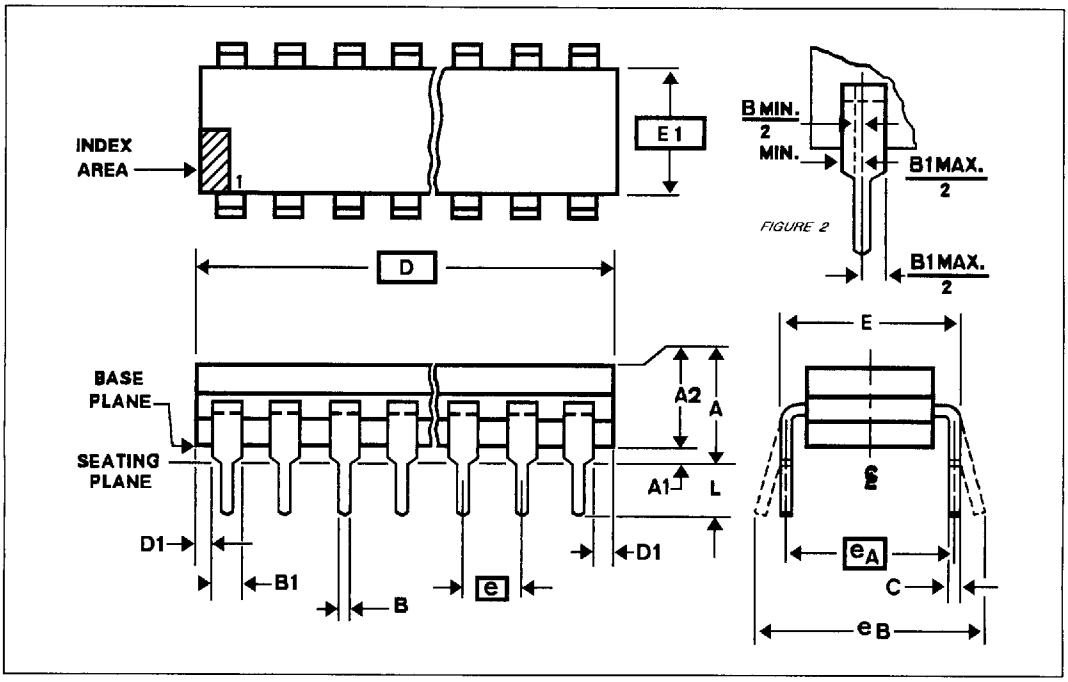
Fn = 1/2 F n-1

S0, S1 : programmable signals for write / read cycle

VCC = 5.5V

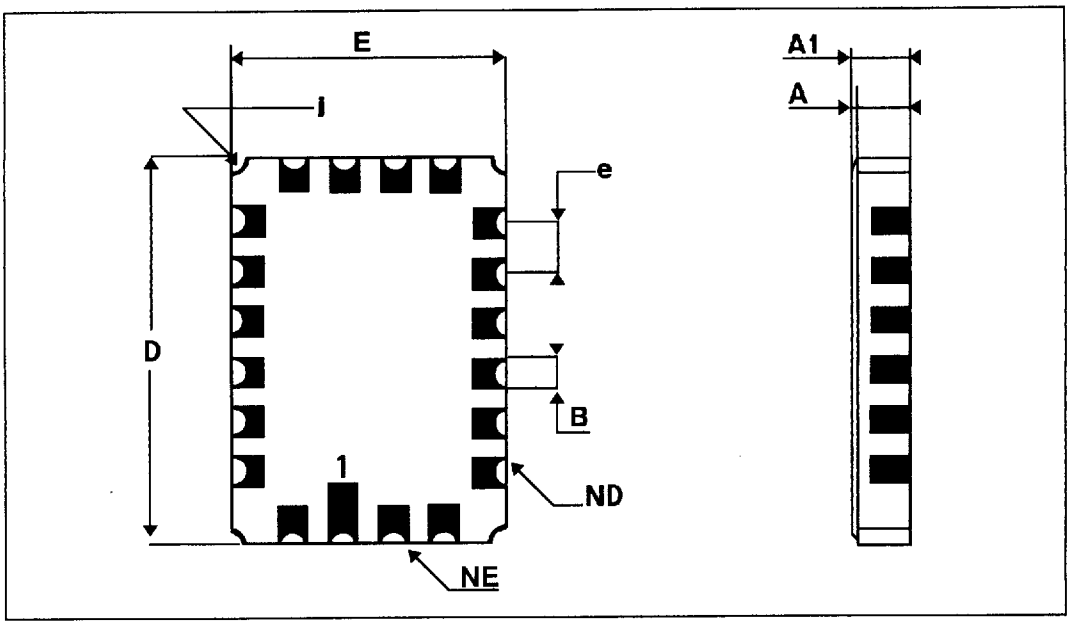
NC = Not connected

PACKAGE OUTLINES



20 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	—	0.18	3.81	0.38	0.76	0.20	23.87	0.13	8.00	7.24	2.54	7.90	8.08	3.17
	MAX	5.71	—	4.95	0.58	1.78	0.38	24.63	—	8.38	7.87	BSC	BSC	10.82	3.81
INCHES	MIN	—	.007	.150	.015	.030	.008	.940	.005	.315	.285	.100	.311	.318	.125
	MAX	.225	—	.195	.023	.070	.015	.970	—	.330	.310	BSC	BSC	.426	.150



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20 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER

		A	A1	B	D	E	e	h	j	ND	NE
MM	MIN	1.24	1.50	0.53	10.64	7.21	1.27	—	0.30	6	4
	MAX	1.93	2.23	0.76	10.94	7.52	BSC	—	RAD		
INCHES	MIN	.049	.059	.021	.419	.284	.050	—	.012	6	4
	MAX	.076	.088	.030	.431	.296	BSC	—	RAD		