REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Table I, change parameter I_{CC}. Figure 1, change to case outline U. Change vendor FSCM to vendor CAGE.	18 May 87	

REV																																
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REV STATUS	REV	A			A						A											A										
OF PAGES	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20											

Defense Electronics Supply Center Dayton, Ohio	PREPARED BY	**MILITARY DRAWING** This drawing is available for use by all Departments and Agencies of the Department of Defense
Original date of drawing: 16 May 1986	CHECKED BY	TITLE: MICROCIRCUITS, DIGITAL 16-BIT BIPOLAR MICROCONTROLLER, MONOLITHIC SILICON
AMSC N/A	APPROVED BY	
	SIZE A / CODE IDENT. NO. 14933	DWG NO. 5962-85503
	REV A	PAGE 1 OF 20

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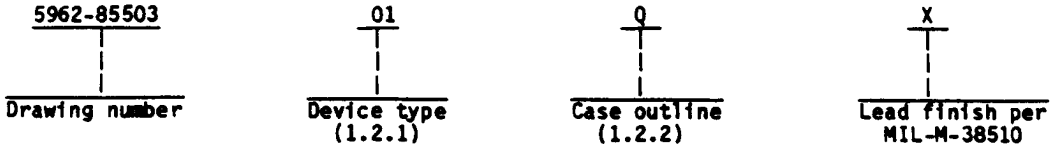
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193

1. SCOPE

1.1 Scope. This drawing describes the requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	8X320	16-bit bipolar microcontroller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2-1/16"), dual-in-line package
U	C-5 (44-terminal, .650" x .650"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.3 V dc to +7.0 V dc
Input voltage	-0.3 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, (P_D) 1/	1.5 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	See MIL-M-38510, appendix C
Case U	25°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	5.0 V dc ±10%
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high level input voltage (logic inputs)	2.0 V dc
Maximum low level input voltage (logic inputs)	0.8 V dc
Minimum high level output voltage	2.4 V dc
Maximum low level output voltage	0.5 V dc
Maximum frequency of operation	8.0 MHz

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$		Group A subgroups	Limits Min	Limits Max	Unit
Low level input voltage	V_{IL}	$4.5\ V \le V_{CC} \le 5.5\ V$		1,2,3		.8	V
High level input voltage	V_{IH}	$4.5\ V \le V_{CC} \le 5.5\ V$		1,2,3	2.0		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5\ V$, $I_{OL} = 16\ mA$		1,2,3		.5	V
High level output voltage	V_{OH}	$V_{CC} = 4.5\ V$, $I_{OH} = -3\ mA$		1,2,3	2.5		V
Input clamp voltage	V_{IC}	$V_{CC} = 4.5\ V$, $I_I = -18\ mA$		1,2,3		-1.5	V
Supply current	I_{CC}	$V_{CC} = 5.5\ V$		1 2 3		260 210 300	mA mA mA
Short circuit 3/ output current	I_{OS}	$V_{CC} = 5.5\ V$		1,2,3	-20	-100	mA
WC, MCLK, SC, and $\overline{ME}$	I_{IL}	$V_{CC} = 5.5\ V$, $V_{IL} = 0.5\ V$		1,2,3		-1.0	mA
B/$\overline{W}$				1,2,3		-1.6	mA
A0-A3				1,2,3		-1.0	mA
$\overline{DMAE}$				1,2,3		-800	µA
WS, $\overline{PIOE}$, and R/$\overline{W}$				1,2,3		-400	µA
$\overline{IV0}$-$\overline{IV7}$				1,2,3		-400 each line	µA
DO_A-$D7_A$/DO_B-$D7_B$				1,2,3		-400 each line	µA
WC, SC, MCLK, and $\overline{ME}$	I_{IH}	$V_{CC} = 5.5\ V$, $V_{IH} = 5.5\ V$		1,2,3		100	µA
B/$\overline{W}$				1,2,3		240	µA
AD				1,2,3		120	µA
A1-A3				1,2,3		60	µA
$\overline{DMAE}$				1,2,3		120	µA
WS, $\overline{PIOE}$, and R/$\overline{W}$				1,2,3		60	µA
$\overline{IV0}$-$\overline{IV7}$ and DO_A-$D7_A$/DO_B-$D7_B$				1,2,3		100	µA
		FROM	TO				
Address access time	T_{AA}	A3-A0 A3-A0	DO_A-$D7_A$/ DO_B-$D7_B$	9,10,11		65	ns
Primary port enable time	T_{CE}	+ $\overline{PIOE}$ + $\overline{DMAE}$	DO_A-$D7_A$/ DO_B-$D7_B$	9,10,11		30	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ FROM	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ TO	Group A subgroups	Limits Min	Limits Max	Unit
Primary port disable time	T_{CD}	+ $\overline{PIOE}$ + $\overline{DMAE}$	DO_A-$D7_A$/ DO_B-$D7_B$	9,10,11		35	ns
Address setup time	T_{WSA}	A3-A0	+ WS	9,10,11	60		ns
Address hold time	T_{WHA}	+ WS	A3-A0	9,10,11	0		ns
Primary port data setup time	T_{WSD}	DO_A-$D7_A$/ DO_B-$D7_B$	WS	9,10,11	30		ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ 4.5 V ≤ V_{CC} ≤ 5.5 V, -55°C ≤ T_C ≤ +125°C		Group A subgroups	Limits		Unit
		FROM	TO		Min	Max	
Primary port data hold time	T_{WHD}	WS	DO_A-$D7_A$/ DO_B-$D7_B$	9,10,11	5		ns
Write mode control setup time	T_{WSC}	$\overline{PIOE}$	WS	9,10,11	35		ns
		$\overline{DMAE}$	WS	9,10,11	45		ns
		R/$\overline{W}$	WS	9,10,11	55		ns
Write mode control hold time	T_{WHC}	+ WS	$\overline{PIOE}$	9,10,11	15		ns
			$\overline{DMAE}$	9,10,11	10		ns
			R/$\overline{W}$	9,10,11	10		ns
Write strobe pulse width	T_{WP}			9,10,11	25		ns
Primary port data delay 4/	T_{PD1}	DO_A-$D7_A$/ DO_B-$D7_B$	$\overline{IV0}$-$\overline{IV7}$	9,10,11		90	ns
Primary port data delay from WS 5/	T_{PD2}	+ WS	$\overline{IV0}$-$\overline{IV7}$	9,10,11		90	ns
$\overline{MCLK}$ pulse width	t_W			9,10,11	30		ns
Data setup time	T_{SD1}	$\overline{IV0}$-$\overline{IV7}$	+ MCLK	9,10,11	35		ns
$\overline{ME}$ setup time	T_{SD2}	$\overline{ME}$	+ MCLK	9,10,11	40		ns
SC setup time	T_{SD3}	+ SC	+ MCLK	9,10,11	40		ns
WC setup time	T_{SD4}	+ WC	+ MCLK	9,10,11	40		ns
Data hold time	T_{HD1}	+ MCLK	$\overline{IV0}$-$\overline{IV7}$	9,10,11	5		ns
$\overline{ME}$ hold time	T_{HD2}	+ MCLK	$\overline{ME}$	9,10,11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $4.5\ V \leq V_{CC} \leq 5.5\ V$, $-55°C \leq T_C \leq +125°C$ FROM	TO	Group A subgroups	Limits Min	Limits Max	Unit
SC hold time	T_{HD3}	↓ MCLK	SC	9,10,11	0		ns
WC hold time	T_{HD4}	↓ MCLK	WC	9,10,11	0		ns
$\overline{IV}$ propagation delay 6/	T_{PD3}	$\overline{IV}$	DO_A-$D7_A$/ DO_B-$D7_B$	9,10,11		55	ns
Output enable	T_{OE}	$\overline{ME}$, SC, or WC	$\overline{IV0}$-$\overline{IV7}$	9,10,11		30	ns
Output enable	T_{OD}	$\overline{ME}$, SC, WC	$\overline{IV0}$-$\overline{IV7}$	9,10,11		35	ns

1/ Operating temperature ranges are guaranteed after terminal equilibrium has been reached.
2/ All voltages are measured with respect to ground terminal (see figure 4).
3/ Short only one output at a time.
4/ Measurement with write strobe set high and the control signals of the secondary port set for output data from the same register.
5/ Measurement with primary port data stable and control signals of the secondary port set for output data from the same register.
6/ Measured with MCLK = high and control signals of the primary port set for output data from the same register.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sample and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 or MIL-STD-883).

(1) Test condition A or B or C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 functional testing shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

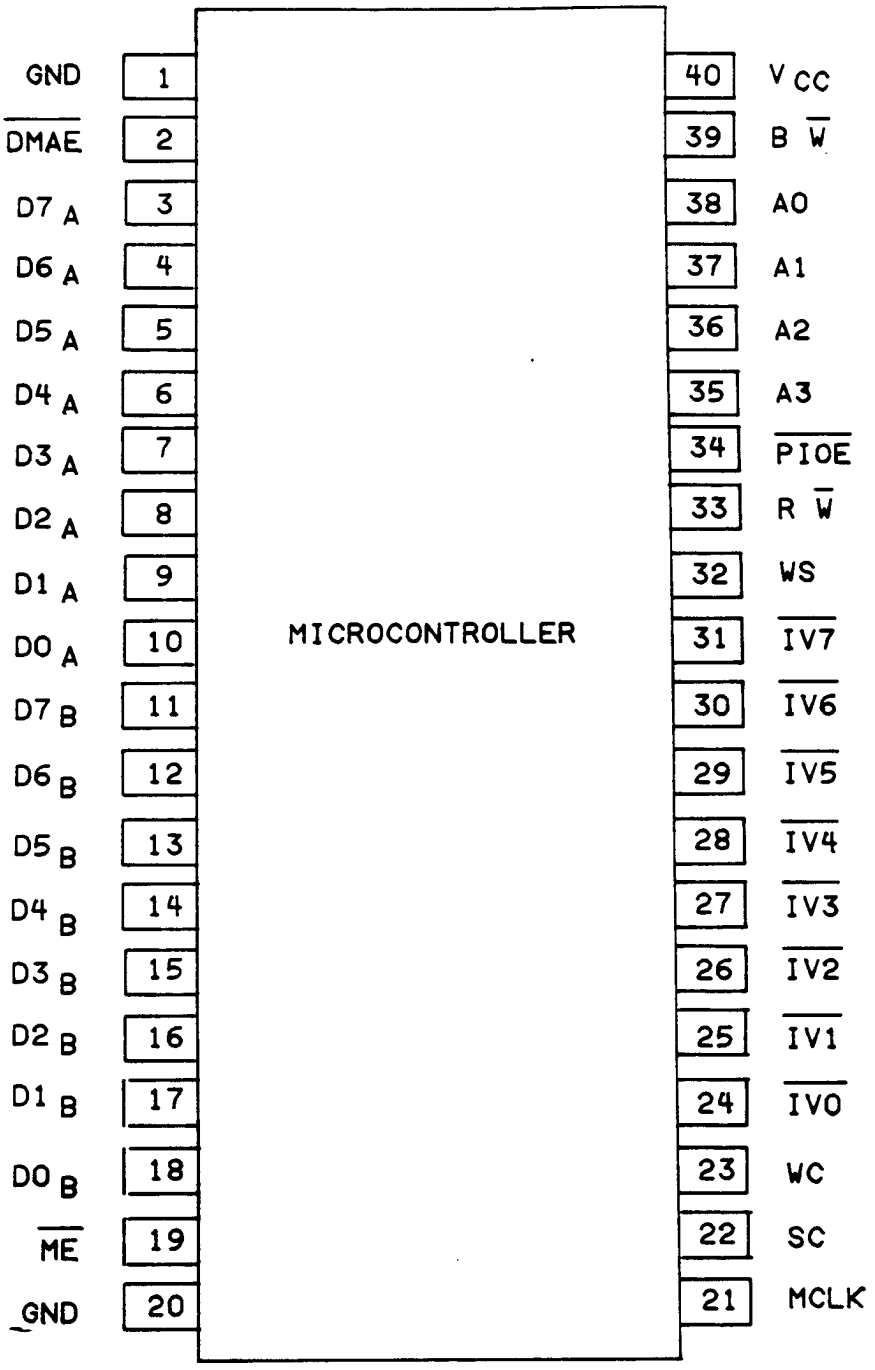
b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A or B or C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

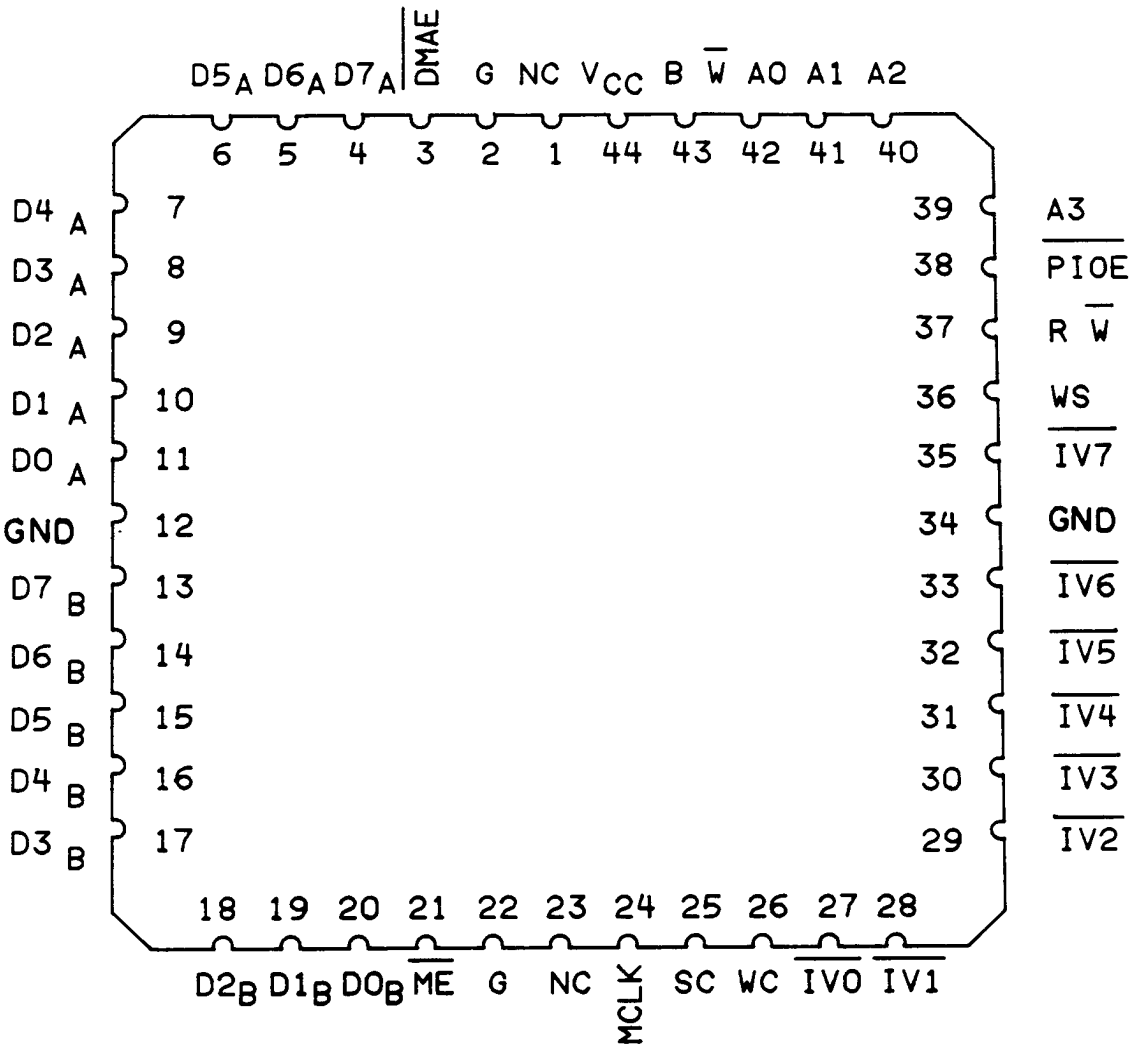
Case Q



TOP VIEW

FIGURE 1. Terminal connections.

Case U



TOP VIEW

FIGURE 1. Terminal connections - Continued.

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MODE CONTROL OF PRIMARY PORT

Mode	$\overline{PIOE}$	$\overline{DMAE}$
Disabled (output)	1	1
Programmed I/O	0	1
DMA	X	0

X = Don't care

PRIMARY PORT OPERATING IN PROGRAMMED I/O MODE

Mode	B/$\overline{W}$	A0	DO_A-$D7_A$ (Even addresses)	DO_B-$D7_B$ (Odd addresses)
Read	0 (Word)	X	Stored data	Stored data
Read	1 (Byte)	0	Stored data	HI-Z
Read	1 (Byte)	1	HI-Z	Stored data
Write	0 (Word)	X	Write	Write
Write	1 (Byte)	0	Write	No change
Write	1 (Byte)	1	No change	Write

X = Don't care

FIGURE 2. Truth table.

DMA OPERATION OF THE PRIMARY PORT

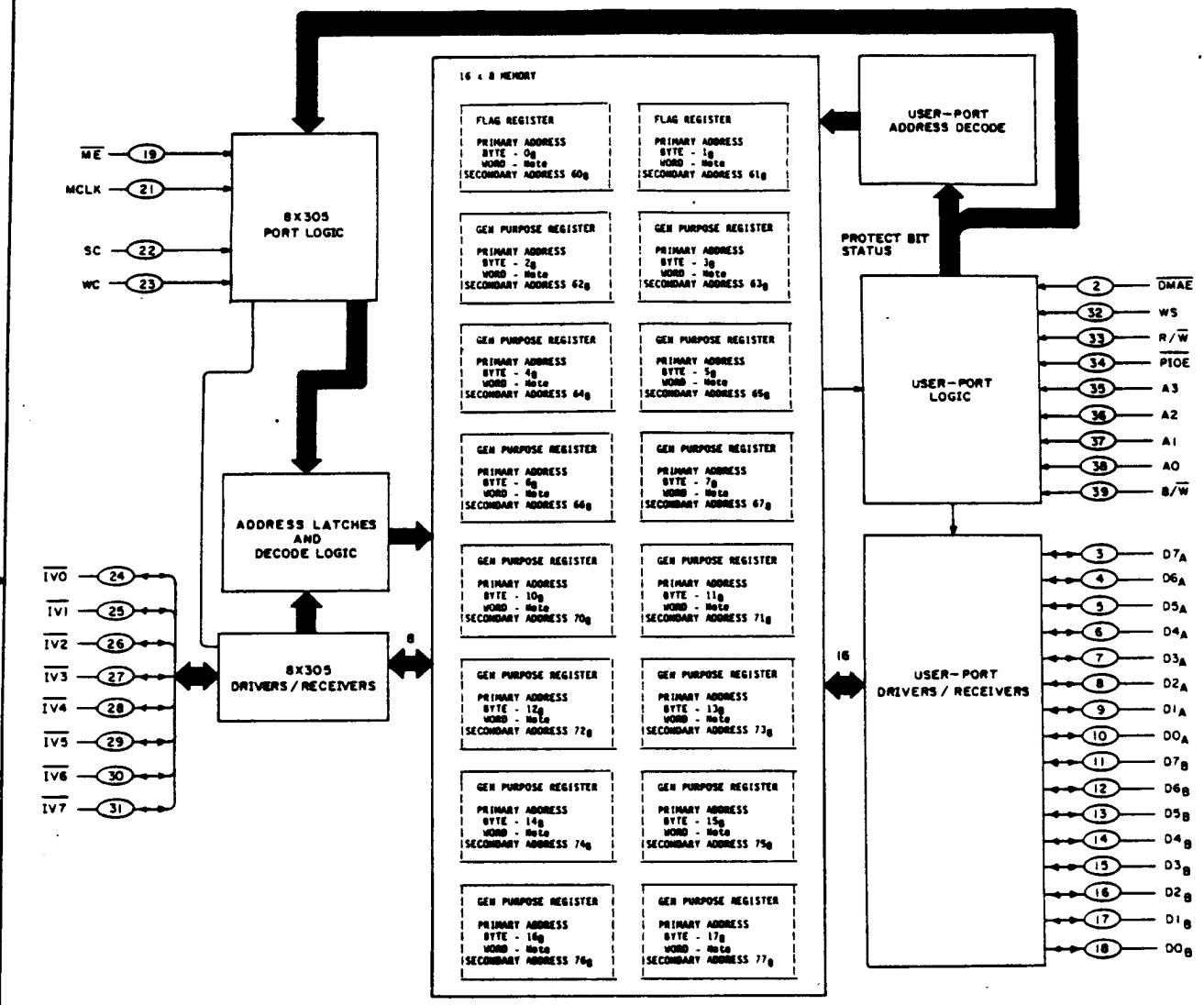
Mode	Byte/word	A0	DO_A-$D7_A$	DO_B-$D7_B$
Read	0 (Word)	0	Data stored in byte 14_8	Data stored in byte 15_8
Read	0 (Word)	1	Data stored in byte 16_8	Data stored in byte 17_8
Read	1 (Byte)	0	Data stored in byte 16_8	HI-Z
Read	1 (Byte)	1	HI-Z	Data stored in byte 17_8
Write	0 (Word)	0	Write to byte 14_8	Write to byte 15_8
Write	0 (Word)	1	Write to byte 16_8	Write to byte 17_8
Write	1 (Byte)	0	Write to byte 16_8	HI-Z
Write	1 (Byte)	1	HI-Z	Write to byte 17_8

FIGURE 2. Truth table - Continued.

$\overline{ME}$	SC[1]	WC[1]	MCLK	R/$\overline{W}$	Status latch	Function of secondary bus
L	L	L	X	X	Set	Output data from controller memory to processor
L	L	H	H	H	Set	Data from processor is input and written-into a previously-selected memory location of the controller (note 2).
L	L	H	H	L	Set	With the primary port in the write mode (R/$\overline{W}$ = 0), the secondary port is overridden and connot write to the same register addressed by the primary port; however, the register addressed by the primary port can be read and any other register can be read-from or written-into from the secondary port (note 2).
L	H	L	H	X	X	Data transmitted to the secondary port via the $\overline{IV}$ bus is interpreted as an address; if address is within range of 60_8-77_8 the memory status latch is subsequently set.
L	L	H	L	X	X	Inactive
L	H	L	L	X	X	Inactive
L	L	X	X	X	Not set	Inactive
H	X	X	X	X	X	Inactive

NOTES:
1. The SC and WC lines should never both be high at the same time.
2. During read or write operations, the same register can be simultaneously addressed from either port. For any write operation by both ports on the same register, the primary port has priority; other than this, the device does not indicate error conditions or resolve conflicts.
3. X = Don't care.

FIGURE 2. Truth table - Continued.



NOTE: In the work mode, the registers are addressed in specific pairs byte 0/byte 1, byte 2/byte 3, byte 4/byte 5 . . . byte 14/byte 15 and byte 16/byte 17.

FIGURE 3. Functional block diagram.

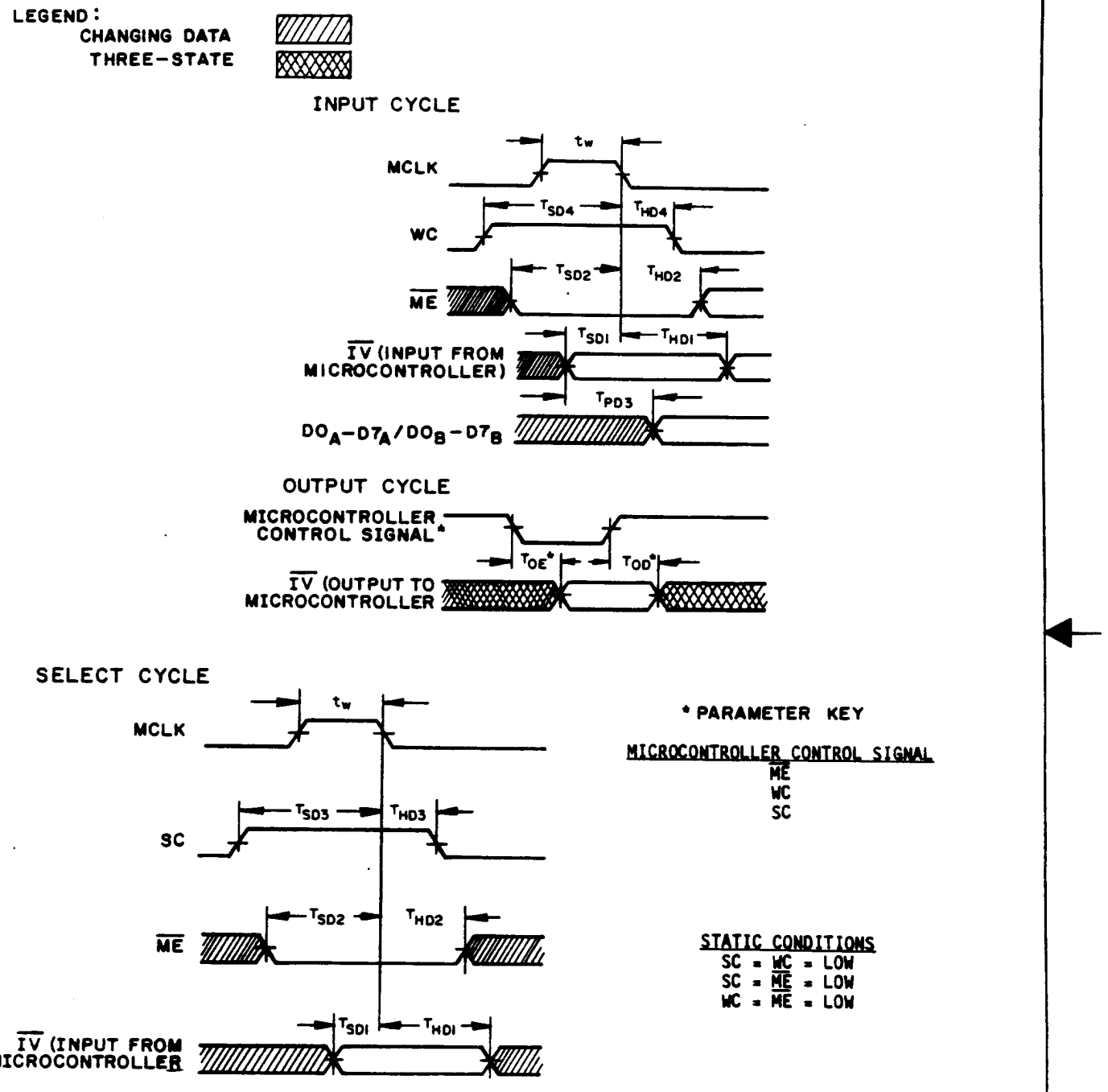


FIGURE 4. Timing waveforms and test circuit.

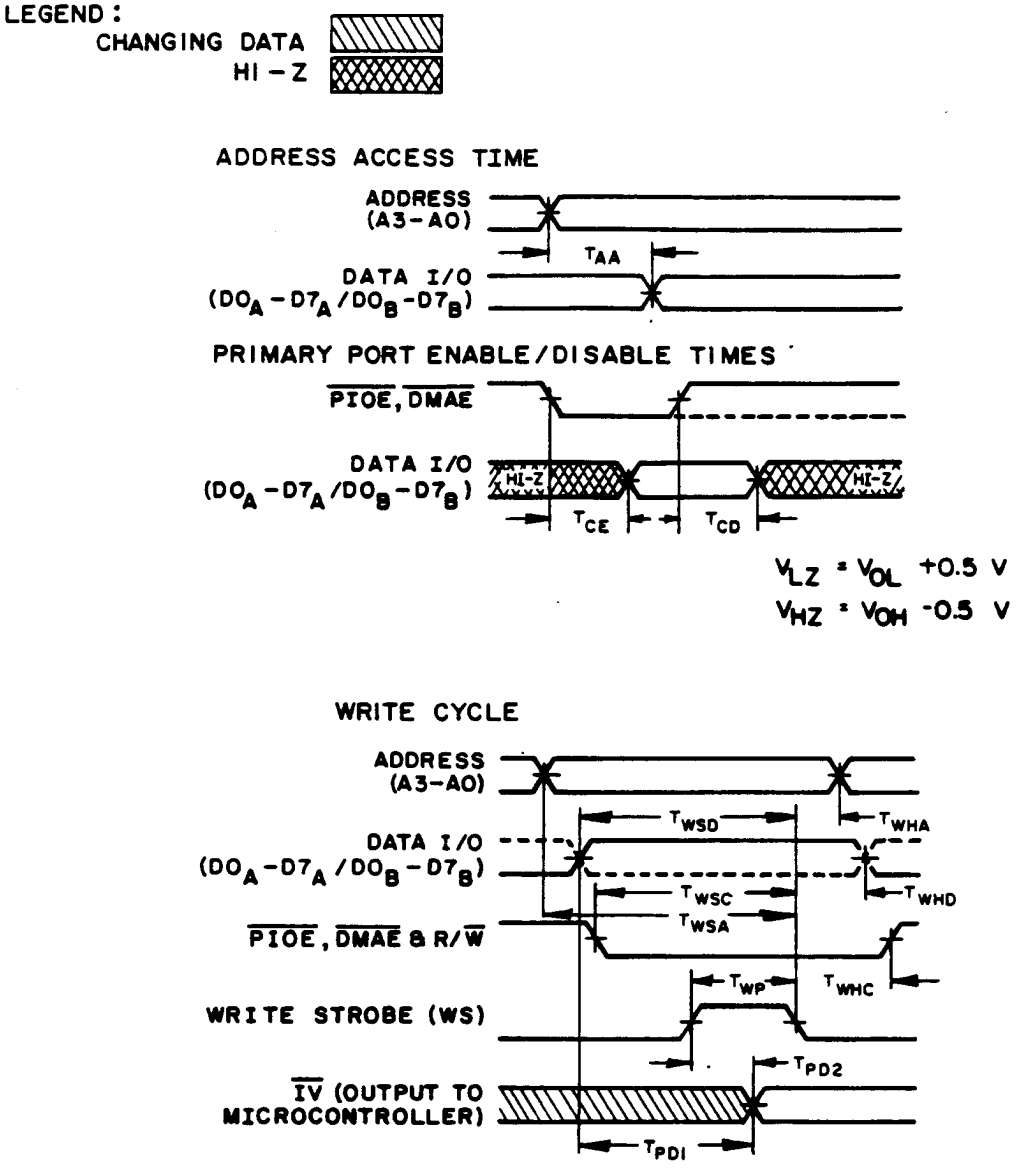
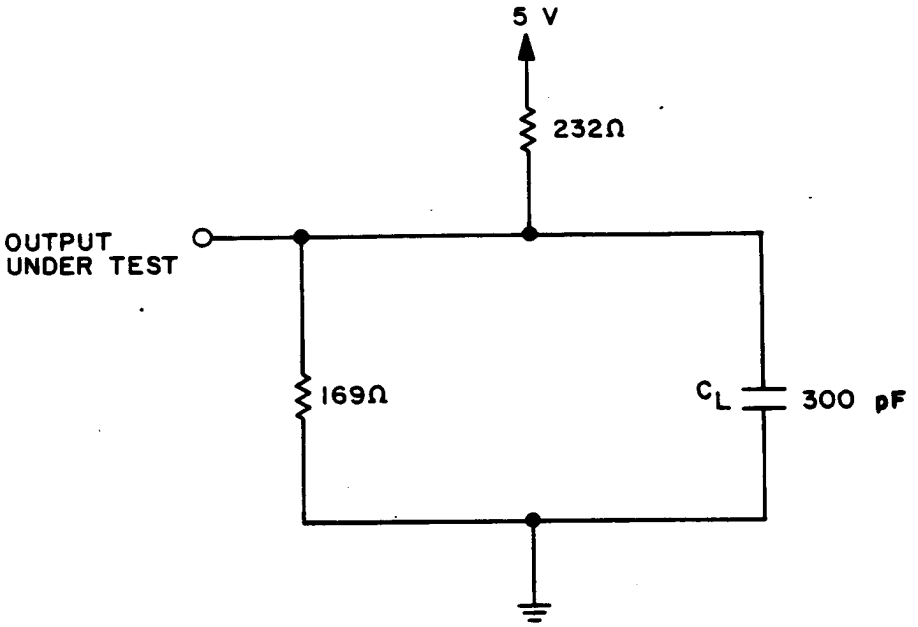


FIGURE 4. Timing waveforms and test circuit - Continued.

Test circuit



NOTE:
C_L INCLUDES JIG AND PROBE CAPACITANCE

FIGURE 4. Timing waveforms and test circuit - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Terminal and pin definitions.

Identifier	Function
GND	Circuit ground.
$\overline{DMAE}$	Enables primary port to facilitate DMA transfers; does not affect secondary port.
DO_A-$D7_A$ DO_B-$D7_B$	Sixteen 3-state lines used for data transfer to-and-from the primary data port; most significant bit is DO_B and least significant bit is $D7_A$.
$\overline{ME}$	Enables secondary port when active low ($\overline{ME}$).
MCLK	When MCLK is high, and device is enables ($\overline{ME}$ = Low), a register location may be either selected or written-into under control of SC and WC.
SC	With SC high, WC low, MCLK high and $\overline{ME}$ low, data on IV0 through IV7 is interpreted as an address. If any one of the 16 register addresses (60_8-77_8) matches that on the I/O (IV) bus, that particular register is selected and remains selected until another address on the same bank (i.e., $\overline{ME}$ = Low) is output on the I/O bus - at which time, the old register is deselected and a new register may or may not be selected.
WC	With WC high, SC low, MCLK high and $\overline{ME}$ low, the selected register stores contents of $\overline{IV0}$-$\overline{IV7}$ as data.
IV0-IV7	Eight 3-state lines used to transfer data or I/O address to-and-from the secondary data port; most significant bit is $\overline{IV0}$ and least significant bit is $\overline{IV7}$.
WS	When active high, data appearing at the primary port (DO_A-$D7_A$/DO_B-$D7_B$) is stored in the register array if the primary port is in the "write" mode.
R/$\overline{W}$	When this signal is high, primary port is in "read" mode; when signal is low, primary port is in "write" mode.
$\overline{PIOE}$	When active low, primary port operates in programmed input/output mode with register to be read-from or write-into selected by A0-A3.
A0-A3	Selects register or register-pair that primary port is to read-from or write-into. Most significant bit is A3; least significant bit is A0.
B/$\overline{W}$	When signal is high, the primary port operates in the byte (8-bit) mode; when signal is low, the primary port operates in the word (16-bit) mode.
V_{CC}	+5 volts.

All barred symbols (DMAE, etc.) denote signals that are asserted (or active) when low (logical 0), signal that are not barred are asserted in the high state (logical 1).

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8550301UX	18324	8X320/BUX
5962-85503010X	18324	8X320/BQC

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834