REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Revise table I limits. Revise figure 3 waveforms. Make editorial changes.	16 Mar 1987	M. A. Frye

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OF PAGES	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16															

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
18 June 1986

AMSC N/A

PREPARED BY: Greg A. Pitz
CHECKED BY: D. A. DiCenzo
APPROVED BY: M. A. Frye

SIZE: A
CODE IDENT. NO.: 14933
REV: A

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, CMOS PROGRAMMABLE INTERRUPT CONTROLLER MONOLITHIC SILICON

DWG NO. 5962-85016

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5962-E227

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-85016	01	Y	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit
01	82C59A-5	5 MHz	CMOS programmable interrupt controller
02	82C59A	8 MHz	CMOS programmable interrupt controller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Y	D-10 (28-lead, 1/2" x 1-3/8") dual-in-line package
3	C-4 (28-terminal, .450" x .450") square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage (referenced to GND)	+8.0 V dc 1/
Input, output, or I/O voltage applied	GND -0.5 V dc to V_{CC} +0.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1 W
Thermal resistance, junction-to-case (θ_{JC}): 2/	
Case Y	20°C/W
Case 3	25°C/W
Junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+275°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range	+4.5 V dc to +5.5 V dc 1/
Frequency of operation:	
Device type 01	5 MHz
Device type 02	8 MHz
Case operating temperature range	-55°C ≤ T_C ≤+125°C
Data float after $\overline{RD}/\overline{INTA}$ (t_{RHDZ}) reference number 14	3/
Device type 01	10 ns minimum, 100 ns maximum
Device type 02	10 ns minimum, 85 ns maximum

1/ All voltages referenced to V_{SS}.
2/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.
3/ The reference number refers to the parameter being measured on figure 3. The parameter being measured uses test condition 2 on figure 4.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified		Device type	Ref no. 1/	Group A subgroups	Limits Min	Limits Max	Unit
High level input voltage	V_{IH}	V_{CC} = 5.5 V		01,02		1, 2, 3	2.2		V
Low level input voltage	V_{IL}	V_{CC} = 4.5 V		01,02		1, 2, 3		0.8	V
High level output voltage 2/	V_{OH1}	I_{OH} = -2.5 mA V_{CC} = 4.5 V		01,02		1, 2, 3	3.0		V
	V_{OH2}	I_{OH} = -100 µA V_{CC} = 4.5 V		01,02		1, 2, 3	V_{CC}-0.4		V
Low level output voltage 2/	V_{OL}	I_{OL} = +2.5 mA V_{CC} = 4.5 V		01,02		1, 2, 3		0.4	V
Input leakage current	I_I	V_{CC} = 5.5 V	V_{IN} = 0 V	01,02		1, 2, 3	-1.0		µA
			V_{IN} = V_{CC}					1.0	
I/O leakage current	I_O	V_{CC} = 5.5 V	V_{IN} = 0 V	01,02		1, 2, 3	-10		µA
			V_{IN} = V_{CC}					10	
Standby power supply current	I_{CCSB}	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND 3/ outputs open		01,02		1, 2, 3		10	µA
IR input load current	I_{LIR}	V_{IN} = 0 V, V_{CC} = 5.5 V		01,02		1, 2, 3		-500	µA
		V_{IN} = V_{CC}, V_{CC} = 5.5 V		01,02		1, 2, 3		10	µA
Functional tests	FT	See 4.3.1d 5/	V_{CC} = 5.5 V and 4.5 V	01,02		7, 8			
Input capacitance	C_{IN}	FREQ = 1 MHz T_C = +25°C See 4.3.1c All measurements referenced to device ground.		Case Y		4		15	pF
				Case 3		4		7	
Output capacitance	C_O			Case Y		4		15	pF
				Case 3		4		7	
I/O capacitance	$C_{I/O}$			Case Y		4		15	pF
				Case 3		4		7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified	Device type	Ref no. 1/	Group A subgroups	Limits Min	Limits Max	Unit
A0/$\overline{CS}$ Setup to $\overline{RD}/\overline{INTA}$	t_{AHRL}	V_{CC} = 4.5 V and 5.5 V 5/	01,02	1	9,10,11	10		ns
A0/$\overline{CS}$ Hold after $\overline{RD}/\overline{INTA}$	t_{RHAX}		01,02	2	9,10,11	5		ns
$\overline{RD}/\overline{INTA}$ Pulse Width	t_{RLRH}		01	3	9,10,11	235		ns
			02	3	9,10,11	160		ns
A0/$\overline{CS}$ Setup to $\overline{WR}$	t_{AHWL}		01,02	4	9,10,11	0		ns
A0/$\overline{CS}$ Hold after $\overline{WR}$	t_{WHAX}		01,02	5	9,10,11	5		ns
$\overline{WR}$ Pulse Width	t_{WLWH}		01	6	9,10,11	165		ns
			02	6	9,10,11	95		ns
Data Setup to $\overline{WR}$	t_{DVWH}		01	7	9,10,11	240		ns
			02	7	9,10,11	160		ns
Data Hold after $\overline{WR}$	t_{WHDX}		01,02	8	9,10,11	5		ns
Interrupt Request Width (Lo) 6/	t_{JLJH}		01,02	9	9,10,11	100		ns
Cascade Setup to second or third $\overline{INTA}$ (slave only)	t_{CVIAL}		01	10	9,10,11	55		ns
			02	10	9,10,11	40		ns
End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	t_{RHRL}		01,02	11	9,10,11	160		ns
End of $\overline{WR}$ to next $\overline{WR}$	t_{WHWL}		01,02	12	9,10,11	190		ns
End of Command to next Command (not same command type) 7/ End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	t_{CHCL}		01	21	9,10,11	500		ns
			02	21	9,10,11	400		ns
Data Valid from $\overline{RD}/\overline{INTA}$ 4/	t_{RLDV}		01	13	9,10,11		160	ns
			02	13	9,10,11		120	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Ref no. 1/	Group A subgroups	Limits Min	Limits Max	Unit
Interrupt Output Delay	t_{JHIH}	V_{CC} = 4.5 V and 5.5 V 4/ 5/	01	15	9,10,11		350	ns
			02	15	9,10,11		300	ns
Cascade Valid from first $\overline{INTA}$ (Master only)	t_{IALCV}		01	16	9,10,11		565	ns
			02	16	9,10,11		360	ns
Enable Active from $\overline{RD}$ or $\overline{INTA}$	t_{RLEL}		01	17	9,10,11		125	ns
			02	17	9,10,11		100	ns
Enable Inactive from $\overline{RD}$ or $\overline{INTA}$	t_{RHEH}		01	18	9,10,11		60	ns
			02	18	9,10,11		50	ns
Data Valid from Stable Address	t_{AHDV}		01	20	9,10,11		210	ns
			02	20	9,10,11		200	ns
Cascade Valid to Valid Data	t_{CVDV}		01	19	9,10,11		300	ns
			02	19	9,10,11		200	ns

1/ The reference number refers to the parameter being measured on figure 3.
2/ Interchanging of force and sense conditions are permitted.
3/ For IR0-IR7 pins, $V_{IN} = V_{CC}$ or open.
4/ The parameter being measured uses test condition 1 on figure 4.
5/ Tested as follows: f = 1 MHz, V_{IH} = 2.6 V, V_{IL} = 0.4 V, $V_{OH} \ge 1.5$ V, $V_{OL} \le 1.5$ V and C_L = 50 pF unless otherwise noted. Circuits and waveforms on figure 4.
6/ This is the low time required to clear the input latch in the edge triggered mode.
7/ Worst case timing for t_{CHCL} in an actual microprocessor system is typically much greater than the limits shown.

CASE Y

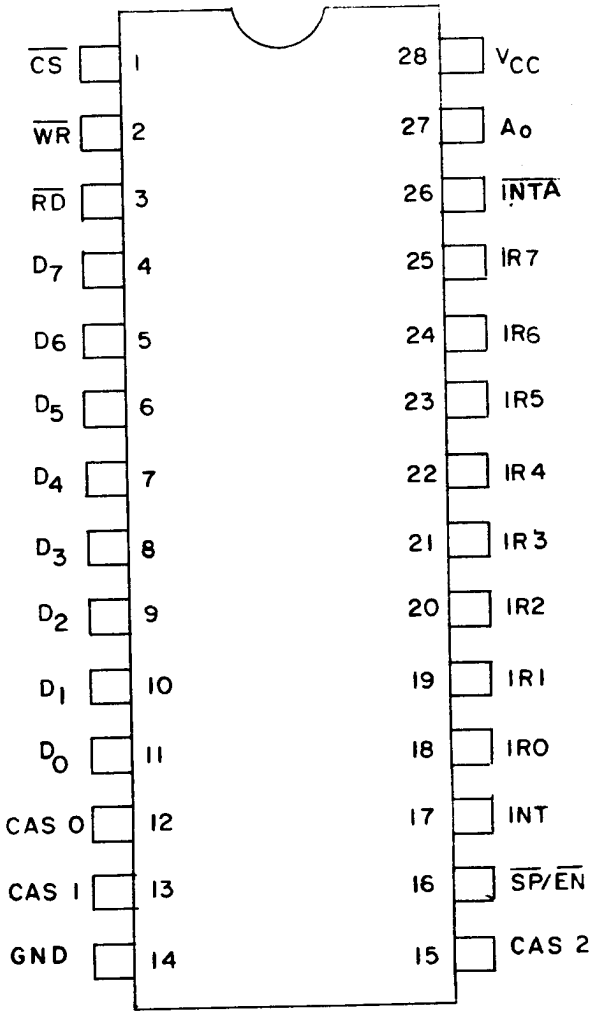

FIGURE 1. Terminal connections.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-85016
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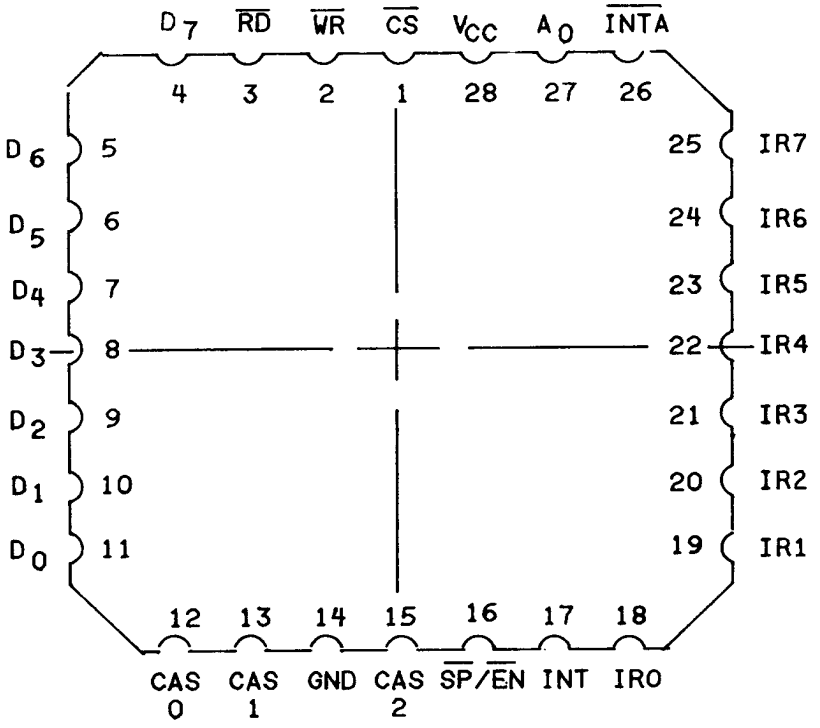
CASE 3



TOP VIEW

FIGURE 1. Terminal connections - Continued.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-85016
		REV	PAGE 8

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FEB 86

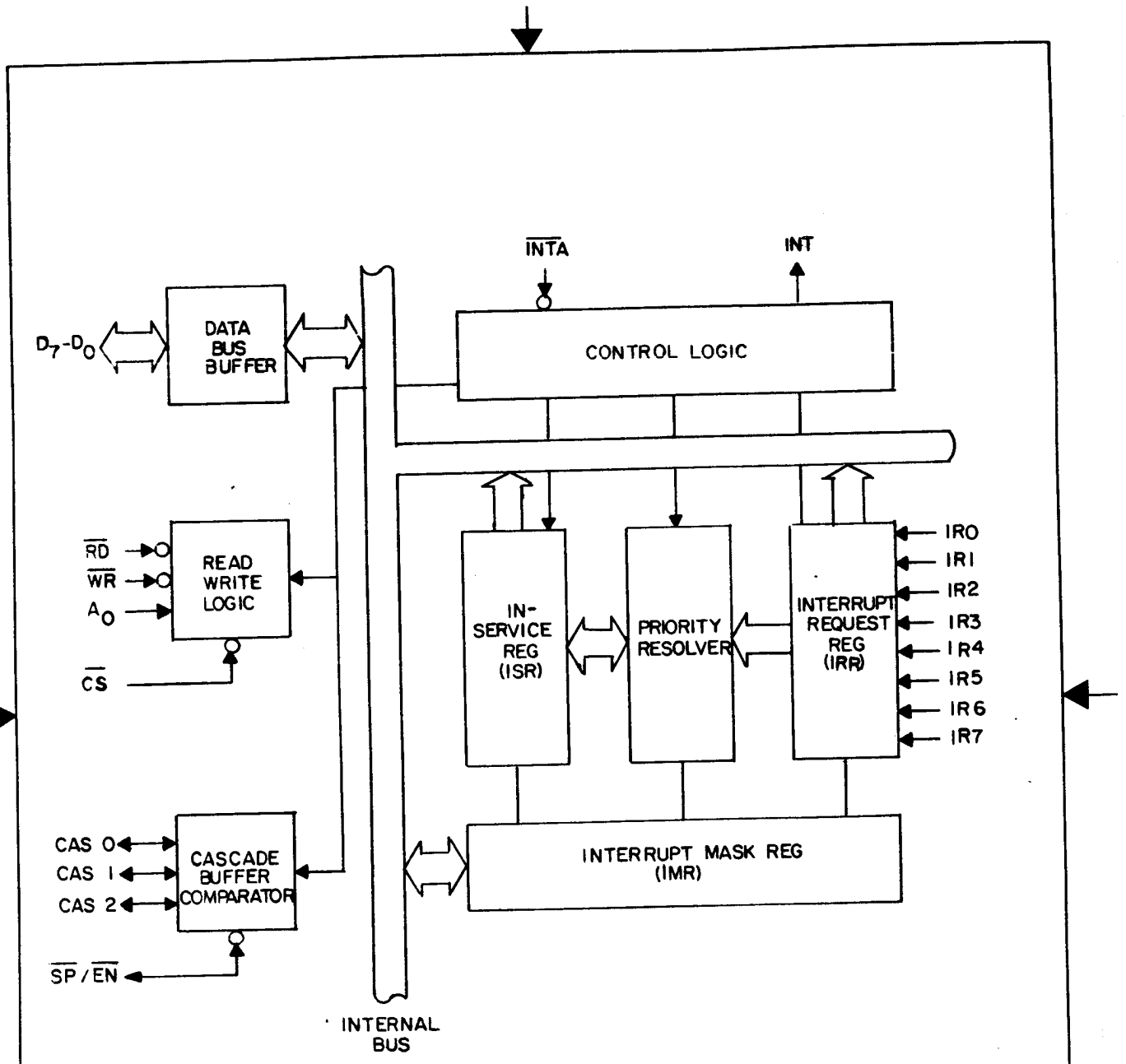


FIGURE 2. Functional block diagram.

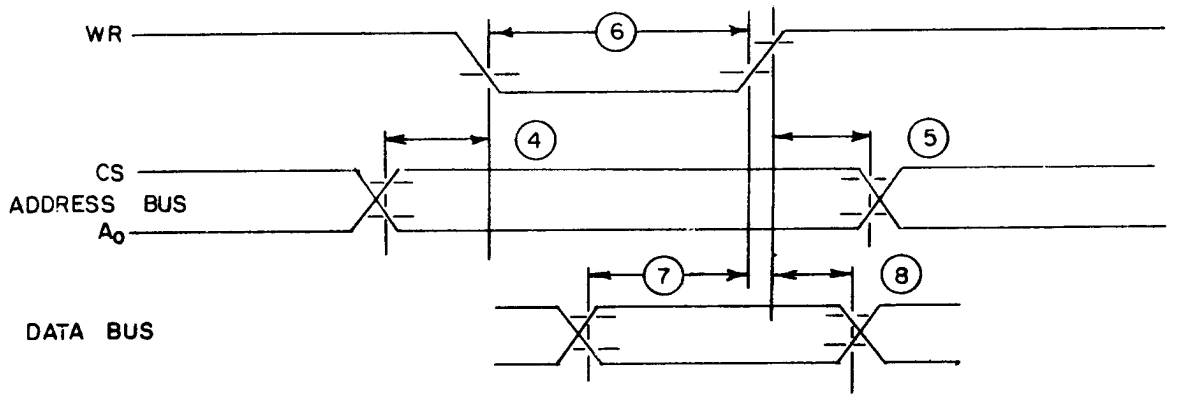


FIGURE 3. Waveforms - WRITE cycle.

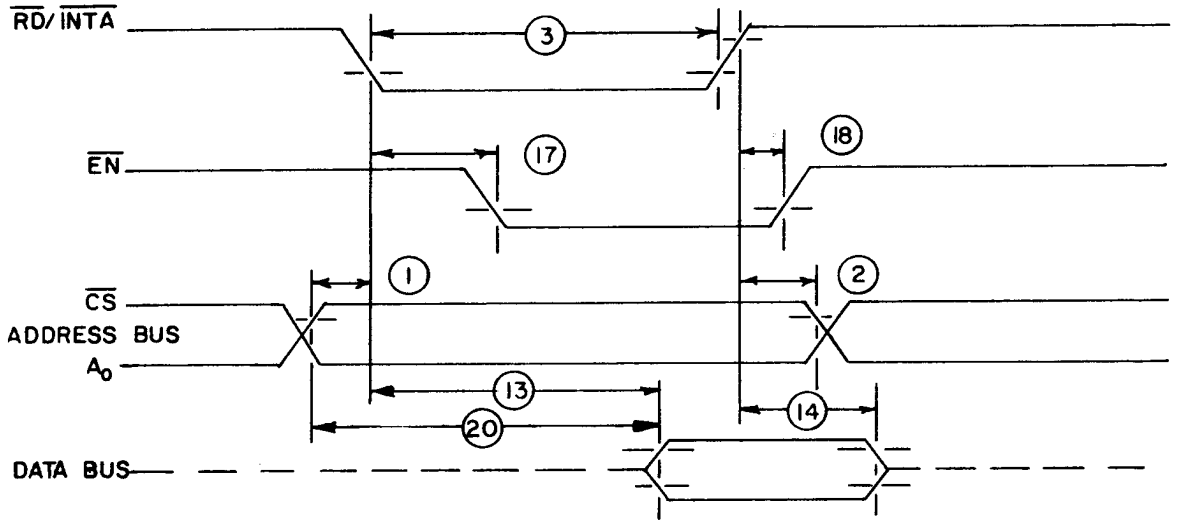


FIGURE 3. Waveforms - $\overline{READ}/\overline{INTA}$ cycle

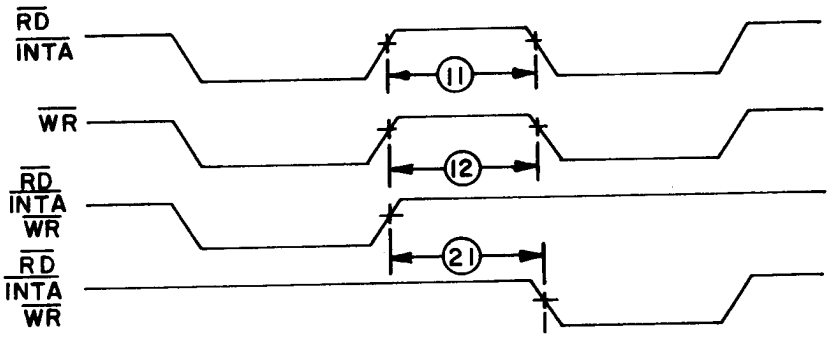
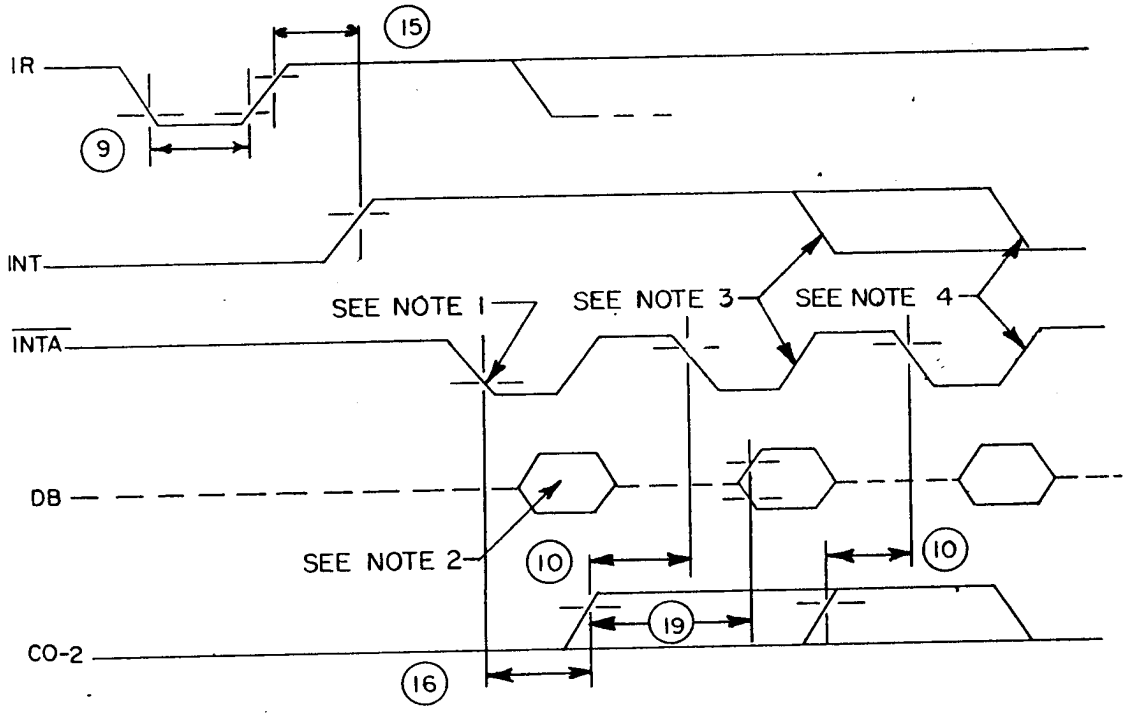
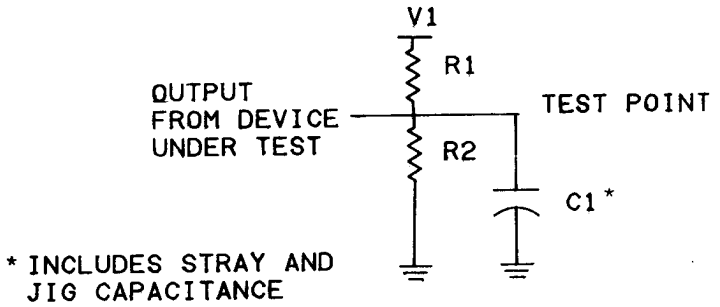


FIGURE 3. Waveforms - Other timing.



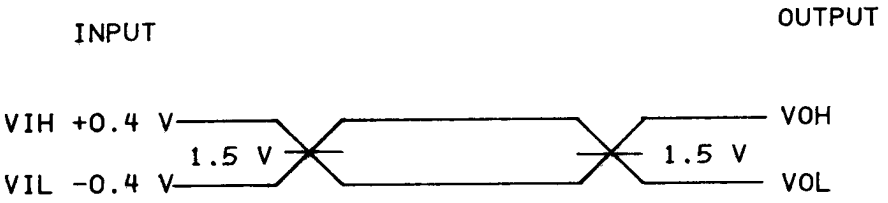
NOTES:
1. Interrupt request (IR) must remain HIGH until leading edge of first $\overline{\text{INTA}}$.
2. During first $\overline{\text{INTA}}$, the DATA BUS is not active in 80C86/80C88 mode.
3. 80C86/80C88 mode.
4. 8080/8085 mode.

FIGURE 3. Waveforms - $\overline{\text{INTA}}$ sequence.



TEST CONDITION	V1	R1	R2	C1 Min
1	1.7 V	523Ω	OPEN	100 pF
2	V_{CC}	1.8 kΩ	1.8 kΩ	30 pF

TEST CONDITION DEFINITION TABLE



AC Testing: All input signals must switch between VIL -0.4 V and VIH +0.4 V. T_R and T_F are driven at 1.0 ns/V.

FIGURE 4. AC test circuits and waveforms.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_O, and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 functional tests shall include verification of programming set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8,9, 10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8 (+125°C only), 10
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Symbols, definitions and functional descriptions. The symbols, definitions, and functional descriptions for these devices shall be as follows:

Symbol	Name and function
V_{CC}	POWER SUPPLY +5 V Supply pin. A 0.1 µF capacitor between V_{CC} and GND is recommended for decoupling.
GND	GROUND
$\overline{CS}$	CHIP SELECT: A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the device. INTA functions are independent of $\overline{CS}$.
$\overline{WR}$	WRITE: A low on this pin when $\overline{CS}$ is low enables the device to accept command words from the CPU.
$\overline{RD}$	READ: A low on this pin when $\overline{CS}$ is low enables the device to release status onto the data bus for the CPU.
D_7-D_0	BIDIRECTIONAL DATA BUS: Control status and interrupt-vector information is transferred via this bus.
CAS0-CAS2	CASCADE LINES: The CAS lines form a private device bus to control a multiple device structure. These pins are outputs for a master device and inputs for a slave device.
$\overline{SP}/\overline{EN}$	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the buffered mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master (SP=1) or slave (SP=0).
INT	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR0-IR7	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE: This pin is used to enable device interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the device to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A_0 address line (A_1 for 80C86/88).

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962 - 8501601YX	34371	MD82C59A-5/B	- - -
5962 - 85016013X	34371	MR82C59A-5/B	- - -
5962 - 8501602YX	34371	MD82C59A/B	- - -
5962 - 85016023X	34371	MR82C59A/B	- - -

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P. O. Box 883 Melbourne, Florida 32901