Ordering number: EN 4484A

CMOS LSI

SANYO No. 4484A

LC3564RM/RMF-10LV/12LV/15LV

64 K (8192 words × 8 bits) SRAM

Overview

The LC3564RM/RMF are 8192-word × 8-bit, asynchronous, silicon gate, low-voltage CMOS SRAM LSIs. They operate from a 2.0 to 3.6 V supply, making them ideal for hand-held, battery-operated equipment.

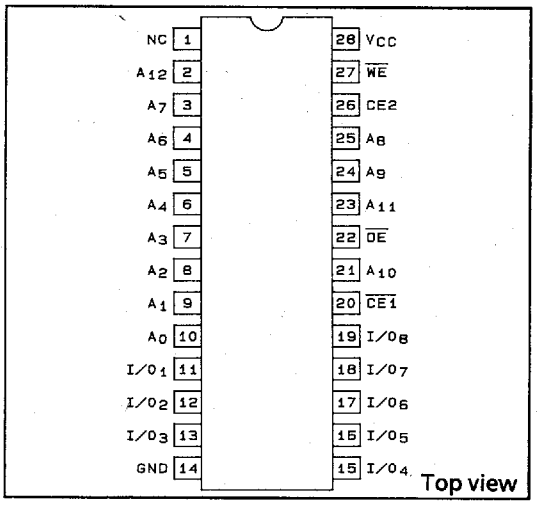
They are fully CMOS devices employing 2-layer Al wiring to realize high-speed access, low operating current consumption and very low standby current. They incorporate control signal inputs; $\overline{OE}$ for high-speed memory access, and 2 chip enables $\overline{CE1}$ and CE2 for power-down and device selection.

They are ideal for systems requiring high speed, low power and battery backup or for easy memory expansion. The very low standby current means that backup can also be achieved using a capacitor.

Features

- 2.0 to 3.6 V supply voltage range
  - 2.7 to 3.6 V (3 V operation)
  - 2.0 to 2.4 V (2 V operation)
- High-speed access time
  - 3 V operation
    - 100 ns max. (LC3564RM, RMF-10LV)
    - 120 ns max. (LC3564RM, RMF-12LV)
    - 150 ns max. (LC3564RM, RMF-15LV)
  - 2 V operation
    - 200 ns max. (LC3564RM, RMF-10LV)
    - 250 ns max. (LC3564RM, RMF-12LV)
    - 300 ns max. (LC3564RM, RMF-15LV)
- Very-low standby current
  - 3 V operation
    - 1.0 μA ($T_a \leq 70$ °C)
    - 3.0 μA ($T_a \leq 85$ °C)
  - 2 V operation
    - 0.85 μA ($T_a \leq 70$ °C)
    - 2.5 μA ($T_a \leq 85$ °C)
- –40 to +85 °C operating temperature range
- 2.0 to 3.6 V data retention supply voltage
- V_{CC} – 0.4 V/0.4 V input/output levels
- Package
  - SOP 28-pin plastic package (450mil): LC3564RM series)
  - MFP 28-pin plastic package (375mil): LC3564RMF series)
- 3 control inputs ($\overline{OE}$, $\overline{CE1}$, CE2)
- Common-pin input/outputs, 3-state output
- Clock not needed (fully-static RAM)

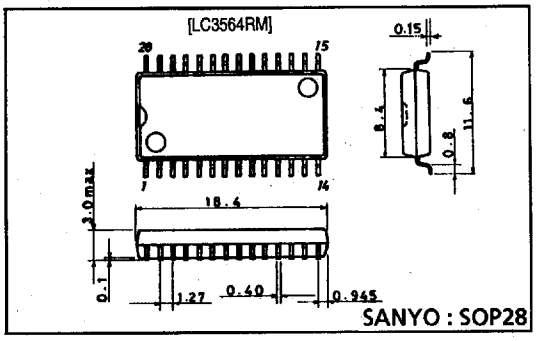
Pin Assignment



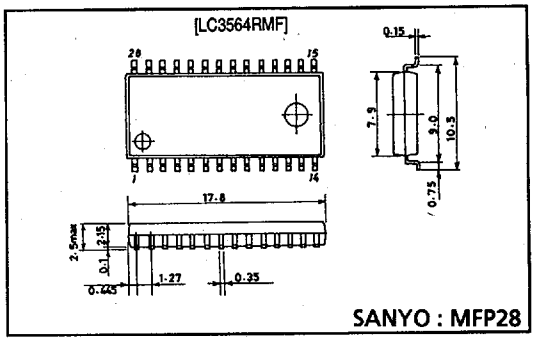
Package Dimensions

Unit: mm

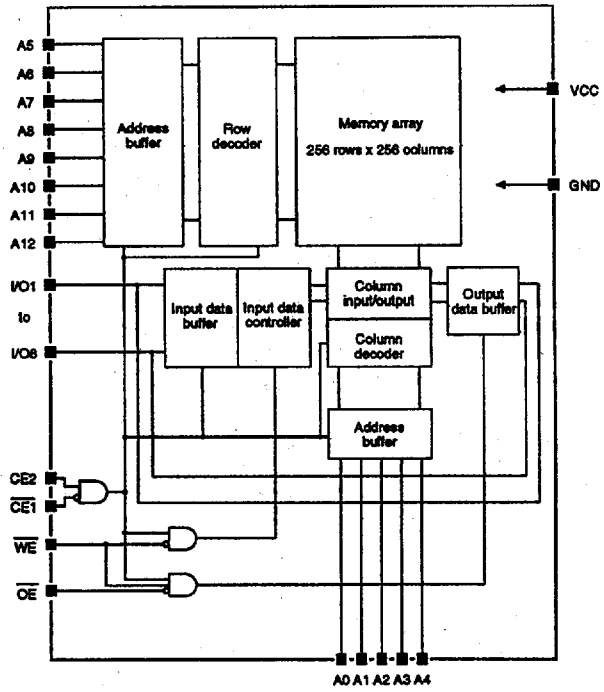
3158-SOP28



3091-MFP28



Block Diagram



Pin Functions

Number	Name	Function
1	NC	No connection
2 to 10, 21, 23 to 25	A0 to A12	Address inputs
27	$\overline{WE}$	Read/write control input
22	$\overline{OE}$	Output enable input
20, 26	$\overline{CE1}$, CE2	Chip enable inputs

Number	Name	Function
11 to 13, 15 to 19	I/O1 to I/O8	Data input/outputs
28, 14	V_{CC}, GND	Supply and ground pins

Truth Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	H	L	H	Data output	I_{CCA}
Write cycle	L	H	X	L	Data input	I_{CCA}
Output disable	L	H	H	H	High impedance	I_{CCA}
No selection	H	X	X	X	High impedance	I_{CCS}
	X	L	X	X	High impedance	I_{CCS}

Note
X = H or L

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		4.6	V
Input voltage range	V_{IN}		–0.3 to V_{CC} + 0.3	V
Input/output voltage range	$V_{I/O}$		–0.3 to V_{CC} + 0.3	V
Operating temperature range	T_{opr}		–40 to +85	°C
Storage temperature range	T_{stg}		–55 to +125	°C

Note
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended operating conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Input/Output Capacitance

T_a = 25 °C, f = 1 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min.	typ.	max.	
Input/output pin capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	–	6	10	pF
Input pin capacitance	C_I	V_{IN} = 0 V	–	6	10	pF

Note
Measured samples only.

3 V Operation

DC Recommended Operating Ranges

T_a = –40 to +85 °C, V_{CC} = 2.7 to 3.6 V

Parameter	Symbol	Ratings			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	V_{CC} – 0.4	–	V_{CC} + 0.3	V
	V_{IL}	–0.3*	–	+0.4	V

* When pulsewidth is less than 30 ns, the minimum value is –2.0 V.

DC Electrical Characteristics

T_a = –40 to +85 °C, V_{CC} = 2.7 to 3.6 V

Parameter		Symbol	Conditions		Ratings			Unit
					min.	typ.*	max.	
Input leakage current		I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0	–	+1.0	µA
I/O leakage current		I_{LO}	$V_{\overline{CE1}}$ = V_{IH} or V_{CE2} = V_{IL} or $V_{\overline{OE}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CC}		–1.0	–	+1.0	µA
Output high level voltage		V_{OH}	I_{OH} = –2.0 mA		V_{CC} – 0.4	–	–	V
Output low level voltage		V_{OL}	I_{OL} = 2.0 mA		–	–	0.4	V
Operating supply current	V_{CC} – 0.2 V/0.2 V input	I_{CCA1}	$V_{\overline{CE1}}$ ≤ 0.2 V, V_{CE2} ≥ V_{CC} – 0.2 V, $I_{I/O}$ = 0 mA, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V	T_a ≤ 70 °C	–	0.01	1.0	µA
				T_a ≤ 85 °C	–	–	3.0	µA
	V_{CC} – 0.4 V/0.4 V input	I_{CCA2}	$V_{\overline{CE1}}$ = V_{IL}, V_{CE2} = V_{IH}, $I_{I/O}$ = 0 mA, V_{IN} = V_{IH} or V_{IL}		–	–	4	mA
		I_{CCA3}	$V_{\overline{CE1}}$ = V_{IL}, V_{CE2} = V_{IH}, $I_{I/O}$ = 0 mA, duty = 100%	min. cycle	–	–	25	mA
				200 ns cycle	–	–	15	mA
				1 µs cycle	–	–	10	mA
Standby supply current	V_{CC} – 0.2 V/0.2 V input	I_{CCS1}	V_{CE2} ≤ 0.2 V or {$V_{\overline{CE1}}$ ≥ V_{CC} – 0.2 V, V_{CE2} ≥ V_{CC} – 0.2 V}	T_a ≤ 70 °C	–	0.01	1.0	µA
				T_a ≤ 85 °C	–	–	3.0	µA
	V_{CC} – 0.4 V/0.4 V input	I_{CCS2}	V_{CE2} = V_{IL} or $V_{\overline{CE1}}$ = V_{IH}, V_{IN} = 0 V to V_{CC}		–	–	1	mA

* V_{CC} = 3.0 V, T_a = 25 °C

AC Electrical Characteristics

T_a = −40 to +85 °C, V_{CC} = 2.7 to 3.6 V

AC test conditions

Input pulse voltage level: V_{IH} = V_{CC} − 0.4 V, V_{IL} = 0.4 V

Input rise and fall times: 5 ns

Input/output timing level: $V_{CC}/2$

Output load: 30 pF (including jig capacitance)

Read Cycle

Parameter	Symbol	LC3564RM/RMF						Unit
		10LV		12LV		15LV		
		min.	max.	min.	max.	min.	max.	
Read cycle time	t_{RC}	100	–	120	–	150	–	ns
Address access time	t_{AA}	–	100	–	120	–	150	ns
$\overline{CE1}$ access time	t_{CA1}	–	100	–	120	–	150	ns
CE2 access time	t_{CA2}	–	100	–	120	–	150	ns
$\overline{OE}$ access time	t_{OA}	–	50	–	60	–	75	ns
Output hold time	t_{OH}	10	–	10	–	10	–	ns
$\overline{CE1}$ output enable time	t_{COE1}	10	–	10	–	10	–	ns
CE2 output enable time	t_{COE2}	10	–	10	–	10	–	ns
$\overline{OE}$ output enable time	t_{OOE}	5	–	5	–	5	–	ns
$\overline{CE1}$ output disable time	t_{COD1}	–	35	–	40	–	50	ns
CE2 output disable time	t_{COD2}	–	35	–	40	–	50	ns
$\overline{OE}$ output disable time	t_{OOD}	–	25	–	30	–	40	ns

Write Cycle

Parameter	Symbol	LC3564RM/RMF						Unit
		10LV		12LV		15LV		
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{WC}	100	–	120	–	150	–	ns
Address setup time	t_{AS}	0	–	0	–	0	–	ns
Write pulsewidth	t_{WP}	60	–	70	–	80	–	ns
$\overline{CE1}$ setup time	t_{CW1}	70	–	80	–	90	–	ns
CE2 setup time	t_{CW2}	70	–	80	–	90	–	ns
Write recovery time	t_{WR}	0	–	0	–	0	–	ns
$\overline{CE1}$ write recovery time	t_{WR1}	0	–	0	–	0	–	ns
CE2 write recovery time	t_{WR2}	0	–	0	–	0	–	ns
Data setup time	t_{DS}	50	–	55	–	60	–	ns
Data hold time	t_{DH}	0	–	0	–	0	–	ns
$\overline{CE1}$ data hold time	t_{DH1}	0	–	0	–	0	–	ns
CE2 data hold time	t_{DH2}	0	–	0	–	0	–	ns
$\overline{WE}$ output enable time	t_{WOE}	5	–	5	–	5	–	ns
$\overline{WE}$ output disable time	t_{WOD}	–	35	–	40	–	45	ns

2 V Operation

DC Recommended Operating Ranges

T_a = –40 to +85 °C, V_{CC} = 2.0 to 2.4 V

Parameter	Symbol	Ratings			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	2.0	2.2	2.4	V
Input voltage	V_{IH}	V_{CC} – 0.4	–	V_{CC} + 0.3	V
	V_{IL}	–0.3	–	+0.4	V

DC Electrical Characteristics

T_a = –40 to +85 °C, V_{CC} = 2.0 to 2.4 V

Parameter		Symbol	Conditions		Ratings			Unit
					min.	typ.*	max.	
Input leakage current		I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0	–	+1.0	µA
I/O leakage current		I_{LO}	$V_{\overline{CE1}}$ = V_{IH} or V_{CE2} = V_{IL} or $V_{\overline{OE}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, $V_{I/O}$ = 0 V to V_{CC}		–1.0	–	+1.0	µA
Output high level voltage		V_{OH}	I_{OH} = –0.5 mA		V_{CC} – 0.2	–	–	V
Output low level voltage		V_{OL}	I_{OL} = 0.5 mA		–	–	0.2	V
Operating supply current	V_{CC} – 0.2 V/0.2 V input	I_{CCA1}	$V_{\overline{CE1}}$ ≤ 0.2 V, V_{CE2} ≥ V_{CC} – 0.2 V, $I_{I/O}$ = 0 mA, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V	T_a ≤ 70 °C	–	0.01	0.85	µA
				T_a ≤ 85 °C	–	–	2.5	µA
	V_{CC} – 0.4 V/0.4 V input	I_{CCA2}	$V_{\overline{CE1}}$ = V_{IL}, V_{CE2} = V_{IH}, $I_{I/O}$ = 0 mA, V_{IN} = V_{IH} or V_{IL}		–	–	2	mA
		I_{CCA3}	$V_{\overline{CE1}}$ = V_{IL}, V_{CE2} = V_{IH}, $I_{I/O}$ = 0 mA, duty = 100%	min. cycle	–	–	10	mA
				1 µs cycle	–	–	5	mA
Standby supply current	V_{CC} – 0.2 V/0.2 V input	I_{CCS1}	V_{CE2} ≤ 0.2 V or {$V_{\overline{CE1}}$ ≥ V_{CC} – 0.2 V, V_{CE2} ≥ V_{CC} – 0.2 V}	T_a ≤ 70 °C	–	0.01	0.85	µA
				T_a ≤ 85 °C	–	–	2.5	µA
	V_{CC} – 0.4 V/0.4 V input	I_{CCS2}	V_{CE2} = V_{IL} or $V_{\overline{CE1}}$ = V_{IH}, V_{IN} = 0 V to V_{CC}		–	–	800	µA

* V_{CC} = 2.2 V, T_a = 25 °C

AC Electrical Characteristics

T_a = –40 to +85 °C, V_{CC} = 2.0 to 2.4 V

AC test conditions

Input pulse voltage level: V_{IH} = V_{CC} – 0.4 V, V_{IL} = 0.4 V

Input rise and fall times: 10 ns

Input/output timing level: $V_{CC}/2$

Output load: 30 pF (including jig capacitance)

Read Cycle

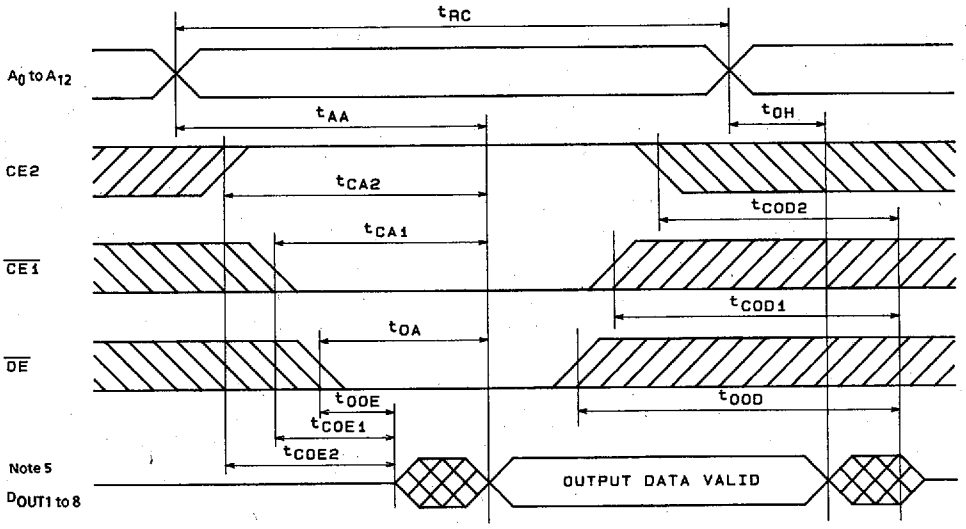
Parameter	Symbol	LC3564RM/RMF						Unit
		10LV		12LV		15LV		
		min.	max.	min.	max.	min.	max.	
Read cycle time	t_{RC}	200	–	250	–	300	–	ns
Address access time	t_{AA}	–	200	–	250	–	300	ns
$\overline{CE1}$ access time	t_{CA1}	–	200	–	250	–	300	ns
CE2 access time	t_{CA2}	–	200	–	250	–	300	ns
$\overline{OE}$ access time	t_{OA}	–	120	–	130	–	150	ns
Output hold time	t_{OH}	10	–	10	–	10	–	ns
$\overline{CE1}$ output enable time	t_{COE1}	10	–	10	–	10	–	ns
CE2 output enable time	t_{COE2}	10	–	10	–	10	–	ns
$\overline{OE}$ output enable time	t_{OOE}	5	–	5	–	5	–	ns
$\overline{CE1}$ output disable time	t_{COD1}	–	70	–	80	–	100	ns
CE2 output disable time	t_{COD2}	–	70	–	80	–	100	ns
$\overline{OE}$ output disable time	t_{OOD}	–	50	–	60	–	80	ns

Write Cycle

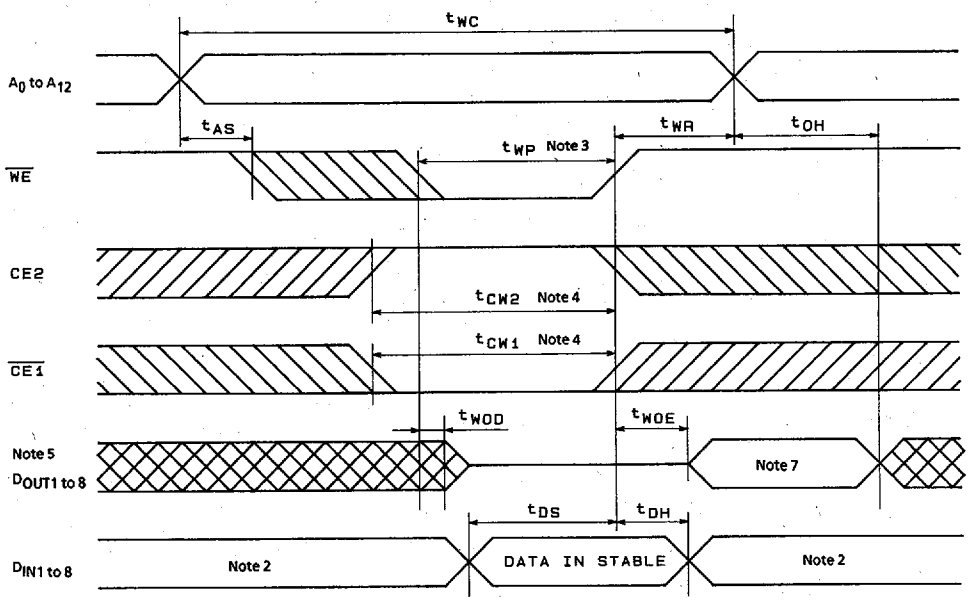
Parameter	Symbol	LC3564RM/RMF						Unit
		10LV		12LV		15LV		
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{WC}	200	–	250	–	300	–	ns
Address setup time	t_{AS}	0	–	0	–	0	–	ns
Write pulsewidth	t_{WP}	120	–	140	–	160	–	ns
$\overline{CE1}$ setup time	t_{CW1}	140	–	160	–	180	–	ns
CE2 setup time	t_{CW2}	140	–	160	–	180	–	ns
Write recovery time	t_{WR}	0	–	0	–	0	–	ns
$\overline{CE1}$ write recovery time	t_{WR1}	0	–	0	–	0	–	ns
CE2 write recovery time	t_{WR2}	0	–	0	–	0	–	ns
Data setup time	t_{DS}	120	–	130	–	150	–	ns
Data hold time	t_{DH}	0	–	0	–	0	–	ns
$\overline{CE1}$ data hold time	t_{DH1}	0	–	0	–	0	–	ns
CE2 data hold time	t_{DH2}	0	–	0	–	0	–	ns
$\overline{WE}$ output enable time	t_{WOE}	5	–	5	–	5	–	ns
$\overline{WE}$ output disable time	t_{WOD}	–	70	–	80	–	90	ns

Timing Chart

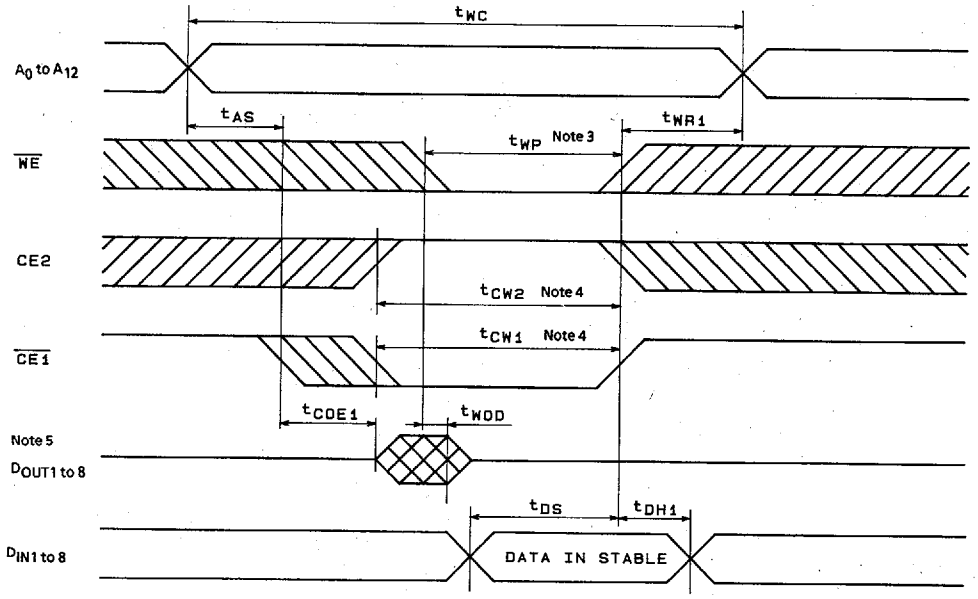
Read Cycle: Note 1



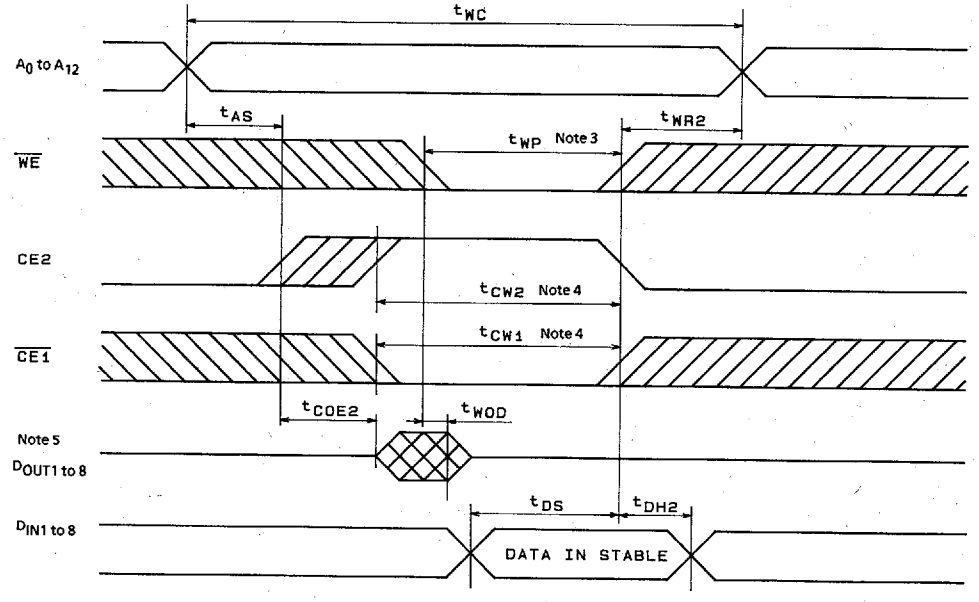
Write Cycle 1 ($\overline{WE}$ write): Note 6



Write Cycle 2 ($\overline{CE1}$ write): Note 6



Write Cycle 3 (CE2 write): Note 6



Notes

1. $\overline{WE}$ should be held HIGH during the read cycle.
2. Do not apply external signals that are out-of-phase with DOUT.
3. t_{WP} is a period when $\overline{CE1}$ and $\overline{WE}$ are LOW and CE2 is HIGH. It is measured from when $\overline{WE}$ goes LOW to when either $\overline{CE1}$ and $\overline{WE}$ go HIGH or CE2 goes LOW, whichever occurs first.
4. t_{CW1} and t_{CW2} are periods when $\overline{CE1}$ and $\overline{WE}$ are LOW and CE2 is HIGH. They are measured from when $\overline{CE1}$ goes LOW and CE2 goes HIGH, respectively, to when either $\overline{CE1}$ and $\overline{WE}$ go HIGH or CE2 goes LOW, whichever occurs first.
5. The outputs DOUT1 to DOUT8 are in a high-impedance state when $\overline{OE}$ is HIGH, $\overline{CE1}$ is HIGH, CE2 is LOW and $\overline{WE}$ is LOW.
6. During the write cycle, $\overline{OE}$ is V_{IH} or V_{IL}.
7. DOUT has the same phase as the write data.

Data Retention Characteristics

T_a = –40 to +85 °C

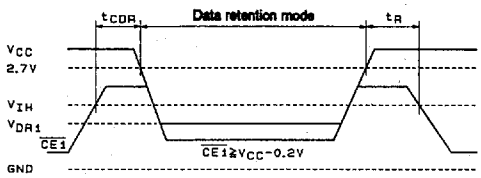
3 V Operation

Parameter	Symbol	Conditions	Ratings			Unit
			min.	typ.	max.	
Data retention supply voltage	V_{DR1}	$V_{\overline{CE1}} \geq V_{CC} - 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V or $V_{CE2} \leq 0.2$ V	2.0	–	–	V
	V_{DR2}	$V_{CE2} \leq 0.2$ V	2.0	–	–	V
Chip enable setup time	t_{CDR}		0	–	–	ns
Chip enable hold time	t_R		t_{RC}	–	–	ns

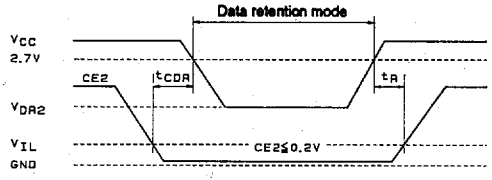
Note

t_{RC} is the read cycle time.

Data Retention Waveform 1 ($\overline{CE1}$ control)



Data Retention Waveform 2 (CE2 control)



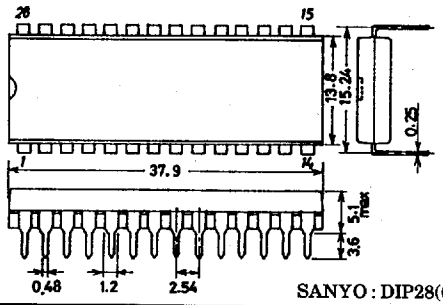
2 V Operation

Parameter	Symbol	Conditions	Ratings			Unit
			min.	typ.	max.	
Data retention supply voltage	V_{DR1}	$V_{\overline{CE1}} \geq V_{CC} - 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V or $V_{CE2} \leq 0.2$ V	2.0	–	–	V
	V_{DR2}	$V_{CE2} \leq 0.2$ V	2.0	–	–	V

MEMORY PACKAGE DIMENSIONS

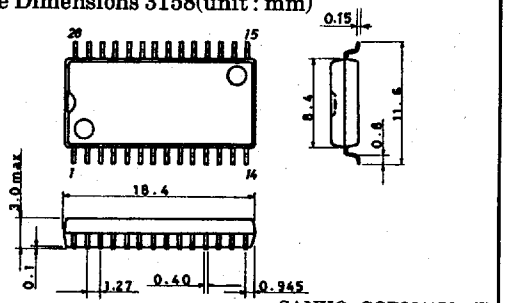
- All of Sanyo Memory package dimensions are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

Package Dimensions 3012A(unit : mm)



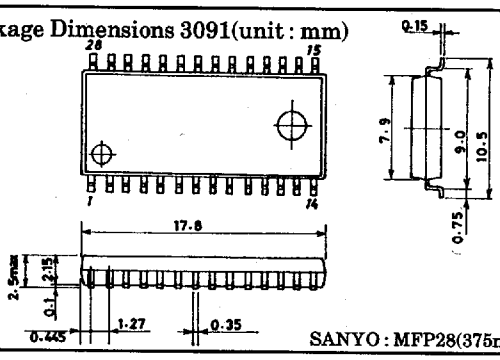
SANYO : DIP28(600mil)

Package Dimensions 3158(unit : mm)



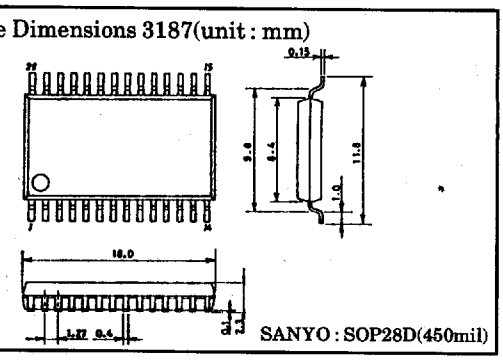
SANYO : SOP28(450mil)

Package Dimensions 3091(unit : mm)



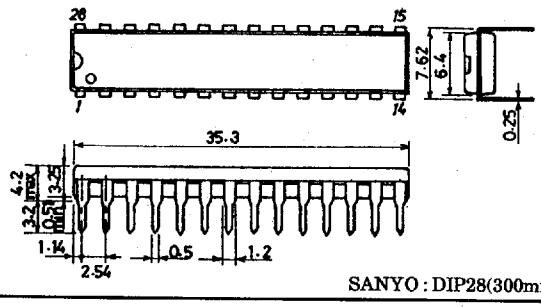
SANYO : MFP28(375mil)

Package Dimensions 3187(unit : mm)



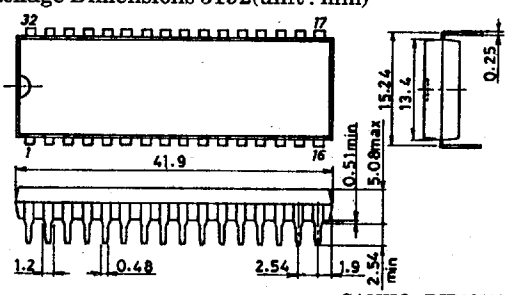
SANYO : SOP28D(450mil)

Package Dimensions 3123(unit : mm)



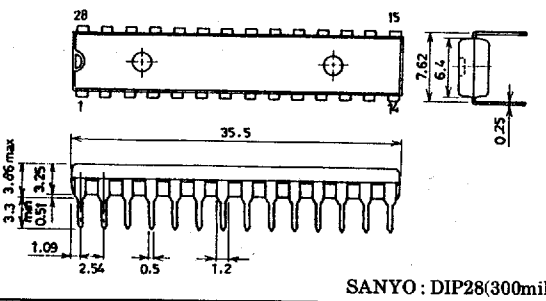
SANYO : DIP28(300mil)

Package Dimensions 3192(unit : mm)



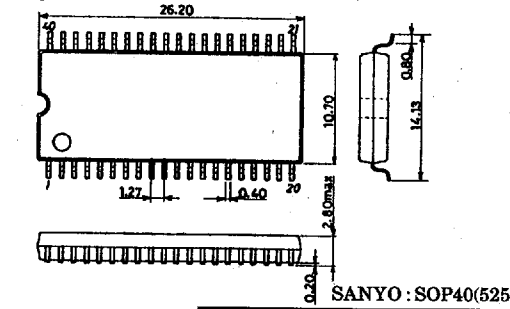
SANYO : DIP32(600mil)

Package Dimensions 3133 (unit : mm)



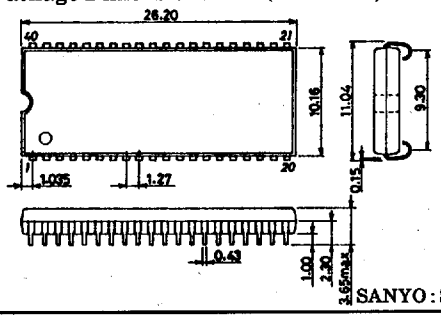
SANYO : DIP28(300mil)

Package Dimensions 3195(unit : mm)



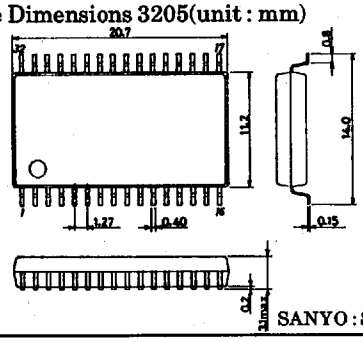
SANYO : SOP40(525mil)

Package Dimensions 3200(unit : mm)



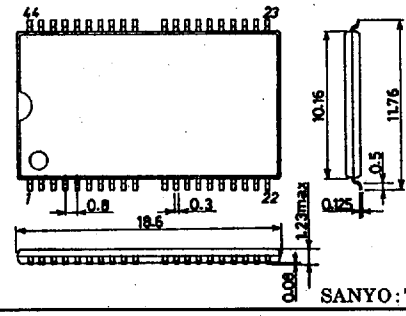
SANYO : SOJ40(400mil)

Package Dimensions 3205(unit : mm)



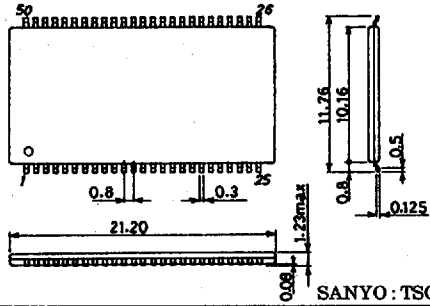
SANYO : SOP32(525mil)

Package Dimensions 3207(unit : mm)



SANYO : TSOP44 II

Package Dimensions 3211(unit : mm)



SANYO : TSOP50 II