

HM628512 Series

524288-word × 8-bit High Speed CMOS Static RAM

The Hitachi HM628512 is a 4M-bit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5 μ m Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400 mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. LP-version is suitable for battery back up system.

Features

- High speed: Fast access time 55/70/85/100 ns (max)
- Low power
Standby: 10 μ W (typ) (L/L-SL version)
Operation: 75 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L/L-SL version)

Ordering Information

Type No.	Access time	Package
HM628512P-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512P-7	70 ns	
HM628512P-8	85 ns	
HM628512P-10	100 ns	
HM628512LP-5	55 ns	
HM628512LP-7	70 ns	
HM628512LP-8	85 ns	
HM628512LP-10	100 ns	
HM628512LP-5SL	55 ns	
HM628512LP-7SL	70 ns	
HM628512LP-8SL	85 ns	
HM628512LP-10SL	100 ns	

Type No.	Access time	Package
HM628512FP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512FP-7	70 ns	
HM628512FP-8	85 ns	
HM628512FP-10	100 ns	
HM628512LFP-5	55 ns	
HM628512LFP-7	70 ns	
HM628512LFP-8	85 ns	
HM628512LFP-10	100 ns	
HM628512LFP-5SL	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512LFP-7SL	70 ns	
HM628512LFP-8SL	85 ns	
HM628512LFP-10SL	100 ns	
HM628512LTT-5*1	55 ns	
HM628512LTT-7*1	70 ns	
HM628512LTT-8*1	85 ns	
HM628512LTT-10*1	100 ns	
HM628512LTT-5SL*1	55 ns	
HM628512LTT-7SL*1	70 ns	
HM628512LTT-8SL*1	85 ns	
HM628512LTT-10SL*1	100 ns	
HM628512LRR-5*1	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512LRR-7*1	70 ns	
HM628512LRR-8*1	85 ns	
HM628512LRR-10*1	100 ns	
HM628512LRR-5SL*1	55 ns	
HM628512LRR-7SL*1	70 ns	
HM628512LRR-8SL*1	85 ns	
HM628512LRR-10SL*1	100 ns	

Note: 1. Preliminary

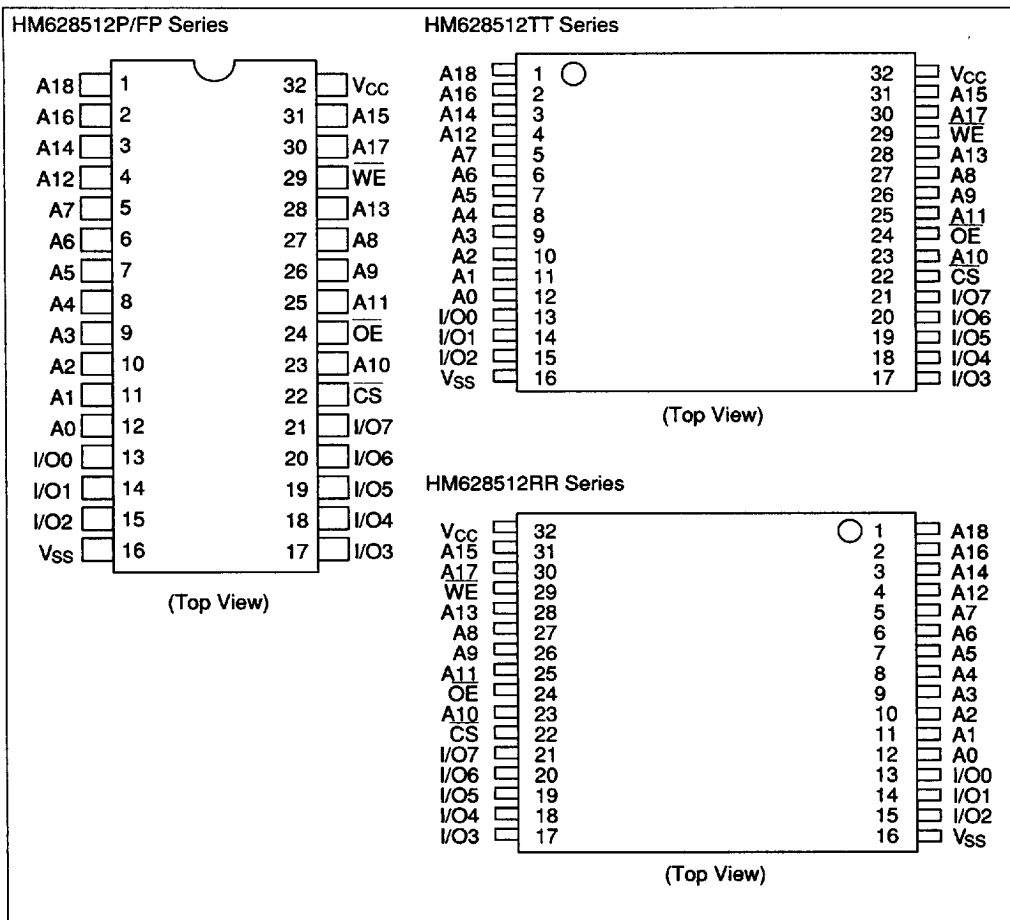
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Pin Arrangement



Pin Description

Symbol	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
CS	Chip select
WE	Write enable

Symbol	Function
OE	Output enable
Vcc	Power supply
Vss	Ground

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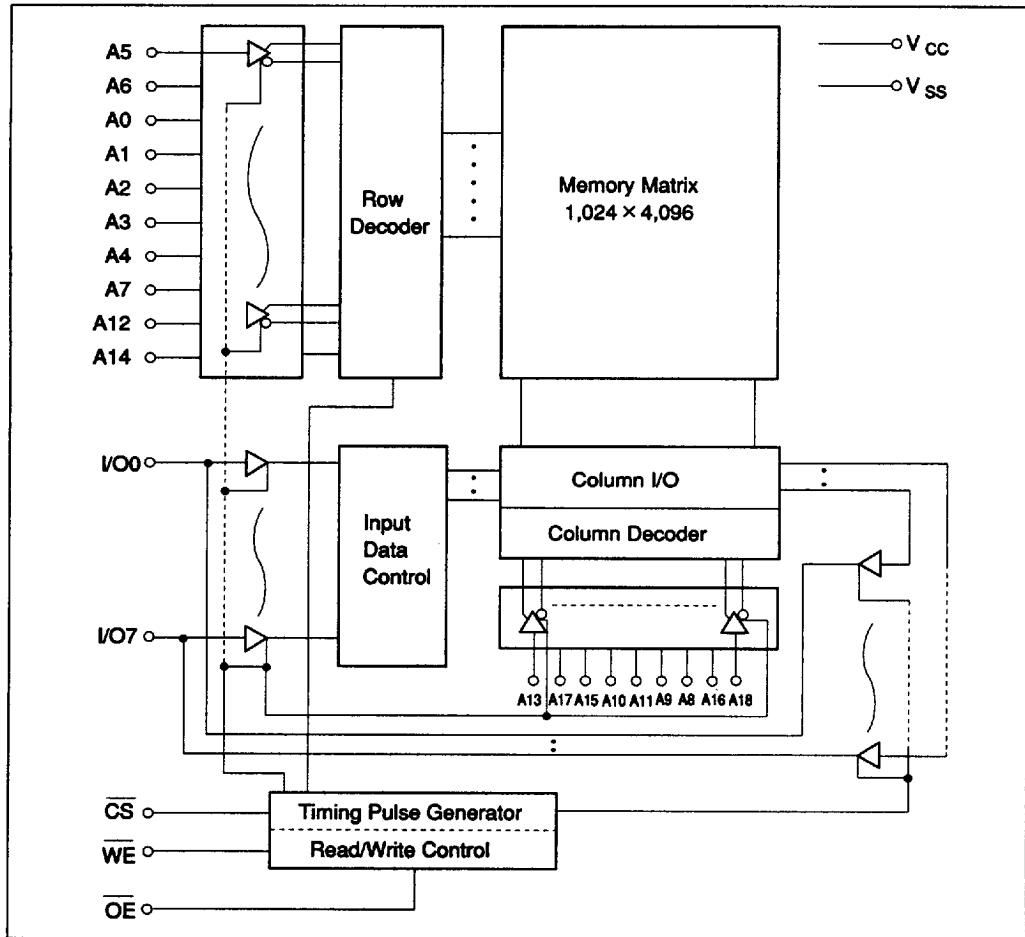
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Block Diagram



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Function Table

WE	CS	OE	Mode	V _{CC} current	Dout pin	Ref. cycle
X	H	X	Not selected	I _{SB} , I _{SB1}	High-Z	—
H	L	H	Output disable	I _{CC}	High-Z	—
H	L	L	Read	I _{CC}	Dout	Read cycle
L	L	H	Write	I _{CC}	Din	Write cycle (1)
L	L	L	Write	I _{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _T	−0.5 ^{*1} to +7.0	V
Power dissipation	P _T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. −3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high (logic 1) voltage	V _{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V _{IL}	−0.3 ^{*1}	—	0.8	V

Note: 1. −3.0 V for pulse half-width ≤ 30 ns

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter		Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current		$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current		$ I_{LO} $	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $WE = V_{IL}$, $V_{I/O} = V_{SS} \text{ to } V_{CC}$
Operating power supply current: DC		I_{CCREAD}	—	15	25	mA	$\overline{CS} = V_{IL}$, $WE = V_{IH}$, others = V_{IH}/V_{IL} , $I_{I/O} = 0 \text{ mA}$
		$I_{CCWRITE}$	—	20	45	mA	$\overline{CS} = V_{IL}$, $WE = V_{IL}$, others = V_{IH}/V_{IL} , $I_{I/O} = 0 \text{ mA}$
Operating power supply current	−5	I_{CC1}	—	70	100	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} $I_{I/O} = 0 \text{ mA}$
	−7		—	60	90	mA	
	−8/10		—	55	80	mA	
		I_{CC2}	—	15	35	mA	Cycle time = 1 μs , duty = 100% $I_{I/O} = 0 \text{ mA}$, $\overline{CS} \leq 0.2 \text{ V}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$, $V_{IL} \leq 0.2 \text{ V}$
Standby power supply current: DC		I_{SB}	—	1	3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC		I_{SB1}	—	0.02	2	mA	$V_{in} \geq 0 \text{ V}$, $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
	—		2	100*2	μA		
	—		2	50*3	μA		
Output low voltage		V_{OL}	—	—	0.4	V	$I_{OL} = 2.1 \text{ mA}$
Output high voltage		V_{OH}	2.4	—	—	V	$I_{OH} = -1.0 \text{ mA}$

- Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.
 2. This characteristics is guaranteed only for L-version.
 3. This characteristics is guaranteed only for L-SL version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)*1

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	C_{in}	—	8	pF	$V_{in} = 0\text{ V}$
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall times: 5 ns
- Output load: 1 TTL Gate + C_L (100 pF)
(Including scope & jig)

Read Cycle

Parameter	Symbol	HM628512-5		HM628512-7		HM628512-8		HM628512-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	55	—	70	—	85	—	100	—	ns	
Address access time	t_{AA}	—	55	—	70	—	85	—	100	ns	
Chip select access time	t_{CO}	—	55	—	70	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	25	—	35	—	45	—	50	ns	
Chip selection to output in low-Z	t_{LZ}	10	—	10	—	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{HZ}	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	0	30	0	35	ns	1, 2, 3
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns	

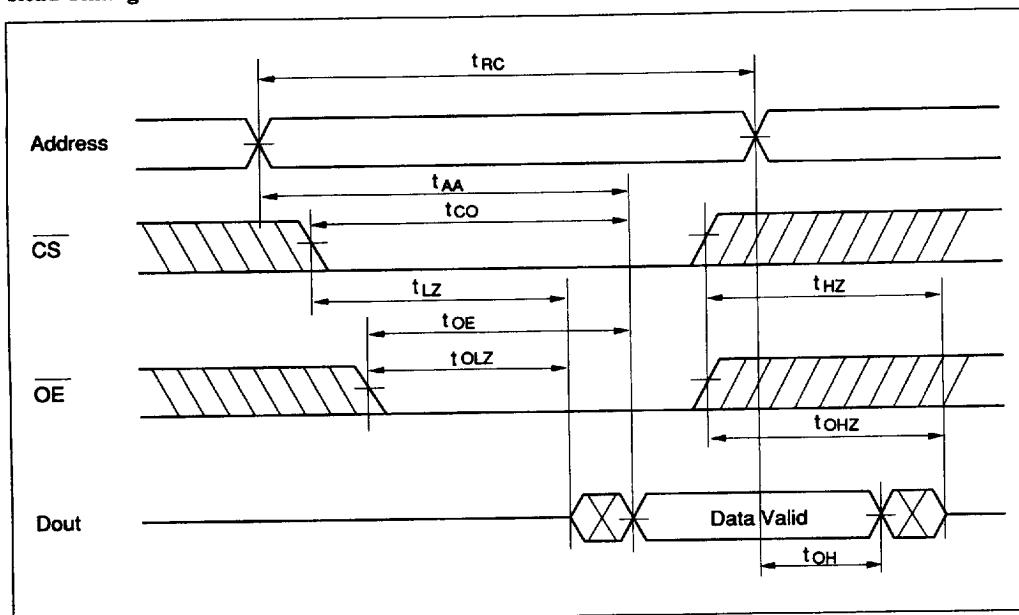
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5-83

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Read Timing Waveform *4



- Notes:
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min.
 3. This parameter is sampled and not 100% tested.
 4. WE is high for read cycle.

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5-84

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Write Cycle

Parameter	Symbol	HM628512-5		HM628512-7		HM628512-8		HM628512-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t _{WC}	55	—	70	—	85	—	100	—	ns	
Chip selection to end of write	t _{CW}	50	—	60	—	75	—	80	—	ns	2
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns	3
Address valid to end of write	t _{AW}	50	—	60	—	75	—	80	—	ns	
Write pulse width	t _{WP}	40	—	50	—	55	—	60	—	ns	1, 12
Write recovery time	t _{WR}	5	—	5	—	5	—	5	—	ns	4
WE to output in high-Z	t _{WHZ}	0	20	0	25	0	30	0	35	ns	10, 11
Data to write time overlap	t _{DW}	25	—	30	—	35	—	40	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns	
Output active from end of write	t _{OW}	5	—	5	—	5	—	5	—	ns	10

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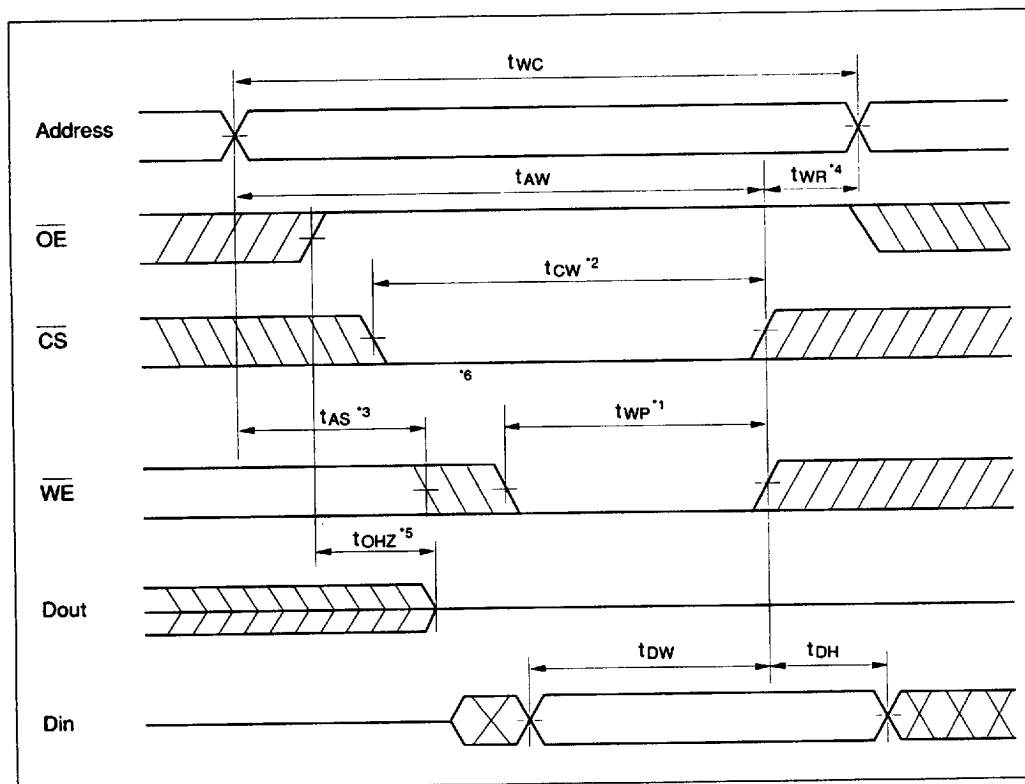
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5-85

HM628512 Series

Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



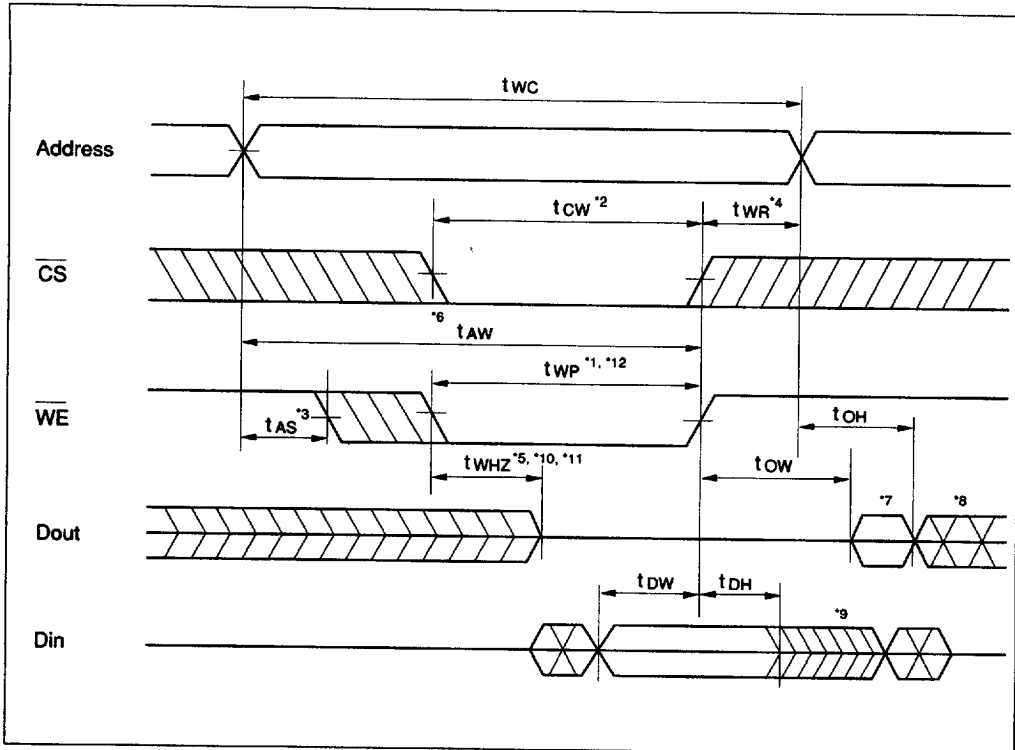
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Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



- Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
 2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
 3. t_{AS} is measured from the address valid to the beginning of write.
 4. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
 5. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 6. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
 7. $\overline{Dout}$ is the same phase of the write data of this write cycle.
 8. $\overline{Dout}$ is the read data of next address.
 9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
 10. This parameter is sampled and not 100% tested.
 11. t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referred to output voltage levels.
 12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention.

$$t_{WP} \geq t_{OW} \text{ min} + t_{WHZ} \text{ max}$$

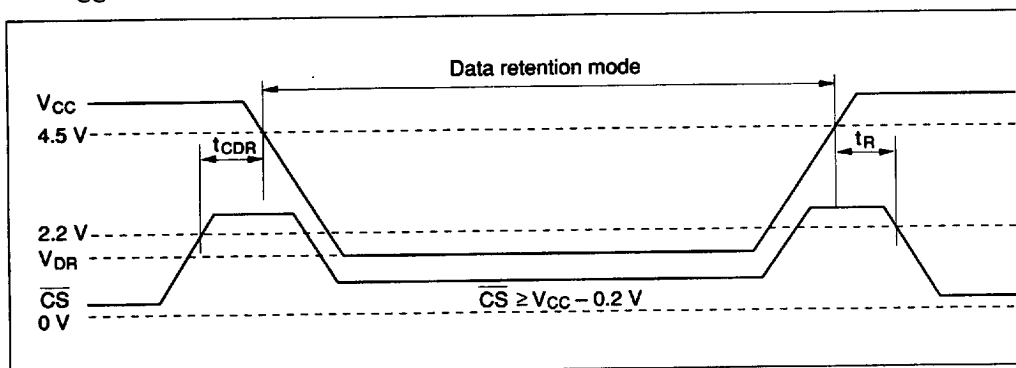
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Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L/L-SL version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions ^{*3}
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \geq 0 \text{ V}$
Data retention current	I_{CCDR}	—	1	50^{*1}	μA	$V_{CC} = 3.0 \text{ V}$, $V_{in} \geq 0 \text{ V}$ $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
		—	1	15^{*2}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

Low V_{CC} Data Retention Timing Waveform ($\overline{CS}$ Controlled)



- Notes:
1. For L-version and $20 \mu\text{A}$ max. at $T_a = 0$ to 40°C .
 2. For SL-version and $3 \mu\text{A}$ max. at $T_a = 0$ to 40°C .
 3. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and D_{in} buffer. In data retention mode, V_{in} levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

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5-88

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