# GAL22V10B
# GAL22V10

## High Performance E²CMOS PLD

T-46-19-07

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## FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - 7.5 ns Maximum Propagation Delay
  - Fmax = 111 MHz
  - 5 ns Maximum from Clock Input to Data Output
  - TTL Compatible 16 mA Outputs
  - UltraMOS® Advanced CMOS Technology
- **ACTIVE PULL-UPS ON ALL PINS**
- **COMPATIBLE WITH STANDARD 22V10 DEVICES**
  - Fully Function/Fuse-Map/Parametric Compatible with Bipolar and UVCMOS 22V10 Devices
- **50% REDUCTION IN POWER VERSUS BIPOLAR**
- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<100ms)
  - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
  - Maximum Flexibility for Complex Logic Designs
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

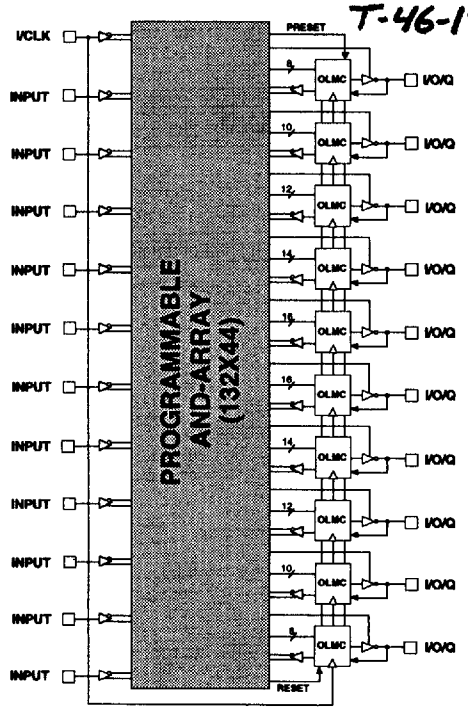
## DESCRIPTION

The GAL22V10B, at 7.5ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10/B to consume much less power when compared to bipolar 22V10 devices. E² technology offers high speed (<100ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

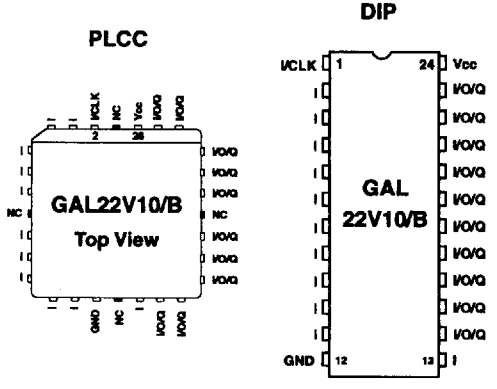
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10/B is fully function/fuse map/parametric compatible with standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

## FUNCTIONAL BLOCK DIAGRAM




## PACKAGE DIAGRAMS



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May 1992

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# Specifications *GAL22V10B* *GAL22V10*

## GAL22V10/B ORDERING INFORMATION

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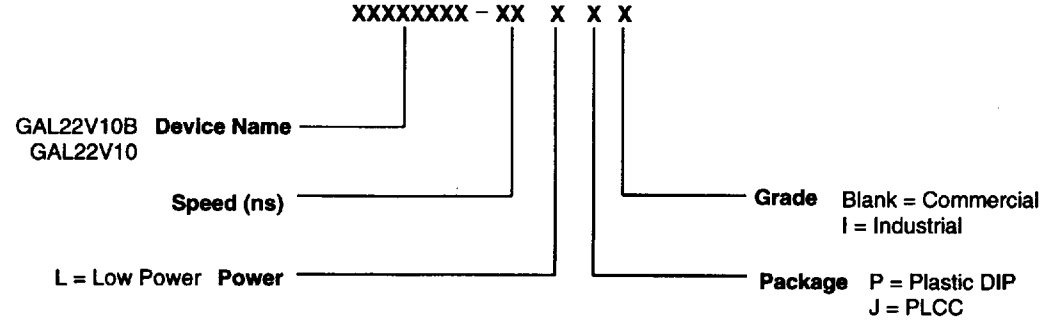
### Commercial Grade Specifications

| Tpd (ns) | Tsu (ns) | Tco (ns) | Icc (mA) | Ordering # | Package |
|---|---|---|---|---|---|
| 7.5 | 6.5 | 5 | 140 | GAL22V10B-7LP | 24-Pin Plastic DIP |
| | | | 140 | GAL22V10B-7LJ | 28-Lead PLCC |
| 10 | 7 | 7 | 130 | GAL22V10B-10LP | 24-Pin Plastic DIP |
| | | | 130 | GAL22V10B-10LJ | 28-Lead PLCC |
| 15 | 10 | 8 | 130 | GAL22V10B-15LP | 24-Pin Plastic DIP |
| | | | 130 | GAL22V10B-15LJ | 28-Lead PLCC |
| 25 | 15 | 15 | 90 | GAL22V10B-25LP | 24-Pin Plastic DIP |
| | | | 90 | GAL22V10B-25LJ | 28-Lead PLCC |
| | | | 130 | GAL22V10-25LP | 24-Pin Plastic DIP |
| | | | 130 | GAL22V10-25LJ | 28-Lead PLCC |

### Industrial Grade Specifications

| Tpd (ns) | Tsu (ns) | Tco (ns) | Icc (mA) | Ordering # | Package |
|---|---|---|---|---|---|
| 15 | 10 | 8 | 150 | GAL22V10B-15LPI | 24-Pin Plastic DIP |
| | | | 150 | GAL22V10B-15LJI | 28-Lead PLCC |
| 20 | 14 | 10 | 150 | GAL22V10B-20LPI | 24-Pin Plastic DIP |
| | | | 150 | GAL22V10B-20LJI | 28-Lead PLCC |
| 25 | 15 | 15 | 150 | GAL22V10B-25LPI | 24-Pin Plastic DIP |
| | | | 150 | GAL22V10B-25LJI | 28-Lead PLCC |

## PART NUMBER DESCRIPTION



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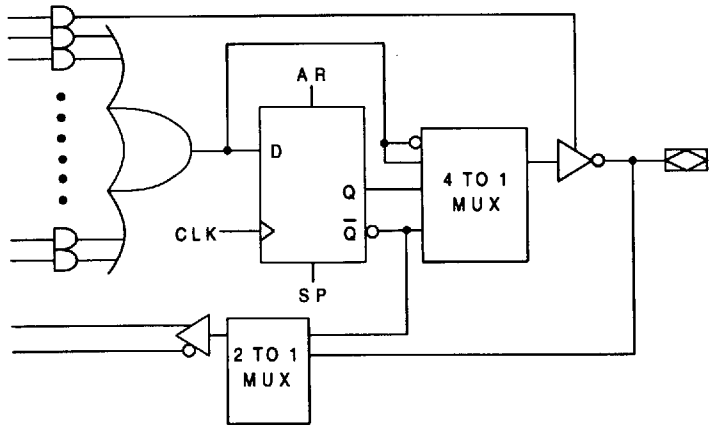
## OUTPUT LOGIC MACROCELL (OLMC)

The GAL22V10/B has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19). In addition to the product terms available for logic, each OLMC has an additional product-term dedicated to output enable control.

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinatorial or registered mode. This allows each output to be individually configured as either active high or active low.

The GAL22V10/B has a product term for Asynchronous Reset (AR) and a product term for Synchronous Preset (SP). These two product terms are common to all registered OLMCs. The Asynchronous Reset sets all registers to zero any time this dedicated product term is asserted. The Synchronous Preset sets all registers to a logic one on the rising edge of the next clock pulse after this product term is asserted.

NOTE: The AR and SP product terms will force the Q output of the flip-flop into the same state regardless of the polarity of the output. Therefore, a reset operation, which sets the register output to a zero, may result in either a high or low at the output pin, depending on the pin polarity chosen.




**GAL22V10/B OUTPUT LOGIC MACROCELL (OLMC)**

## OUTPUT LOGIC MACROCELL CONFIGURATIONS

Each of the Macrocells of the GAL22V10/B has two primary functional modes: registered, and combinatorial I/O. The modes and the output polarity are set by two bits (SO and S1), which are normally controlled by the logic compiler. Each of these two primary modes, and the bit settings required to enable them, are described below and on the following page.

### REGISTERED

In registered mode the output pin associated with an individual OLMC is driven by the Q output of that OLMC's D-type flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each OLMC, and can therefore be defined by a logic equation. The D flip-flop's /Q output is fed back into the AND array, with both the true and complement of the feedback available as inputs to the AND array.

NOTE: In registered mode, the feedback is from the /Q output of the register, and not from the pin; therefore, a pin defined as registered is an output only, and cannot be used for dynamic I/O, as can the combinatorial pins.

### COMBINATORIAL I/O

In combinatorial mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or inverted (active low). Output tri-state control is available as an individual product-term for each output, and may be individually set by the compiler as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feedback into the AND array is from the pin side of the output enable buffer. Both polarities (true and inverted) of the pin are fed back into the AND array.

## REGISTERED MODE

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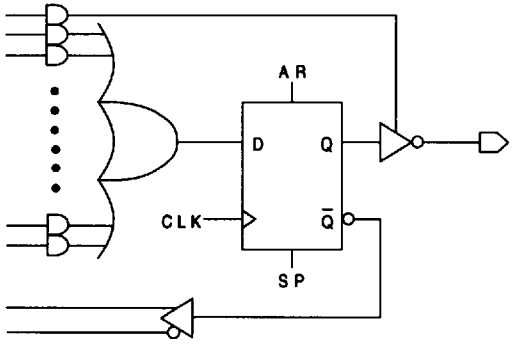
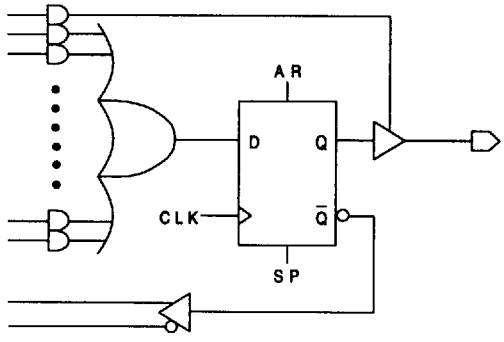



**ACTIVE LOW**

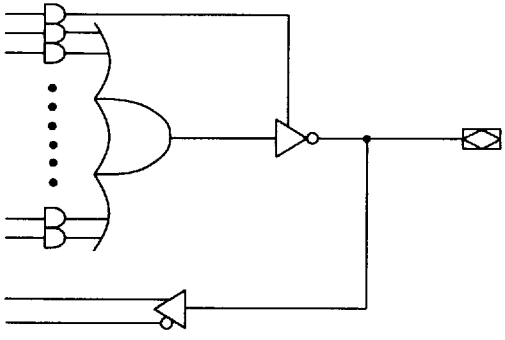
$S_0 = 0$
$S_1 = 0$




**ACTIVE HIGH**

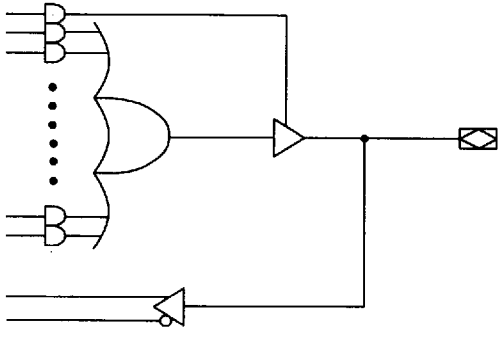
$S_0 = 1$
$S_1 = 0$

## COMBINATORIAL MODE



**ACTIVE LOW**

$S_0 = 0$
$S_1 = 1$



**ACTIVE HIGH**

$S_0 = 1$
$S_1 = 1$

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# Specifications GAL22V10B GAL22V10

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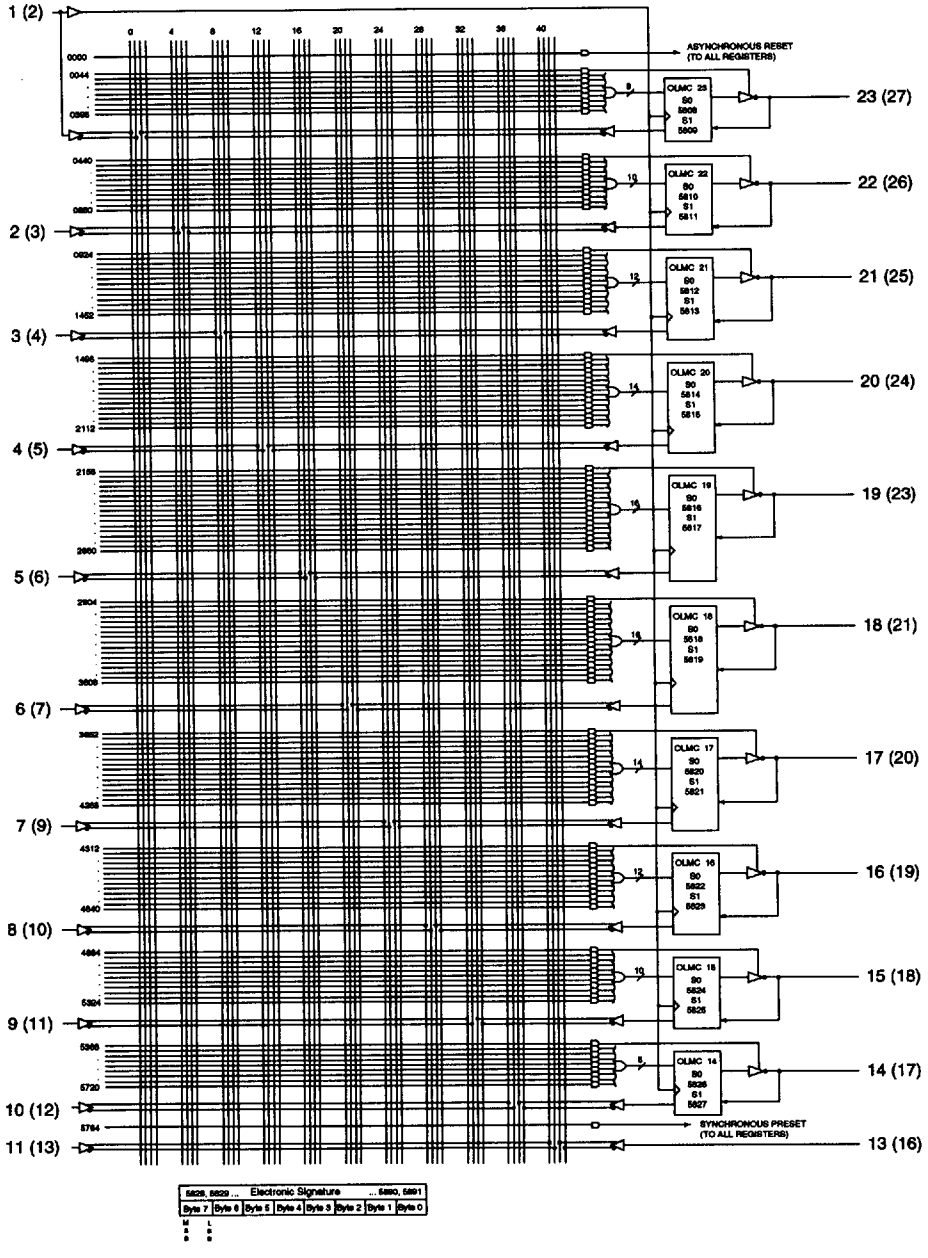
## GAL22V10/B LOGIC DIAGRAM / JEDEC FUSE MAP

**DIP (PLCC) Package Pinouts**

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# Specifications *GAL22V10B*
## Commercial

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## ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage $V_{CC}$ ..... -0.5 to +7V

Input voltage applied ..... -2.5 to $V_{CC}$ +1.0V
Off-state output voltage applied ..... -2.5 to $V_{CC}$ +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## RECOMMENDED OPERATING COND.

**Commercial Devices:**
Ambient Temperature ($T_A$) ..... 0 to +75°C
Supply voltage ($V_{CC}$)
with Respect to Ground ..... +4.75 to +5.25V

## DC ELECTRICAL CHARACTERISTICS

**Over Recommended Operating Conditions (Unless Otherwise Specified)**

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP.3 | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | Vss – 0.5 | — | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | — | Vcc+1 | V |
| $I_{IL}$1 | Input or I/O Low Leakage Current | $0V \le V_{IN} \le V_{IL}$ (MAX.) | — | — | –100 | µA |
| $I_{IH}$ | Input or I/O High Leakage Current | $3.5V \le V_{IN} \le V_{CC}$ | — | — | 10 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = MAX. Vin = $V_{IL}$ or $V_{IH}$ | — | — | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = MAX. Vin = $V_{IL}$ or $V_{IH}$ | 2.4 | — | — | V |
| $I_{OL}$ | Low Level Output Current | | — | — | 16 | mA |
| $I_{OH}$ | High Level Output Current | | — | — | –3.2 | mA |
| $I_{OS}$2 | Output Short Circuit Current | $V_{CC}$ = 5V $V_{OUT}$ = 0.5V $T_A$ = 25°C | –30 | — | –130 | mA |
| $I_{CC}$ | Operating Power Supply Current | $V_{IL}$ = 0.5V $V_{IH}$ = 3.0V, Outputs Open, $f_{toggle}$ = 25MHz, -7 | — | 90 | 140 | mA |
| | | $V_{IL}$ = 0.5V $V_{IH}$ = 3.0V, Outputs Open, $f_{toggle}$ = 25MHz, -10/-15 | — | 90 | 130 | mA |
| | | $V_{IL}$ = 0.5V $V_{IH}$ = 3.0V, Outputs Open, $f_{toggle}$ = 15MHz, -25 | — | 75 | 90 | mA |

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and $T_A$ = 25 °C

## CAPACITANCE ($T_A$ = 25 C, f = 1.0 MHz)

| SYMBOL | PARAMETER | MAXIMUM* | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_I$ | Input Capacitance | 8 | pF | $V_{CC}$ = 5.0V, $V_I$ = 2.0V |
| $C_{I/O}$ | I/O Capacitance | 8 | pF | $V_{CC}$ = 5.0V, $V_{I/O}$ = 2.0V |

*Guaranteed but not 100% tested.

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# Specifications *GAL22V10B* Commercial

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## AC SWITCHING CHARACTERISTICS

**Over Recommended Operating Conditions**

| PARAMETER | TEST COND.[1] | DESCRIPTION | -7 | | -10 | | -15 | | -25 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{pd}$ | 1 | Input or I/O to Combinatorial Output | 3 | 7.5 | 3 | 10 | 3 | 15 | 3 | 25 | ns |
| $t_{co}$ | 1 | Clock to Output Delay | 2 | 5 | 2 | 7 | 2 | 8 | 2 | 15 | ns |
| $t_{cf}$[2] | — | Clock to Feedback Delay | — | 2.5 | — | 2.5 | — | 2.5 | — | 13 | ns |
| $t_{su_1}$ | — | Setup Time, Input or Feedback before Clock | 6.5 | — | 7 | — | 10 | — | 15 | — | ns |
| $t_{su_2}$ | — | Setup Time, SP before Clock | 10 | — | 10 | — | 10 | — | 15 | — | ns |
| $t_h$ | — | Hold Time, Input or Feedback after Clock | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $f_{max}$[3] | 1 | Maximum Clock Frequency with External Feedback, 1/(tsu + tco) | 87 | — | 71.4 | — | 55.5 | — | 33.3 | — | MHz |
| | 1 | Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf) | 111 | — | 105 | — | 80 | — | 35.7 | — | MHz |
| | 1 | Maximum Clock Frequency with No Feedback | 111 | — | 105 | — | 83.3 | — | 38.5 | — | MHz |
| $t_{wh}$ | — | Clock Pulse Duration, High | 4 | — | 4 | — | 6 | — | 13 | — | ns |
| $t_{wl}$ | — | Clock Pulse Duration, Low | 4 | — | 4 | — | 6 | — | 13 | — | ns |
| $t_{en}$ | 2 | Input or I/O to Output Enabled | 3 | 8 | 3 | 10 | 3 | 15 | 3 | 25 | ns |
| $t_{dis}$ | 3 | Input or I/O to Output Disabled | 3 | 8 | 3 | 9 | 3 | 15 | 3 | 25 | ns |
| $t_{ar}$ | 1 | Input or I/O to Asynchronous Reset of Register | 3 | 13 | 3 | 13 | 3 | 20 | 3 | 25 | ns |
| $t_{arw}$ | — | Asynchronous Reset Pulse Duration | 8 | — | 8 | — | 15 | — | 25 | — | ns |
| $t_{arr}$ | — | Asynchronous Reset to Clock Recovery Time | 8 | — | 8 | — | 10 | — | 25 | — | ns |
| $t_{spr}$ | — | Synchronous Preset to Clock Recovery Time | 10 | — | 10 | — | 10 | — | 15 | — | ns |

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

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# Specifications *GAL22V10*
## Commercial

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## ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage $V_{CC}$ ..... -0.5 to +7V
Input voltage applied ..... -2.5 to $V_{CC}$ +1.0V
Off-state output voltage applied ..... -2.5 to $V_{CC}$ +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## RECOMMENDED OPERATING COND.

**Commercial Devices:**
Ambient Temperature ($T_A$) ..... 0 to +75°C
Supply voltage ($V_{CC}$)
with Respect to Ground ..... +4.75 to +5.25V

## DC ELECTRICAL CHARACTERISTICS

**Over Recommended Operating Conditions (Unless Otherwise Specified)**

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP.[3] | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | Vss – 0.5 | — | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | — | Vcc+1 | V |
| $I_{IL}$[1] | Input or I/O Low Leakage Current | $0V \le V_{IN} \le V_{IL}$ (MAX.) | — | — | –150 | µA |
| $I_{IH}$ | Input or I/O High Leakage Current | $3.5V \le V_{IN} \le V_{CC}$ | — | — | 10 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = MAX. Vin = $V_{IL}$ or $V_{IH}$ | — | — | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = MAX. Vin = $V_{IL}$ or $V_{IH}$ | 2.4 | — | — | V |
| $I_{OL}$ | Low Level Output Current | | — | — | 16 | mA |
| $I_{OH}$ | High Level Output Current | | — | — | –3.2 | mA |
| $I_{OS}$[2] | Output Short Circuit Current | $V_{CC}$ = 5V $V_{OUT}$ = 0.5V $T_A$ = 25°C | –50 | — | –135 | mA |
| $I_{CC}$ | Operating Power Supply Current | VIL = 0.5V VIH = 3.0V $f_{toggle}$ = 15Mhz Outputs Open | — | 90 | 130 | mA |

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and $T_A$ = 25 °C

## CAPACITANCE ($T_A$ = 25 C, f = 1.0 MHz)

| SYMBOL | PARAMETER | MAXIMUM* | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_I$ | Input Capacitance | 8 | pF | $V_{CC}$ = 5.0V, $V_I$ = 2.0V |
| $C_{I/O}$ | I/O Capacitance | 10 | pF | $V_{CC}$ = 5.0V, $V_{I/O}$ = 2.0V |

*Guaranteed but not 100% tested.

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# Specifications *GAL22V10* Commercial

T-46-19-07

## AC SWITCHING CHARACTERISTICS

**Over Recommended Operating Conditions**

| PARAMETER | TEST COND.[1] | DESCRIPTION | -25 | | UNITS |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| $t_{pd}$ | 1 | Input or I/O to Combinatorial Output | 3 | 25 | ns |
| $t_{co}$ | 1 | Clock to Output Delay | 2 | 15 | ns |
| $t_{cf}$[2] | — | Clock to Feedback Delay | — | 13 | ns |
| $t_{su}$ | — | Setup Time, Input or Feedback before Clock | 15 | — | ns |
| $t_h$ | — | Hold Time, Input or Feedback after Clock | 0 | — | ns |
| $f_{max}$[3] | 1 | Maximum Clock Frequency with External Feedback, 1/(tsu + tco) | 33.3 | — | MHz |
| | 1 | Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf) | 35.7 | — | MHz |
| | 1 | Maximum Clock Frequency with No Feedback | 38.5 | — | MHz |
| $t_{wh}$ | — | Clock Pulse Duration, High | 13 | — | ns |
| $t_{wl}$ | — | Clock Pulse Duration, Low | 13 | — | ns |
| $t_{en}$ | 2 | Input or I/O to Output Enabled | 3 | 25 | ns |
| $t_{dis}$ | 3 | Input or I/O to Output Disabled | 3 | 25 | ns |
| $t_{ar}$ | 1 | Input or I/O to Asynchronous Reset of Register | 3 | 25 | ns |
| $t_{arw}$ | — | Asynchronous Reset Pulse Duration | 25 | — | ns |
| $t_{arr}$ | — | Asynchronous Reset to Clock Recovery Time | 25 | — | ns |
| $t_{spr}$ | — | Synchronous Preset to Clock Recovery Time | 15 | — | ns |

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

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# Specifications *GAL22V10B*
## Industrial

T-46-19-07

## ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage $V_{CC}$ ..... -0.5 to +7V
Input voltage applied ..... -2.5 to $V_{CC}$ +1.0V
Off-state output voltage applied ..... -2.5 to $V_{CC}$ +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## RECOMMENDED OPERATING COND.

**Industrial Devices:**
Ambient Temperature ($T_A$) ..... -40 to 85°C
Supply voltage ($V_{CC}$)
with Respect to Ground ..... +4.50 to +5.50V

## DC ELECTRICAL CHARACTERISTICS

**Over Recommended Operating Conditions (Unless Otherwise Specified)**

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP.[3] | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | Vss – 0.5 | — | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | — | Vcc+1 | V |
| $I_{IL}$[1] | Input or I/O Low Leakage Current | $0V \le V_{IN} \le V_{IL}$ (MAX.) | — | — | -100 | µA |
| $I_{IH}$ | Input or I/O High Leakage Current | $3.5V \le V_{IN} \le V_{CC}$ | — | — | 10 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = MAX. Vin = $V_{IL}$ or $V_{IH}$ | — | — | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = MAX. Vin = $V_{IL}$ or $V_{IH}$ | 2.4 | — | — | V |
| $I_{OL}$ | Low Level Output Current | | — | — | 16 | mA |
| $I_{OH}$ | High Level Output Current | | — | — | –3.2 | mA |
| $I_{OS}$[2] | Output Short Circuit Current | $V_{CC}$ = 5V $V_{OUT}$ = 0.5V $T_A$ = 25°C | –30 | — | –130 | mA |
| $I_{CC}$ | Operating Power Supply Current | $V_{IL}$ = 0.5V $V_{IH}$ = 3.0V Outputs Open; $f_{toggle}$ = 25MHz | — | 90 | 150 | mA |
| | | $f_{toggle}$ = 15MHz | | | | |

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and $T_A$ = 25 °C

## CAPACITANCE ($T_A$ = 25 C, f = 1.0 MHz)

| SYMBOL | PARAMETER | MAXIMUM* | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_I$ | Input Capacitance | 8 | pF | $V_{CC}$ = 5.0V, $V_I$ = 2.0V |
| $C_{I/O}$ | I/O Capacitance | 8 | pF | $V_{CC}$ = 5.0V, $V_{I/O}$ = 2.0V |

*Guaranteed but not 100% tested.

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# Specifications *GAL22V10B* Industrial

## AC SWITCHING CHARACTERISTICS

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**Over Recommended Operating Conditions**

| PARAMETER | TEST COND.[1] | DESCRIPTION | -15 | | -20 | | -25 | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_{pd}$ | 1 | Input or I/O to Combinatorial Output | 3 | 15 | 3 | 20 | 3 | 25 | ns |
| $t_{co}$ | 1 | Clock to Output Delay | 2 | 8 | 2 | 10 | 2 | 25 | ns |
| $t_{cf}$[2] | — | Clock to Feedback Delay | — | 5 | — | 8 | — | 13 | ns |
| $t_{su_1}$ | — | Setup Time, Input or Feedback before Clock | 10 | — | 14 | — | 15 | — | ns |
| $t_{su_2}$ | — | Setup Time, SP before Clock | 12 | — | 14 | — | 15 | — | ns |
| $t_h$ | — | Hold Time, Input or Feedback after Clock | 0 | — | 0 | — | 0 | — | ns |
| $f_{max}$[3] | 1 | Maximum Clock Frequency with External Feedback, 1/(tsu + tco) | 55.5 | — | 41.6 | — | 33 | — | MHz |
| | 1 | Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf) | 66.6 | — | 45.4 | — | 35.7 | — | MHz |
| | 1 | Maximum Clock Frequency with No Feedback | 66.6 | — | 50 | — | 38.5 | — | MHz |
| $t_{wh}$ | — | Clock Pulse Duration, High | 6 | — | 10 | — | 13 | — | ns |
| $t_{wl}$ | — | Clock Pulse Duration, Low | 6 | — | 10 | — | 13 | — | ns |
| $t_{en}$ | 2 | Input or I/O to Output Enabled | 3 | 15 | 3 | 20 | 3 | 25 | ns |
| $t_{dis}$ | 3 | Input or I/O to Output Disabled | 3 | 15 | 3 | 20 | 3 | 25 | ns |
| $t_{ar}$ | 1 | Input or I/O to Asynchronous Reset of Register | 3 | 20 | 3 | 25 | 3 | 25 | ns |
| $t_{arw}$ | — | Asynchronous Reset Pulse Duration | 15 | — | 20 | — | 25 | — | ns |
| $t_{arr}$ | — | Asynchronous Reset to Clock Recovery Time | 10 | — | 20 | — | 25 | — | ns |
| $t_{spr}$ | — | Synchronous Preset to Clock Recovery Time | 12 | — | 14 | — | 15 | — | ns |

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.

2

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# Specifications GAL22V10B GAL22V10

## SWITCHING WAVEFORMS

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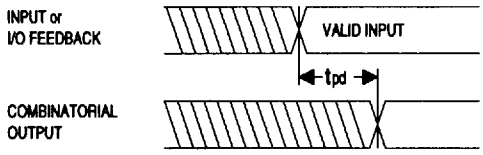
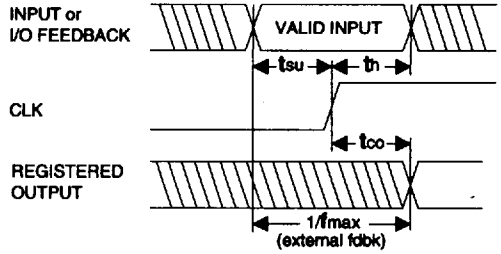
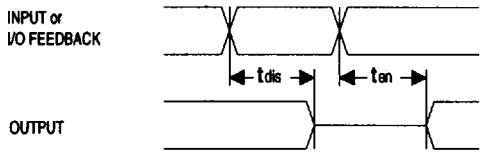


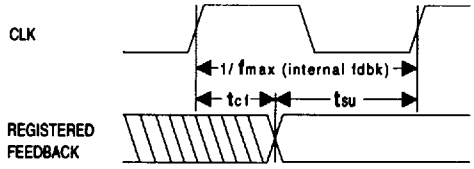

**Combinatorial Output**



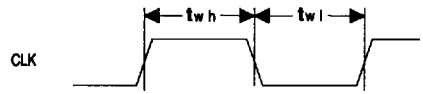

**Registered Output**



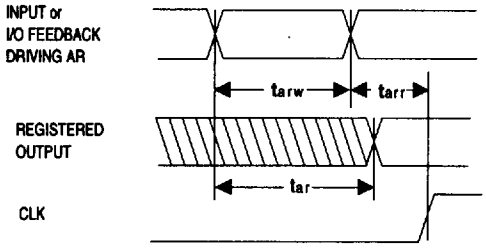

**Input or I/O to Output Enable/Disable**



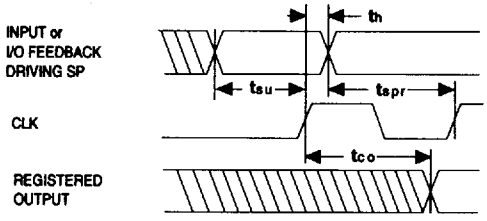

**fmax with Feedback**




**Clock Width**




**Asynchronous Reset**




**Synchronous Preset**

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# Specifications GAL22V10B GAL22V10

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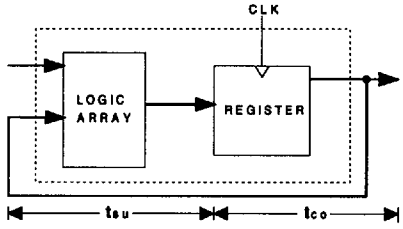
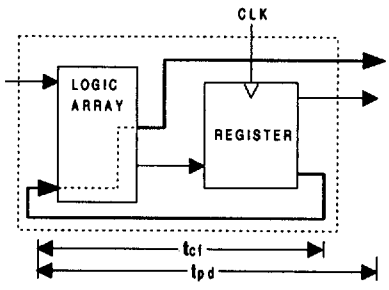
## fmax DESCRIPTIONS



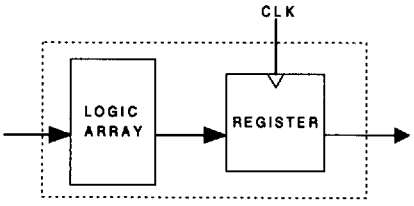

**fmax with External Feedback 1/(tsu+tco)**

**Note:** fmax with external feedback is calculated from measured tsu and tco.




**fmax with Internal Feedback 1/(tsu+tcf)**

**Note:** tcf is a calculated value, derived by subtracting tsu from the period of fmax w/ internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.




**fmax With No Feedback**

**Note:** fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.

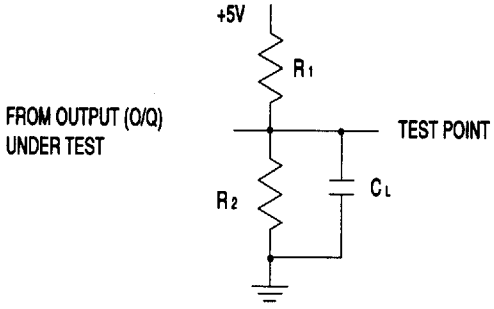
## SWITCHING TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 2 – 3ns 10% – 90% |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| Output Load | See Figure |

3-state levels are measured 0.5V from steady-state active level.

**Output Load Conditions (see figure)**

| Test Condition | | $R_1$ | $R_2$ | $C_L$ |
|---|---|---|---|---|
| 1 | | 300Ω | 390Ω | 50pF |
| 2 | Active High | ∞ | 390Ω | 50pF |
| | Active Low | 300Ω | 390Ω | 50pF |
| 3 | Active High | ∞ | 390Ω | 5pF |
| | Active Low | 300Ω | 390Ω | 5pF |




$C_L$ INCLUDES JIG AND PROBE TOTAL CAPACITANCE

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# Specifications GAL22V10B GAL22V10

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## ELECTRONIC SIGNATURE

An electronic signature is provided in every GAL22V10/B device. It contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

The electronic signature is an additional feature not present in other manufacturers' 22V10 devices. To use the extra feature of the user-programmable electronic signature it is necessary to choose a Lattice 22V10 device type when compiling a set of logic equations. In addition, many device programmers have two separate selections for the device, typically a GAL22V10 and a GAL22V10-UES (UES = User Electronic Signature) or GAL22V10-ES. This allows users to maintain compatibility with existing 22V10 designs, while still having the option to use the GAL device's extra feature.

The JEDEC map for the GAL22V10/B contains the 64 extra fuses for the electronic signature, for a total of 5892 fuses. However, the GAL22V10/B device can still be programmed with a standard 22V10 JEDEC map (5828 fuses) with any qualified device programmer.

## SECURITY CELL

A security cell is provided in every GAL22V10/B device to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

## LATCH-UP PROTECTION

GAL22V10/B devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

## DEVICE PROGRAMMING

GAL devices are programmed using a Lattice-approved Logic Programmer, available from a number of manufacturers (see the the GAL Development Tools section). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

## OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because certain events may occur during system operation that throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

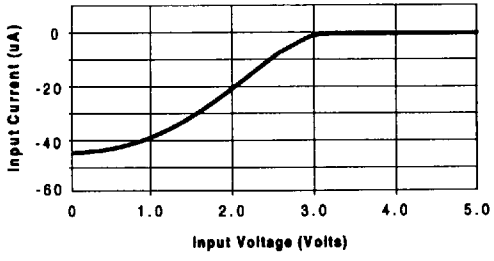
The GAL22V10/B device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

## INPUT BUFFERS

GAL22V10/B devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The input and I/O pins also have built-in active pull-ups. As a result, floating inputs will float to a TTL high (logic 1). However, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, Vcc, or ground. Doing so will tend to improve noise immunity and reduce Icc for the device. (See equivalent input and I/O schematics on the following page.)

**Typical Input Current**



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# Specifications GAL22V10B GAL22V10

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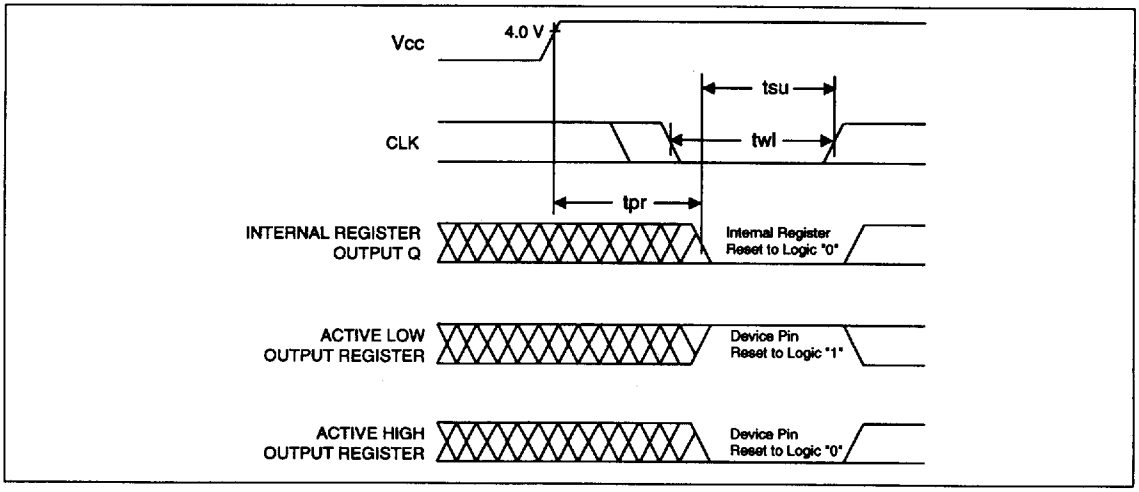
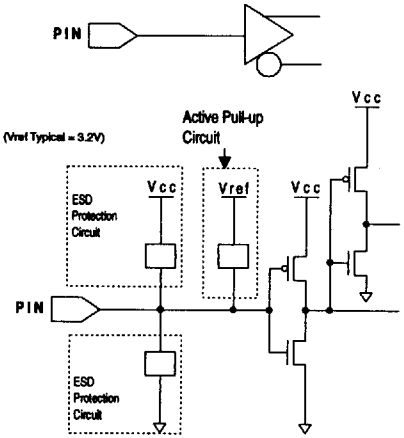
## POWER-UP RESET

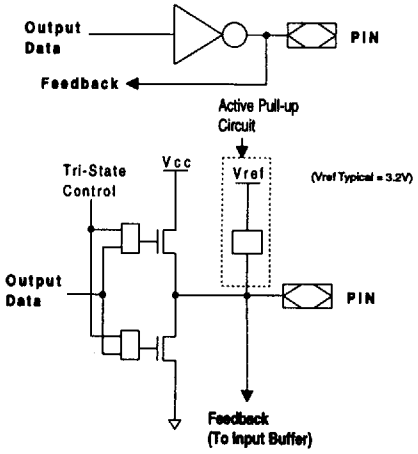



Circuitry within the GAL22V10/B provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will be either high or low on power-up, depending on the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

## INPUT/OUTPUT EQUIVALENT SCHEMATICS




Input




Output

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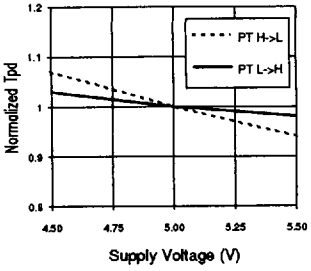
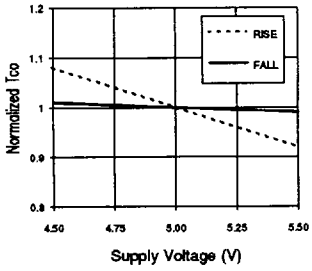
# Specifications *GAL22V10B*
# Typical Characteristics

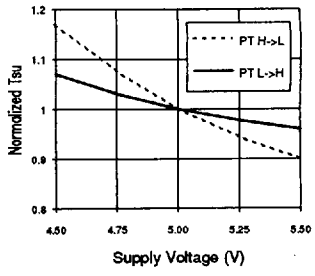
**Normalized Tpd vs Vcc**



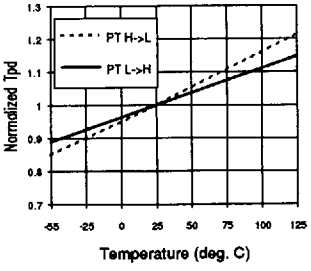

**Normalized Tco vs Vcc**



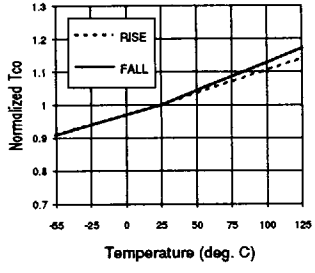

**Normalized Tsu vs Vcc**



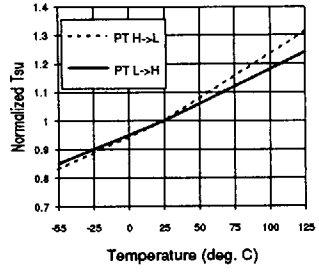

**Normalized Tpd vs Temp**



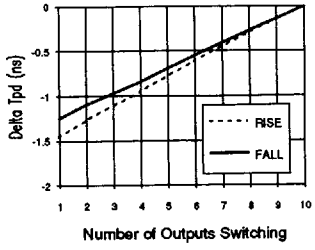

**Normalized Tco vs Temp**



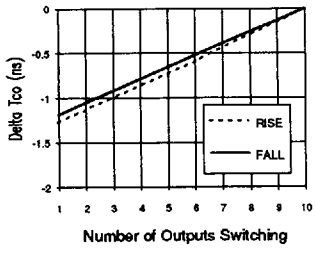

**Normalized Tsu vs Temp**



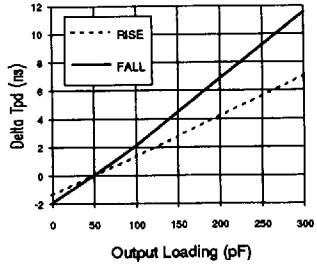

**Delta Tpd vs # of Outputs Switching**



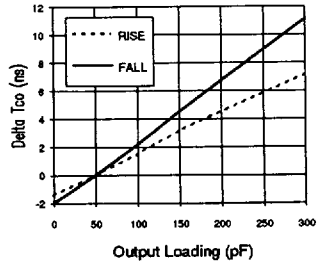

**Delta Tco vs # of Outputs Switching**




**Delta Tpd vs Output Loading**




**Delta Tco vs Output Loading**



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# Specifications *GAL22V10B*

## Typical Characteristics

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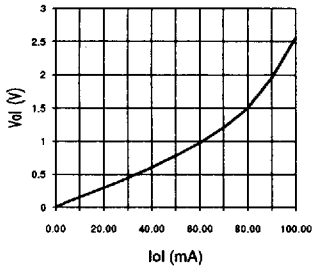
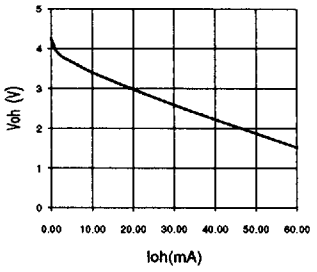
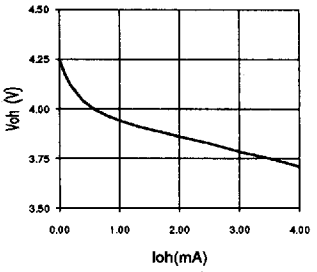
**Vol vs Iol**



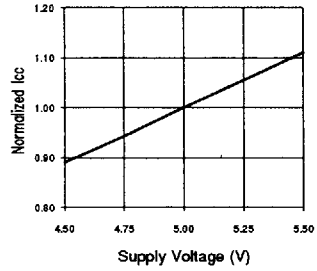

**Voh vs Ioh**



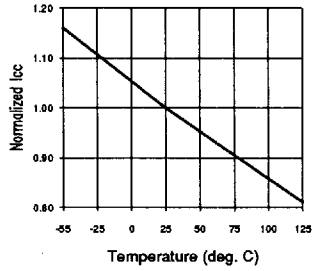

**Voh vs Ioh**



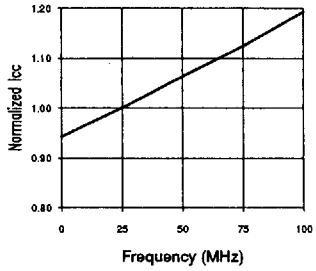

**Normalized Icc vs Vcc**



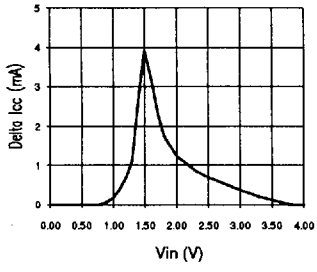

**Normalized Icc vs Temp**



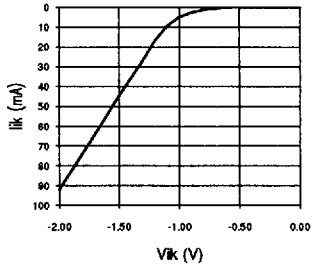

**Normalized Icc vs Freq.**




**Delta Icc vs Vin (1 Input)**




**Input Clamp (Vik)**



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# Specifications *GAL22V10*
## Typical Characteristics

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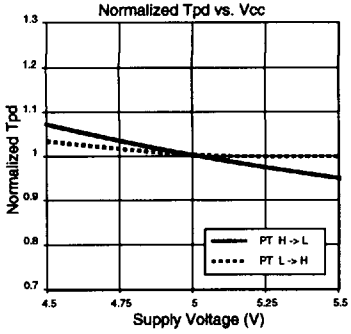
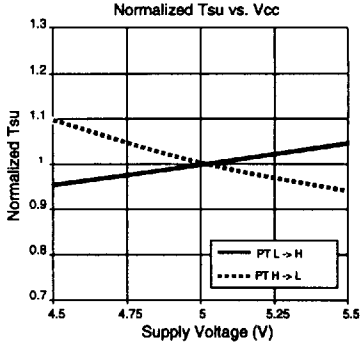
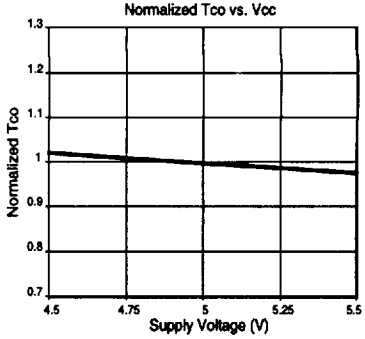
Normalized Tpd vs. Vcc



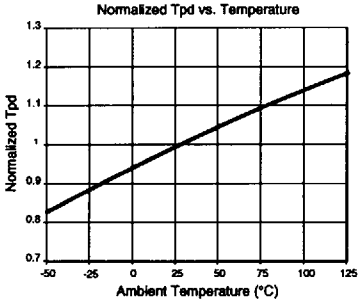

Normalized Tsu vs. Vcc



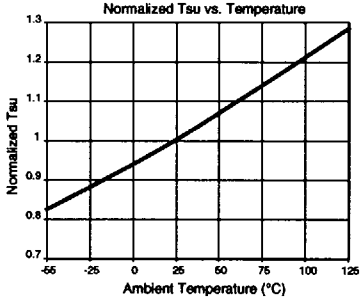

Normalized Tco vs. Vcc



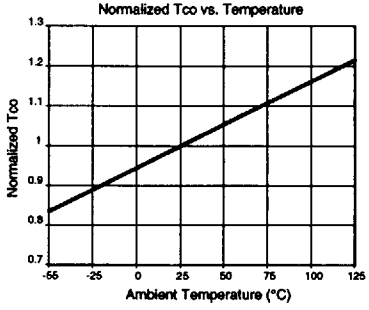

Normalized Tpd vs. Temperature



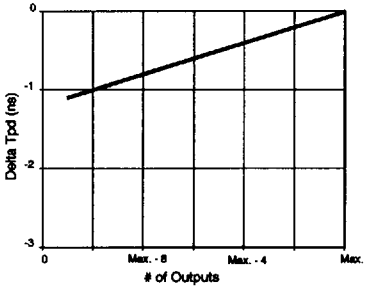

Normalized Tsu vs. Temperature



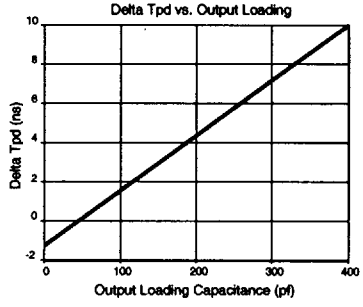

Normalized Tco vs. Temperature



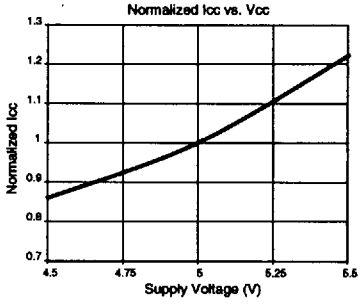

Delta Tpd vs. # of Outputs Switching



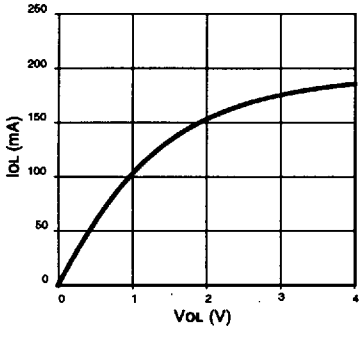

Delta Tpd vs. Output Loading



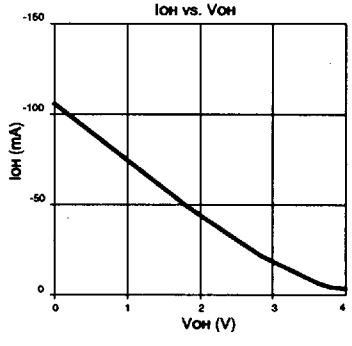

Normalized Icc vs. Vcc




$I_{OL}$ vs. $V_{OL}$




$I_{OH}$ vs. $V_{OH}$




Normalized Icc vs. Temperature