



CYPRESS
SEMICONDUCTOR

T-46-23-14

CYM1841

256K x 32 Static RAM Module

Features

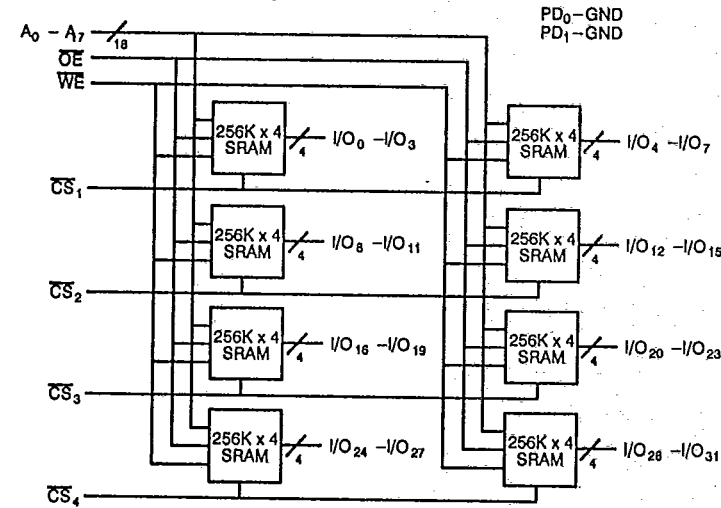
- High-density 8-megabit SRAM module
- High-speed CMOS SRAMs
— Access time of 20 ns
- Low active power
— 5.3W (max.) at 25 ns
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
— Max. height of .58 in.
- Small PCB footprint
— 1.3 sq. in.
- JEDEC-compatible pinout
- Available in SIMM or ZIP format

Functional Description

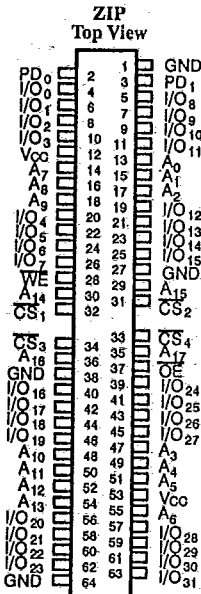
The CYM1841 is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects (CS_1, CS_2, CS_3, CS_4) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects. Writing to each byte is accomplished when the appropriate chipselect (CS_N) and write enable (WE) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip select (CS_N) LOW while write enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X). The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH. Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram



Pin Configuration



1841-1

1841-2

Selection Guide

	1841-20	1841-25	1841-30	1841-35	1841-45	1841-55
Maximum Access Time (ns)	20	25	30	35	45	55
Maximum Operating Current (mA)	1120	960	960	960	960	960
Maximum Standby Current (mA)	480	480	480	480	480	480

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature - 55°C to +125°C
 Ambient Temperature with
 Power Applied - 10°C to +85°C
 Supply Voltage to Ground Potential - 0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State - 0.5V to +7.0V
 DC Input Voltage - 0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

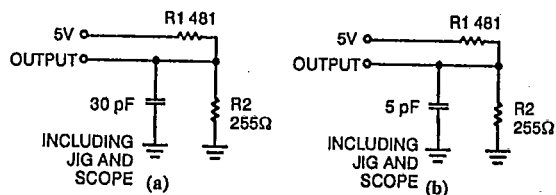
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1841		Units
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		- 0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	- 16	+16	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	- 10	+10	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, C _{SN} ≤ V _{IL}	25, 30, 35 ns	960	mA
			20 ns	1120	mA
I _{SB1}	Automatic CS Power-Down Current ^[1]	Max. V _{CC} , C _{SN} ≥ V _{IH} , Min. Duty Cycle = 100%		480	mA
I _{SB2}	Automatic CS Power-Down Current ^[2]	Max. V _{CC} , C _{SN} ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V		16	mA

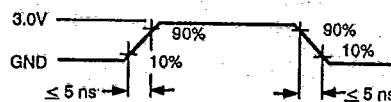
Capacitance^[2]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	70	pF
C _{OUT}	Output Capacitance		20	pF

- Notes:
1. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
 2. Tested on a sample basis.

AC Test Loads and Waveforms

1841-3



1841-4

Equivalent to: THEVENIN EQUIVALENT
 167Ω
 OUTPUT ——— 1.73V



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Switching Characteristics Over the Operating Range^[3]

Parameters	Description	1841-20		1841-25		1841-30		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	20		25		30		ns
t _{AA}	Address to Data Valid		20		25		30	ns
t _{OHA}	Output Hold from Address Change	5		5		5		ns
t _{ACS}	CS LOW to Data Valid		20		25		30	ns
t _{DOE}	OE LOW to Data Valid		13		15		20	ns
t _{LZOE}	OE LOW to Low Z	0		0		0		ns
t _{HZOE}	OE HIGH to High Z		15		15		15	ns
t _{LZCS}	CS LOW to Low Z ^[4]	10		10		10		ns
t _{HZCS}	CS HIGH to High Z ^[4,5]		20		20		20	ns
t _{PD}	CS HIGH to Power Down		20		25		30	ns
WRITE CYCLE ^[6]								
t _{WC}	Write Cycle Time	20		25		30		ns
t _{SCS}	CS LOW to Write End	18		20		25		ns
t _{AW}	Address Set-Up to Write End	18		20		25		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	2		2		2		ns
t _{PWE}	WE Pulse Width	15		20		25		ns
t _{SD}	Data Set-Up to Write End	13		15		15		ns
t _{HD}	Data Hold from Write End	2		2		2		ns
t _{LZWE}	WE HIGH to Low Z ^[4]	0		0		0		ns
t _{HZWE}	WE LOW to High Z ^[4,5]	0	15	0	15	0	15	ns

Parameters	Description	1841-35		1841-45		1841-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	35		45		55		ns
t _{AA}	Address to Data Valid		35		45		55	ns
t _{OHA}	Output Hold from Address Change	5		5		5		ns
t _{ACS}	CS LOW to Data Valid		35		45		55	ns
t _{DOE}	OE LOW to Data Valid		25		30		35	ns
t _{LZOE}	OE LOW to Low Z	0		0		0		ns
t _{HZOE}	OE HIGH to High Z		15		15		15	ns
t _{LZCS}	CS LOW to Low Z ^[4]	10		10		10		ns
t _{HZCS}	CS HIGH to High Z ^[4, 5]		20		20		20	ns
t _{PD}	CS HIGH to Power Down		35		45		55	ns



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Switching Characteristics Over the Operating Range^[3] (continued)

Parameters	Description	1841-35		1841-45		1841-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE ^[6]								
tWC	Write Cycle Time	35		45		55		ns
tSCS	CS LOW to Write End	30		40		50		ns
tAW	Address Set-Up to Write End	30		40		50		ns
tHA	Address Hold from Write End	2		2		2		ns
tSA	Address Set-Up to Write Start	2		2		2		ns
tPWE	WE Pulse Width	30		35		45		ns
tSD	Data Set-Up to Write End	20		25		35		ns
tHD	Data Hold from Write End	2		2		2		ns
tLZWE	WE HIGH to Low Z ^[4]	0		0		0		ns
tHZWE	WE LOW to High Z ^[4, 5]	0	15	0	15	0	15	ns

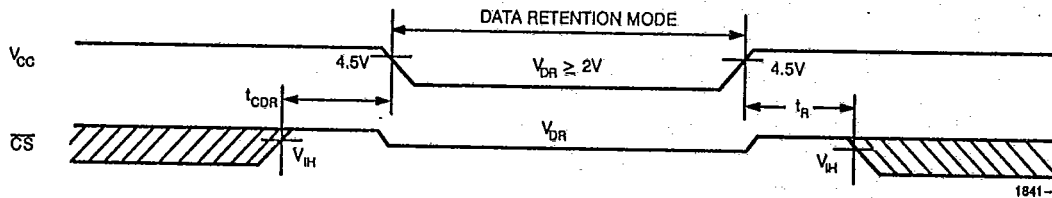
Data Retention Characteristics Over the Operating Range (L Version Only)

Parameters	Description	Test Conditions	1841		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$V_{CC} = 2.0V$, $CE \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			800	μA
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[7]}$	Operation Recovery Time		5		ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
- t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- Guaranteed, not tested.

Data Retention Waveform

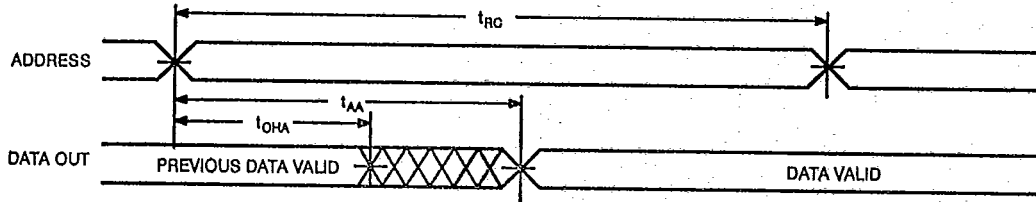


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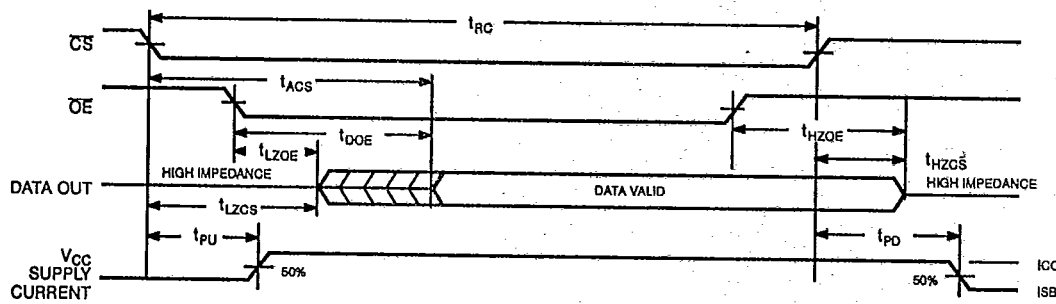
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Switching Waveforms^[8]

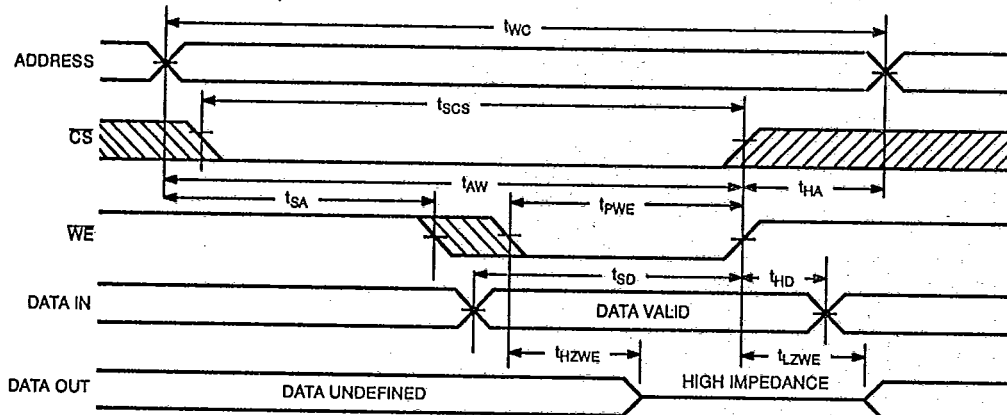
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Read Cycle No. 1^[9,10]

1841-8

Read Cycle No. 2^[9,11]

1841-6

Write Cycle No. 1 (WE Controlled)^[6]

1841-7

Notes:

8. $\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, and $\overline{CS}_4$ are represented by $\overline{CS}$ in the Switching Characteristics and Switching Waveforms sections.
9. $\overline{WE}$ is HIGH for read cycle.

10. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
11. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

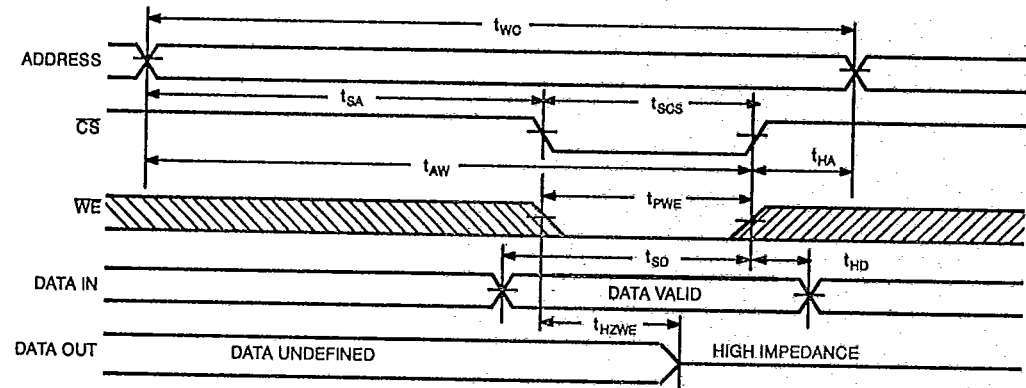


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Switching Waveforms (continued)

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Write Cycle No. 2 (CS Controlled)[6, 12]



1841-9

Notes:
12. If CS goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.

Truth Table

CS _N	WE	OE	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CYM1841PM-20C	PM02	Commercial
	CYM1841PN-20C	PN02	
	CYM1841PZ-20C	PZ03	
25	CYM1841PM-25C	PM02	Commercial
	CYM1841PN-25C	PN02	
	CYM1841PZ-25C	PZ03	
30	CYM1841PM-30C	PM02	Commercial
	CYM1841LPM-30C	PM02	
	CYM1841PN-30C	PN02	
	CYM1841LPN-30C	PN02	
	CYM1841PZ-30C	PZ03	
	CYM1841LPZ-30C	PZ03	
35	CYM1841PM-35C	PM02	Commercial
	CYM1841LPM-35C	PM02	
	CYM1841PN-35C	PN02	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CYM1841LPN-35C	PN02	Commercial
	CYM1841PZ-35C	PZ03	
	CYM1841LPZ-35C	PZ03	
45	CYM1841PM-45C	PM02	Commercial
	CYM1841LPM-45C	PM02	
	CYM1841PN-45C	PN02	
	CYM1841LPN-45C	PN02	
	CYM1841PZ-45C	PZ03	
	CYM1841LPZ-45C	PZ03	
55	CYM1841PM-55C	PM02	Commercial
	CYM1841LPM-55C	PM02	
	CYM1841PN-55C	PN02	
	CYM1841LPN-55C	PN02	
	CYM1841LPZ-55C	PZ03	

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MODULES