世紀民生 MYSON CENTURY, INC.

CS5826

Dual Pixel LVDS Display Interface (LDI) Transmitter

GENERAL DESCRIPTION

The CS5826 converts 48 bits (Dual pixel 24-bit color) of CMOS/TTL data into 8 LVDS (Low Voltage Differential Signalling) data streams. Control signals (VSYNC, HSYNC, DE and two user-defined signals) are sent during blanking intervals.

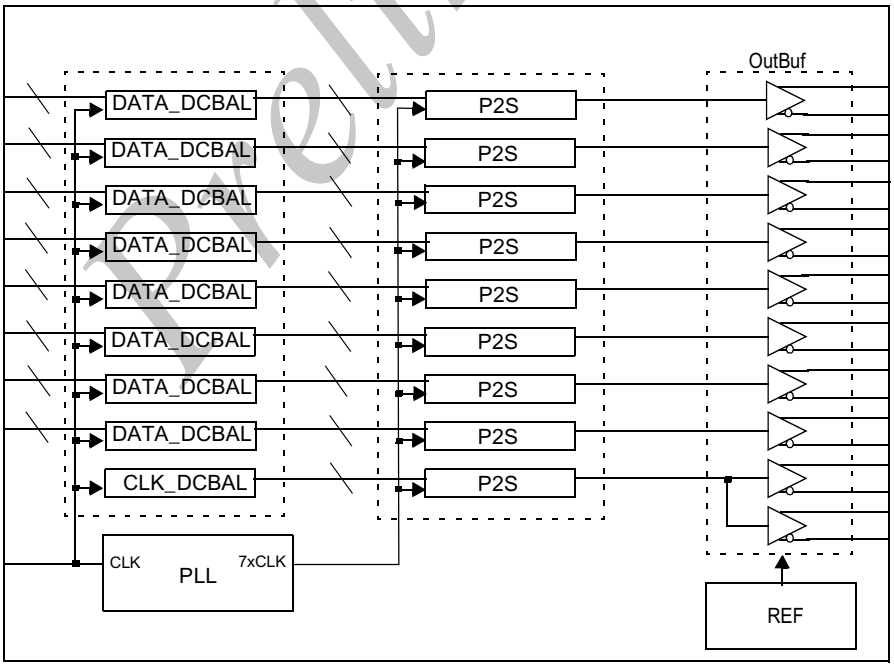
The CS5826 provides 3 operating modes: Single-In-Single-Out, Dual-In-Dual-Out and Single-In-Dual-Out. In Single-In-Single-Out and Dual-In-Dual-Out modes, single pixel data can be clocked into CS5826 at a maximum rate of 112MHz. In Single-In-Dual-Out mode, CS5826 supports a maximum clock rate of 224MHz.

DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable.

FEATURES

- Complies with OpenLDI specification for digital display interface.
- 30 to 112 (224)MHz clock support.
- Supports SVGA through QXGA panel resolutions.
- Drives long, low cost cables.
- DC balance data transmission to reduce ISI distortion.
- Supports single and dual pixel GUI interface
- Rejects cycle-to-cycle jitter.
- 5V tolerant on data and control input pins.
- Programmable data and control strobe select (rising or falling edge strobe)
- Support for two additional user-defined control signals in DC balanced mode
- Compatible with TIA/EIA LVDS standard.
- 100-pin LQFP.

BLOCK DIAGRAM



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