Am29423

10K-ECL 32-Bit Parallel Multiplier

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- **32-Bit Three-Bus Architecture**
  - The device has two 32-bit input ports and one 32-bit output port with maximum multiply time of 48 ns
- **Single Clock with Register Enables**
  - The Am29423 is controlled by one clock with individual register enables
- **Supports Multiprecision Multiplication**
  - The device has dual 32-bit registers on each data input port to perform multiprecision multiplication
- **Registers can be made transparent**
  - Input and output registers can be made transparent independently to eliminate unwanted pipeline delay
- **Supports Two's Complement, Unsigned or Mixed Numbers**
- **Data Integrity Through Master-Slave Mode and Parity Check/Generate**
  - Parity check/generate catches inter-device connection errors and master/slave mode provides complete function check

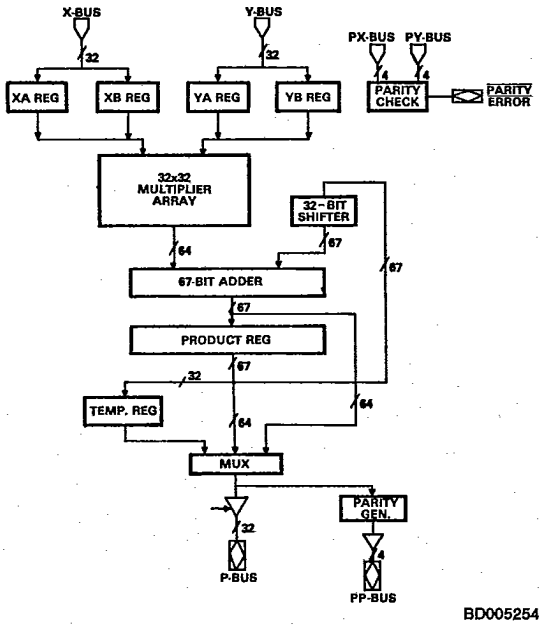
GENERAL DESCRIPTION

The Am29423 is a high-speed 32 x 32-Bit 10K-ECL Parallel Multiplier with 67-Bit Accumulator. The part is designed to maximize system level performance by providing a 32-bit three bus architecture and a single clock with register enables.

The Am29423 further enhances system throughput by providing individual register feedthrough controls, byte parity checking on both input ports and generation on the output port, and dual input registers on each data input bus to support multiprecision multiplication. The Am29423 can manage a wide variety of data types, including two's complement, unsigned, or mixed mode input formats. A 64 x 64-bit multiplication can be performed in seven clock cycles, including input and output. Additional features provided are a format adjust control allowing for standard output or left shifted output suitable for fractional two's complement arithmetic, rounding, and master/slave operation.

The Am29423 is designed with the IMOX* process, which allows internal ECL circuits with 10K-ECL-compatible I/O. The device is housed in a 169-lead pin-grid-array package.

SIMPLIFIED BLOCK DIAGRAM



BD005254

IMOX is a trademark of Advanced Micro Devices, Inc.

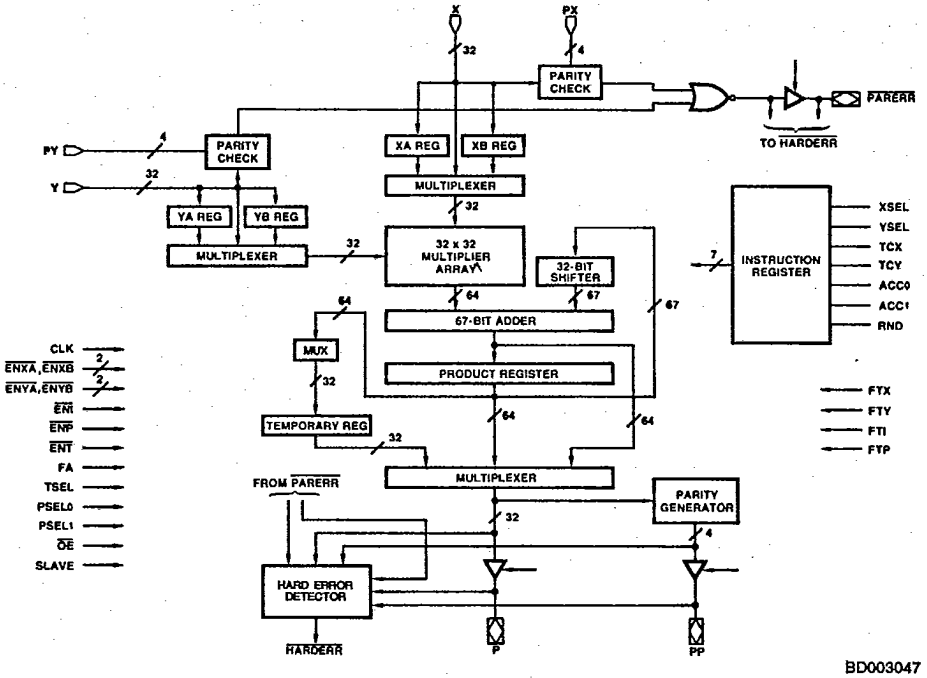
Publication # 07941 | Rev. A | Amendment /0
Issue Date: February 1987

RELATED AMD PRODUCTS

Part No.	Description
AmPAL10H20EG8	10K-ECL PAL* with Output Logic Macrocells (Latches)
AmPAL10H20EV8	10K-ECL PAL with Output Logic Macrocells (Registers)
Am10415	10K Series — 1K x 1 ECL RAM
Am10P44	4K x 4 Generic Series 10K-ECL PROM
Am10470	10K Series — 4K x 1 ECL RAM
Am10474	10K Series — 1K x 4 ECL RAM
Am10480	10K Series — 16K x 1 ECL RAM
Am10484	10K Series — 4K x 4 ECL RAM
Am1850	Mixed ECL/TTL I/O Bipolar Mask-Programmable Gate Array (1800 Gates)
Am29434	ECL 4-Port Dual Access Register File
Am3500	Mask-Programmable ECL Gate Array (5000 Gates)
Am3525	Mask-Programmable ECL Gate Array with 1152-Bit ECL RAM (3750 Gates)
Am3550	Mixed ECL/TTL I/O Bipolar Mask-Programmable Gate Array (5200 Gates)

*PAL is a registered trademark of and is used under license from Monolithic Memories, Inc.

DETAILED BLOCK DIAGRAM



BD003047

CONNECTION DIAGRAM
Bottom View
PGA

T-45-07

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	PY3	Y31	Y30	Y26	Y24	Y23	Y20	Y19	Y15	Y10	Y11	Y07	Y05	Y03	NC	$\overline{ENYA}$	PX3
2	NC	NC	Y29	Y27	PY2	Y21	Y18	Y16	PY1	Y12	Y09	PY0	Y04	Y02	Y0	$\overline{ENYB}$	X31
3	NC	$\overline{PPERR}$	NC	Y28	Y25	Y22	VCC	Y17	Y14	Y13	VEE	Y08	Y06	Y01	FTY	X30	NC
4	VCC0	PP3	NC	NC*											X29	X28	X27
5	P30	P31	P29												X26	X24	X25
6	VCC0	P28	P27												PX2	X23	X22
7	P25	P26	VEE												VCC	X19	X21
8	VCC0	P24	PP2												X18	X17	X20
9	NC	NC	P23												X15	X16	PX1
10	VCC0	P22	P21												X14	X13	X11
11	P19	P20	VCC												VEE	X10	X12
12	P16	P18	P17												X09	X08	PX0
13	VCC0	$\overline{HDERR}$	FTP												X07	X05	X06
14	NC	$\overline{ENP}$	NC												X02	X03	X04
15	$\overline{ENT}$	$\overline{OE}$	SLAVE	P15	P11	P12	VEE	P07	P06	P03	VCC	P01	FTI	TCY	FTX	X01	X0
16	PSEL1	FA	PP1	P14	P13	P09	VEE	PP0	P05	P04	VCC	$\overline{ENI}$	CLK	ACC1	TCX	$\overline{ENXB}$	$\overline{ENXA}$
17	PSEL0	TSEL	VCC0	VCC0	VCC0	P10	VEE	P08	VCC0	P02	VCC	P0	VCC0	RND	ACC0	YSEL	XSEL

CD010451

Key: NC = No Connection
$\overline{PPERR}$ = $\overline{PARERR}$
$\overline{HDERR}$ = $\overline{HARDERR}$
*Reference pin for package orientation (pin #D-4)

PIN DESIGNATIONS

T-45-07

(Sorted by Pin No.)

PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.
A-1	PY_3	1	C-9	P_{23}	75	J-15	P_6	55	R-10	X_{14}	117
A-2	NC	168	C-10	P_{21}	72	J-16	P_5	51	R-11	V_{EE}	116
A-3	NC	83	C-11	V_{CC}	74	J-17	V_{CC0}	135	R-12	X_9	36
A-4	V_{CC0}	81	C-12	P_{17}	153	K-1	Y_{10}	14	R-13	X_7	121
A-5	P_{30}	80	C-13	FTP	151	K-2	Y_{12}	13	R-14	X_2	40
A-6	V_{CC0}	79	C-14	NC	66	K-3	Y_{13}	96	R-15	FTX	125
A-7	P_{25}	160	C-15	SLAVE	146	K-15	P_3	50	R-16	TCX	128
A-8	V_{CC0}	77	C-16	PP_1	145	K-16	P_4	134	R-17	ACC0	45
A-9	NC	157	C-17	V_{CC0}	61	K-17	P_2	133	T-1	$\overline{ENYA}$	105
A-10	V_{CC0}	71	D-1	Y_{26}	4	L-1	Y_{11}	97	T-2	$\overline{ENYB}$	21
A-11	P_{19}	154	D-2	Y_{27}	87	L-2	Y_9	98	T-3	X_{30}	107
A-12	P_{16}	69	D-3	Y_{28}	3	L-3	V_{EE}	95	T-4	X_{28}	108
A-13	V_{CC0}	68	D-15	P_{15}	62	L-15	V_{CC}	53	T-5	X_{24}	110
A-14	NC	67	D-16	P_{14}	144	L-16	V_{CC}	53	T-6	X_{23}	111
A-15	$\overline{ENT}$	65	D-17	V_{CC0}	60	L-17	V_{CC}	53	T-7	X_{19}	113
A-16	PSEL1	148	E-1	Y_{24}	5	M-1	Y_7	16	T-8	X_{17}	114
A-17	PSEL0	64	E-2	PY_2	89	M-2	PY_0	99	T-9	X_{16}	31
B-1	Y_{31}	85	E-3	Y_{25}	88	M-3	Y_8	15	T-10	X_{13}	34
B-2	NC	84	E-15	P_{11}	142	M-15	P_1	132	T-11	X_{10}	119
B-3	$\overline{PARERR}$	166	E-16	P_{13}	143	M-16	$\overline{ENI}$	47	T-12	X_8	120
B-4	PP_3	165	E-17	V_{CC0}	57	M-17	P_0	48	T-13	X_5	122
B-5	P_{31}	164	F-1	Y_{23}	6	N-1	Y_5	17	T-14	X_3	123
B-6	P_{28}	162	F-2	Y_{21}	7	N-2	Y_4	101	T-15	X_1	124
B-7	P_{26}	161	F-3	Y_{22}	90	N-3	Y_6	100	T-16	$\overline{ENXB}$	42
B-8	P_{24}	76	F-15	P_{12}	59	N-15	FTI	130	T-17	YSEL	127
B-9	NC	73	F-16	P_9	141	N-16	CLK	131	U-1	PX_3	22
B-10	P_{22}	156	F-17	P_{10}	58	N-17	V_{CC0}	49	U-2	X_{31}	106
B-11	P_{20}	155	G-1	Y_{20}	91	P-1	Y_3	18	U-3	NC	23
B-12	P_{18}	70	G-2	Y_{18}	92	P-2	Y_2	102	U-4	X_{27}	25
B-13	$\overline{HARDERR}$	152	G-3	V_{CC}	11	P-3	Y_1	19	U-5	X_{25}	26
B-14	$\overline{ENP}$	150	G-15	V_{EE}	137	P-15	TCY	44	U-6	X_{22}	28
B-15	$\overline{OE}$	149	G-16	V_{EE}	137	P-16	ACC1	129	U-7	X_{21}	112
B-16	FA	63	G-17	V_{EE}	137	P-17	RND	46	U-8	X_{20}	29
B-17	TSEL	147	H-1	Y_{19}	8	R-1	NC	20	U-9	PX_1	115
C-1	Y_{30}	2	H-2	Y_{16}	93	R-2	Y_0	103	U-10	X_{11}	35
C-2	Y_{29}	86	H-3	Y_{17}	9	R-3	FTY	104	U-11	X_{12}	118
C-3	NC	167	H-15	P_7	139	R-4	X_{29}	24	U-12	PX_0	37
C-4	NC	82	H-16	PP_0	56	R-5	X_{26}	109	U-13	X_6	38
C-5	P_{29}	163	H-17	P_8	140	R-6	PX_2	27	U-14	X_4	39
C-6	P_{27}	78	J-1	Y_{15}	94	R-7	V_{CC}	32	U-15	X_0	41
C-7	V_{EE}	158	J-2	PY_1	10	R-8	X_{18}	30	U-16	$\overline{ENXA}$	126
C-8	PP_2	159	J-3	Y_{14}	12	R-9	X_{15}	33	U-17	XSEL	43

PIN DESIGNATIONS

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(Sorted by Pin Name)

PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.	PIN NAME	PIN NO.	PAD NO.
ACC0	R-17	45	P_{14}	D-16	144	V_{CC}	L-17	53	X_{24}	T-5	110
ACC1	P-16	129	P_{15}	D-15	62	V_{CC}	R-7	32	X_{25}	U-5	26
CLK	N-16	131	P_{16}	A-12	69	V_{CC0}	A-4	81	X_{26}	R-5	109
$\overline{ENI}$	M-16	47	P_{17}	C-12	153	V_{CC0}	A-6	79	X_{27}	U-4	25
$\overline{ENP}$	B-14	150	P_{18}	B-12	70	V_{CC0}	A-8	77	X_{28}	T-4	108
$\overline{ENT}$	A-15	65	P_{19}	A-11	154	V_{CC0}	A-10	71	X_{29}	R-4	24
$\overline{ENXA}$	U-16	126	P_{20}	B-11	155	V_{CC0}	A-13	68	X_{30}	T-3	107
$\overline{ENXB}$	T-16	42	P_{21}	C-10	72	V_{CC0}	C-17	61	X_{31}	U-2	106
$\overline{ENYA}$	T-1	105	P_{22}	B-10	156	V_{CC0}	D-17	60	XSEL	U-17	43
$\overline{ENYB}$	T-2	21	P_{23}	C-9	75	V_{CC0}	E-17	57	Y_0	R-2	103
FA	B-16	63	P_{24}	B-8	76	V_{CC0}	J-17	135	Y_1	P-3	19
FTI	N-15	130	P_{25}	A-7	160	V_{CC0}	N-17	49	Y_2	P-2	102
FTP	C-13	151	P_{26}	B-7	161	V_{EE}	C-7	158	Y_3	P-1	18
FTX	R-15	125	P_{27}	C-6	78	V_{EE}	G-15	137	Y_4	N-2	101
FTY	R-3	104	P_{28}	B-6	162	V_{EE}	G-16	137	Y_5	N-1	17
$\overline{HARDERR}$	B-13	152	P_{29}	C-5	163	V_{EE}	G-17	137	Y_6	N-3	100
NC	A-2	168	P_{30}	A-5	80	V_{EE}	L-3	95	Y_7	M-1	16
NC	A-3	83	P_{31}	B-5	164	V_{EE}	R-11	116	Y_8	M-3	15
NC	A-9	157	$\overline{PARERR}$	B-3	166	X_0	U-15	41	Y_9	L-2	98
NC	A-14	67	PP_0	H-16	56	X_1	T-15	124	Y_{10}	K-1	14
NC	B-2	84	PP_1	C-16	145	X_2	R-14	40	Y_{11}	L-1	97
NC	B-9	73	PP_2	C-8	159	X_3	T-14	123	Y_{12}	K-2	13
NC	C-3	167	PP_3	B-4	165	X_4	U-14	39	Y_{13}	K-3	96
NC	C-4	82	PSEL0	A-17	64	X_5	T-13	122	Y_{14}	J-3	12
NC	C-14	66	PSEL1	A-16	148	X_6	U-13	38	Y_{15}	J-1	94
NC	R-1	20	PX_0	U-12	37	X_7	R-13	121	Y_{16}	H-2	93
NC	U-3	23	PX_1	U-9	115	X_8	T-12	120	Y_{17}	H-3	9
$\overline{OE}$	B-15	149	PX_2	R-6	27	X_9	R-12	36	Y_{18}	G-2	92
P_0	M-17	48	PX_3	U-1	22	X_{10}	T-11	119	Y_{19}	H-1	8
P_1	M-15	132	PY_0	M-2	99	X_{11}	U-10	35	Y_{20}	G-1	91
P_2	K-17	133	PY_1	J-2	10	X_{12}	U-11	118	Y_{21}	F-2	7
P_3	K-15	50	PY_2	E-2	89	X_{13}	T-10	34	Y_{22}	F-3	90
P_4	K-16	134	PY_3	A-1	1	X_{14}	R-10	117	Y_{23}	F-1	6
P_5	J-16	51	RND	P-17	46	X_{15}	R-9	33	Y_{24}	E-1	5
P_6	J-15	55	SLAVE	C-15	146	X_{16}	T-9	31	Y_{25}	E-3	88
P_7	H-15	139	TCX	R-16	128	X_{17}	T-8	114	Y_{26}	D-1	4
P_8	H-17	140	TCY	P-15	44	X_{18}	R-8	30	Y_{27}	D-2	87
P_9	F-16	141	TSEL	B-17	147	X_{19}	T-7	113	Y_{28}	D-3	3
P_{10}	F-17	58	V_{CC}	C-11	74	X_{20}	U-8	29	Y_{29}	C-2	86
P_{11}	E-15	142	V_{CC}	G-3	11	X_{21}	U-7	112	Y_{30}	C-1	2
P_{12}	F-15	59	V_{CC}	L-15	53	X_{22}	U-6	28	Y_{31}	B-1	85
P_{13}	E-16	143	V_{CC}	L-16	53	X_{23}	T-6	111	YSEL	T-17	127

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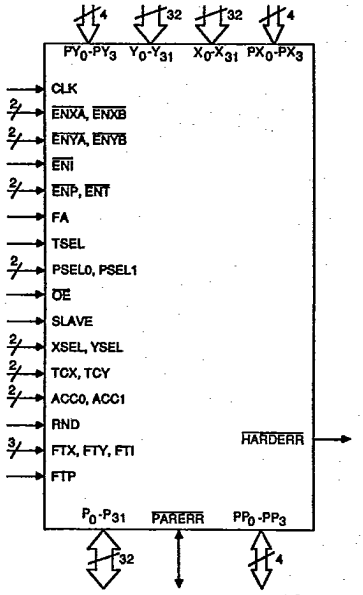
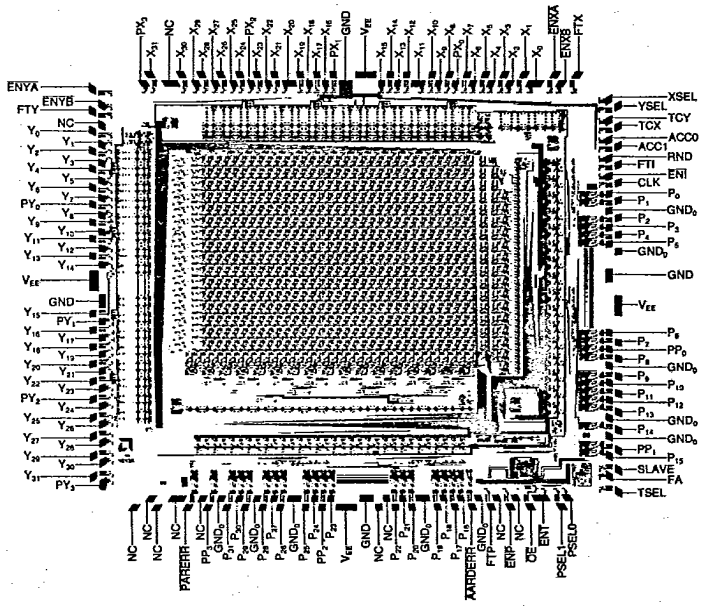
LOGIC SYMBOL



LS002900

METALLIZATION AND PAD LAYOUT



Die Size: 383 x 334 mils
Equivalent Gate Count: 6000 gates

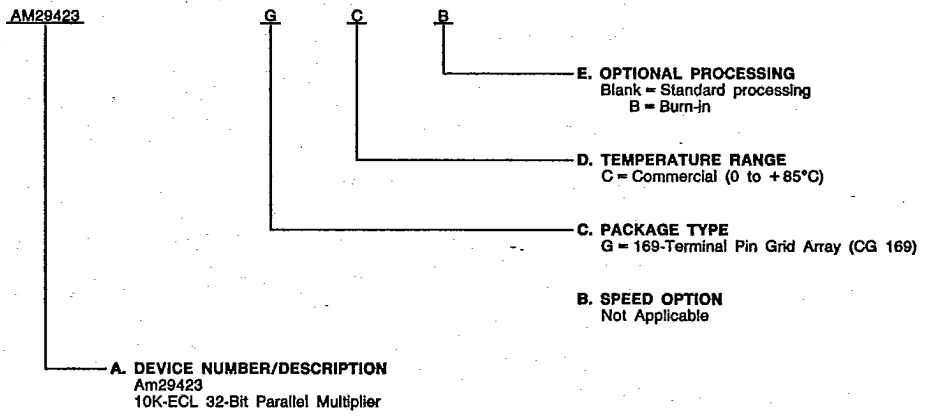
ORDERING INFORMATION

T-45-07

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM29423	GC, GCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

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ACC0, ACC1 Accumulator Control (Input)
Accumulator control lines used to determine accumulator function; PASS, ACCUMULATE, and SHIFT/ACCUMULATE.

CLK Clock (Input)
Clock input for all registers.

$\overline{ENI}$ Instruction Register Enable (Input; Active LOW)
Register enables for instruction register I.

$\overline{ENP}$ Accumulator Register Enable (Input; Active LOW)
Register enable for product register P.

$\overline{ENT}$ Temporary Register Enable (Input; Active LOW)
Register enable for temporary register T.

$\overline{ENXA}$, $\overline{ENXB}$ Multiplicand Register Enable (Input; Active LOW)
Register enables for multiplicand data input registers XA and XB.

$\overline{ENYA}$, $\overline{ENYB}$ Multiplier Register Enable (Input; Active LOW)
Register enables for multiplier data input registers YA and YB.

FA Format Adjust (Input)
Format adjust selects either a full 64-bit product (HIGH) or a left-shifted 63-bit product suitable for fractional two's complement arithmetic (LOW).

FTP Feedthrough Control (Input; Active HIGH)
Feedthrough control for product register.

FTX, FTY, FTI Feedthrough Control (Input; Active HIGH)
Feedthrough control lines for X, Y, and I registers.

$\overline{HARDERR}$ Hard Error Flag (Output; Active LOW)
Used when two Am29423s are configured as master and slave to indicate hardware errors.

$\overline{OE}$ Output Enable Control (Input; Active LOW)
Used to enable (LOW) or disable (HIGH) the P output port.

$P_0 - P_{31}$ Product Output (Input/Output)
Product output for P port.

$\overline{PARERR}$ Parity Error Flag (Input/Output, Active LOW)
Indicates a parity error on the input buses.

$PP_0 - PP_3$ Byte Parity (Input/Output)
Byte parity outputs on P output port (odd parity).

PSEL0, PSEL1 Product Control (Input)
Used to select desired output including disabling P and PP output ports.

$PX_0 - PX_3$ Byte Parity (Input)
Byte parity inputs on X input port (odd parity).

$PY_0 - PY_3$ Byte Parity (Input)
Byte parity inputs on Y input port (odd parity).

RND Round Control (Input; Active HIGH)
Round control for rounding the most significant product.

SLAVE $\overline{\text{Master}}$/Slave Control (Input)
Used to determine mode of operation.

TCX, TCY Mode Control (Input)
Mode control inputs for each input data word; LOW for unsigned data and HIGH for two's complement format.

TSEL Select Control (Input)
Used to route the most significant product register (HIGH) or the least significant product register (LOW) into the temporary register.

V_{CC} Internal Logic Ground
This is the most positive voltage in the internal logic. It is used as the reference level for internal logic.

V_{CCO} Output Drive Ground
This is the most positive voltage in the output buffer logic. It is used as the reference level for the buffer logic.

V_{EE} Power Supply Voltage
This is the most negative voltage. It provides power for internal and buffer logic.

$X_0 - X_{31}$ Multiplicand Data (Input)
Multiplicand data input for X port.

XSEL X Register Select (Input)
Control line used to route the contents of either the XA register (HIGH) or XB register (LOW) into the multiplier array.

$Y_0 - Y_{31}$ Multiplier Data (Input)
Multiplier data input for Y port.

YSEL Y Register Select (Input)
Control line used to route the contents of either the YA register (HIGH) or YB register (LOW) into the multiplier array.

FUNCTIONAL DESCRIPTION

Architecture

The Am29423 comprises a high-speed 32 by 32-bit multiplier array, a 67-bit accumulator, and a 32-bit data path.

Multiplier Array

The multiplier is a 32 by 32-bit array which produces a 64-bit product. This product is then fed to the accumulator section.

Accumulator

The accumulator is 67 bits wide. It performs accumulation for sum of product operations and multiprecision multiplication operations. The accumulator can perform three operations: store product without accumulation, accumulate product, and shift accumulator value and accumulate with product.

The shift and accumulate shifts the value in the product register 32 bits to the right (effectively move the most significant 32 bits to the least significant 32 bits) and sign extends to a full 64 bits. This shifted value is then accumulated with the output of the multiplier array. The 67-bit width is necessary to contain overflows in internal accumulations. These overflows are maintained and used when the product register is right shifted in the multiprecision multiplies. The lower 64 bits contain the 64-bit output while the upper 3 bits contain the overflow.

Data Path

The 32-bit data path consists of X and Y input buses; the P output bus; data registers XA, XB, YA, YB, and the product accumulator; two multiplier input multiplexers; byte parity input checkers; byte parity output generators; and master/slave comparators. Input operands enter the device through the two 32-bit input buses, $X_0 - X_{31}$ and $Y_0 - Y_{31}$. These operands may then be stored in one of the two registers for each bus (XA or XB for X, YA or YB for Y) or they may be fed directly through to the multiplier array. Input parity checking is performed as soon as the operands are put on the input buses. The signals used for output parity generation are taken from

the input side of the output buffer. In case of parity error, $\overline{PARERR}$ is enabled LOW.

Operational Modes

The Am29423 can perform signed, unsigned, or mixed mode multiplication. These different numerical representations are controlled by TCX and TCY. A HIGH input on one of these lines indicates to the device that the respective input should be treated as a two's complement number; a LOW, an unsigned number. The output format is unsigned when both inputs are unsigned. The output format is two's complement when either or both inputs are two's complement.

Slave Mode

Each output has an associated comparator which compares the signal on the output pin with the signal provided to the output driver. If any of these outputs do not agree, the $\overline{HARDERR}$ is asserted. When not in slave mode, this enables the multiplier to check for contention and bus shorts. However, when in slave mode, one multiplier can be used to detect faults in both internal functions and interconnections of the other multiplier. This is accomplished through the master/slave configuration, where the two multipliers operate in parallel. One multiplier is the master and operates normally; the other operates in slave mode.

In slave mode all outputs are turned into inputs from the master, except for the $\overline{HARDERR}$ signal. Since the slave is operated in parallel with the master, it can compare the results it generates to those of the master and signal an error if they differ.

Command Description and Formats

The accumulator is controlled by ACC0 and ACC1. These lines are used to select any of the three operations that the accumulator can perform. This instruction set is described in Table 1.

The temporary output register is controlled by TSEL and FA. These lines are used to select any of the four different sets of data that can be stored in the temporary register. This instruction set is described in Table 2.

The output multiplexer is controlled by PSEL0, PSEL1, and FA. These lines are used to select any of the five different sets of data that can be output through the P port. PSEL0 and PSEL1 can also be used to disable the outputs. (This instruction is independent of $\overline{OE}$.) This instruction set is described in Table 3.

Format Adjust (FA) is used to select either a full 64-bit product or a left-shifted 63-bit product suitable for fractional two's complement arithmetic. This shifting increases the precision of the upper half of the product word by eliminating the redundant sign bit. Output Data Formats show the effect of FA.

Round (RND) is used to round the upper 32 bits of the 64-bit product. If only the upper 32 bits of the product are being used, then the lower 32 bits are truncated when rounding is not used (RND = 0). If rounding is used (RND = 1), then a "1" is added to the most significant of the lower 32 bits. This results in a smaller possible error. This should only be used when the lower 32 bits are to be truncated.

User-Visible Register Descriptions

The Am29423 contains seven different register sets, each with its own clock enable. Two 32-bit registers are attached to each of the input data buses. These registers are differentiated by the suffix A or B. For example, the X bus has registers XA and XB. The 67-bit accumulator register can be used as a regular product register when the part is used as a multiplier only or as the register part of the accumulator section. The 32-bit temporary output register is included to aid in the pipelining of multiprecision operations. An instruction register is also provided.

All of these registers can be made transparent with the exception of the accumulator register and the temporary register. The product from the multiplier can be fed directly to the output by using the FTP control line.

TABLE 1. ACCUMULATOR OPERATION INSTRUCTIONS

ACC1	ACC0	Accumulator Operation
0	0	PASS
0	1	ACCUMULATE
1	0	INVALID
1	1	SHIFT AND ACCUMULATE

TABLE 2. INPUT SELECT INSTRUCTIONS FOR TEMPORARY (T) REGISTER

TSEL	FA	Temp Reg Input
0	0	P_{i-1}
0	1	P_i
1	0	P_{i+31}
1	1	P_{i+32}

TABLE 3. OUTPUT SELECT INSTRUCTIONS FOR PRODUCT (P) PORT

PSEL1	PSEL0	FA	P Port Output
0	0	X	TEMP REGISTER
0	1	0	P_{i-1}
0	1	1	P_i
1	0	0	P_{i+31}
1	0	1	P_{i+32}
1	1	X	DISABLE

Am29423 X AND Y INPUT DATA FORMATS

T-45-07

Fractional Two's Complement

TCX, TCY = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}						2^{-28}	2^{-29}	2^{-30}	2^{-31}

Integer Two's Complement

TCX, TCY = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

Unsigned Fractional

TCX, TCY = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}						2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer

TCX, TCY = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

Am29423 P-PORT OUTPUT DATA FORMATS

T-45-07

Fractional Two's Complement (Shifted)*

FA = 0, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}						2^{-28}	2^{-29}	2^{-30}	2^{-31}

FA = 0, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-32}	2^{-33}	2^{-34}	2^{-35}	2^{-36}	2^{-37}						2^{-60}	2^{-61}	2^{-62}	2^{-63}**

Fractional Two's Complement

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}						2^{-27}	2^{-28}	2^{-29}	2^{-30}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-31}	2^{-32}	2^{-33}	2^{-34}	2^{-35}	2^{-36}						2^{-59}	2^{-60}	2^{-61}	2^{-62}

Integer Two's Complement

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
-2^{63}	2^{62}	2^{61}	2^{60}	2^{59}	2^{58}						2^{35}	2^{34}	2^{33}	2^{32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

Unsigned Fractional

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}						2^{-29}	2^{-30}	2^{-31}	2^{-32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{-33}	2^{-34}	2^{-35}	2^{-36}	2^{-37}	2^{-38}						2^{-61}	2^{-62}	2^{-63}	2^{-64}

Unsigned Integer

FA = 1, PSEL1 = 1, PSEL0 = 0

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{63}	2^{62}	2^{61}	2^{60}	2^{59}	2^{58}						2^{35}	2^{34}	2^{33}	2^{32}

FA = 1, PSEL1 = 0, PSEL0 = 1

31	30	29	28	27	26	–	–	–	–	–	3	2	1	0
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}						2^3	2^2	2^1	2^0

*In this format, an overflow occurs in the attempted multiplication of the two's complement number −1.000 with itself, yielding a product of +1.000 which cannot be represented in this format.
**This bit position (2^{-63}) equals zero in this format.

64 x 64 Multiplication

To perform a 64 x 64-bit multiplication using the Am29423, each 64-bit input must be split into two 32-bit inputs; a most significant half and a least significant half (XW1 and XW0 or YW1 and YW0, respectively). These 32-bit inputs are then used to perform the four multiplications needed to obtain the 128-bit product. This product is represented in four 32-bit words, $PW_3 - PW_0$. The least significant word being PW_0. The product is output 32 bits at a time through the product (P) port. The following equation shows the required multiplications:

$$X * Y = ((XW1 * YW1) * 2^{64}) + ((XW0 * YW1) * 2^{32}) + ((XW1 * YW0) * 2^{32}) + ((XW0 * YW0) * 2^{0})$$

$$P = (PW3 * 2^{96}) + (PW2 * 2^{64}) + (PW1 * 2^{32}) + (PW0 * 2^{0})$$

The Am29423 uses an internal accumulator to sum these intermediate products. The previous equation, in a slightly different form, is shown with the necessary instructions as follows:

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```
X →          .   XW1   XW0
Y →          *   YW1   YW0
-------------------------------------------
                 XW0 * YW0   ← Multiply only
           XW1 * YW0         ← Mult & Shift/Acc
           XW0 * YW1         ← Mult & Accumulate
     XW1 * YW1               ← Mult & Shift/Acc
-------------------------------------------
P →  PW3  PW2  PW1  PW0
```

Table 4 details the movement of the input operands through the Am29423. Table 5 defines the microcode required to perform a signed 64 x 64-bit multiplication. For an unsigned multiplication, TCX and TCY are LOW for all cycles. The operations and data movement are scheduled to produce a single product in seven clock cycles or a new pipelined product every four clock cycles.

TABLE 4. BUS AND REGISTER CONTENTS FOR A 64 x 64-BIT SIGNED MULTIPLICATION WITH ONE COMPLETE EXTENDED MULTIPLICATION SHOWN IN THE UNSHADED CYCLES

Cycle	0	1	2	3	4	5	6
X BUS	XW0	XW1			XW0	XW1	
XA REG	XW0	XW0	XW0	XW0	XW0	XW0	XW0
XB REG	XW1	XW1	XW1	XW1	XW1	XW1	XW1
Y BUS	YW0	YW1			YW0	YW1	
YA REG	YW0	YW0	YW0	YW0	YW0	YW0	YW0
YB REG	YW1	YW1	YW1	YW1	YW1	YW1	YW1
MPY OP	XW1*YW1	XW0*YW0	XW1*YW0	XW0*YW1	XW1*YW1	XW0*YW0	XW1*YW0
ACC OP	S/A	PASS	S/A	ACC	S/A	PASS	S/A
T REG		PW3	PW0			PW3	PW0
P BUS	PW1	PW2	PW3	PW0	PW1	PW2	PW3

Note: MPY OP = Operation of multiplier array (X*Y)
ACC OP = Operation of internal accumulator
PASS = Pass through multiplier product
ACC = Add previous result to current product
S/A = Shift previous result then add to current product

TABLE 5. INSTRUCTION MICROCODE FOR 64 x 64-BIT SIGNED MULTIPLICATION WITH ONE COMPLETE EXTENDED MULTIPLICATION SHOWN IN THE UNSHADED CYCLES

Cycle	0	1	2	3	4	5	6	7	8	9	A	B	C	D
$\overline{ENXA}$	0	1	1	1	0	1	1	1	0	1	1	1	0	1
$\overline{ENXB}$	1	0	1	1	1	0	1	1	1	0	1	1	1	0
TCX	0	1	0	1	0	1	0	1	0	1	0	1	0	1
XSEL	1	0	1	0	1	0	1	0	1	0	1	0	1	0
$\overline{ENYA}$	0	1	1	1	0	1	1	1	0	1	1	1	0	1
$\overline{ENYB}$	1	0	1	1	1	0	1	1	1	0	1	1	1	0
TCY	0	0	1	1	0	0	1	1	0	0	1	1	0	0
YSEL	1	1	0	0	1	1	0	0	1	1	0	0	1	1
$\overline{ENI}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{ENT}$	1	0	0	1	1	0	0	1	1	0	0	1	1	0
TSEL	X	1	0	X	X	1	0	X	X	1	0	X	X	1
ACC0	0	1	1	1	0	1	1	1	0	1	1	1	0	1
ACC1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
$\overline{ENP}$	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PSEL0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
PSEL1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with
Power Applied ..... −55 to +125°C
V_{EE} Pin Potential to GND Pin ..... −7.0 V to +0.5 V
Input Voltage (DC) ..... V_{EE} to +0.5 V
Output Current (DC Output HIGH) .... −30 mA to +0.1 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +85°C
Supply Voltage ..... −5.46 V to −4.94 V
Air Velocity ..... 200 linear feet per minute

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS (Commercial) (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Min. (Note 2)	Max. (Note 2)	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ Max. or V_{IL} Min.	$T_C = 0°C$	−1000	−840	mV
			$T_C = +25°C$	−960	−810	
			$T_C = +85°C$	−900	−720	
V_{OL}	Output Voltage LOW		$T_C = 0°C$	−1870	−1665	mV
			$T_C = +25°C$	−1850	−1650	
			$T_C = +85°C$	−1830	−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IH}$ Min. or V_{IL} Max.	$T_C = 0°C$	−1020		mV
			$T_C = +25°C$	−980		
			$T_C = +85°C$	−920		
V_{OLC}	Output Voltage LOW		$T_C = 0°C$		−1645	mV
			$T_C = +25°C$		−1630	
			$T_C = +85°C$		−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs	$T_C = =0°C$	−1145	−840	mV
			$T_C = +25°C$	−1105	−810	
			$T_C = +85°C$	−1045	−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs	$T_C = =0°C$	−1870	−1490	mV
			$T_C = +25°C$	−1850	−1475	
			$T_C = +85°C$	−1830	−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH}$ Max.	$T_C = 0$ to +85°C		220	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{IL}$ Min.	$T_C = 25°C$		140	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open	$T_C = 0°C$		1600	mA
			$T_C = +85°C$		1400	

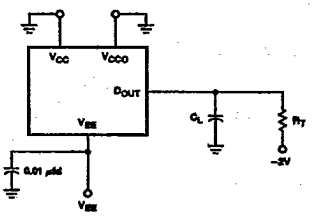
Notes: 1. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical thermal resistance values of the package are:
θ_{JA} (Junction-to-Ambient) = 22°C/Watt (still air)
θ_{JA} (Junction-to-Ambient) = 7.5°C/Watt (at 200 F.P.M. air flow)
θ_{JC} (Junction-to-Case) = 5°C/Watt
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
Unclocked Mode						
1	t_{MUC}	Unclocked Multiply Time X_0-X_{31}, Y_0-Y_{31}, to P_0-P_{31}	FTX/Y/P = HIGH		48	ns
2	t_{MUCPP}	Unclocked Multiply Time X_0-X_{31}, Y_0-Y_{31} to PP_0-PP_3	FTX/Y/P = HIGH			ns
3	t_{IP}	Instruction to P_0-P_{31} (Note 1)	Output Taken From Adder FTI = HIGH			ns
4	t_{IPP}	Instruction to PP_0-PP_3	Output Taken From Adder FTI = HIGH			ns
Clocked Mode						
5	t_{MC}	Clocked Multiply Time	FTX/Y/P = LOW		40	ns
6	t_{PDP}	Clock to P_0-P_{31}	Output Taken from Temp or Product Reg.		6	ns
7	t_{PDPP}	Clock to PP_0-PP_3	Output Taken from Temp or Product Reg.			ns
8	t_{PAP}	Clock to P_0-P_{31}	Output Taken from Adder, FTX/Y/I = LOW			ns
9	t_{PAPP}	Clock to PP_0-PP_3	Output Taken from Adder, FTX/Y/I = LOW			ns
10	t_{SP}	Data to Product Register Setup Time	FTX/Y = HIGH			ns
11	t_{HP}	Data to Product Register Hold Time	FTX/Y = HIGH			ns
12	t_{SIPT}	Instruction to Product Reg. Setup Time (Note 1)	FTI = HIGH			ns
13	t_{HIPT}	Instruction to Product Reg. Hold Time (Note 1)	FTI = HIGH			ns
14	t_{PWH}	Clock Pulse Width HIGH		10		ns
15	t_{PWL}	Clock Pulse Width LOW		10		ns
Setup and Hold Times						
16	t_{SXY}	Register XA, XB, YA, YB Setup Time		6		ns
17	t_{HXY}	Register XA, XB, YA, YB Hold Time		0		ns
18	t_{SI}	Instruction Register Setup Time (Note 1)		6		ns
19	t_{HI}	Instruction Register Hold Time (Note 1)		0		ns
20	t_{SEN}	Register Enable Setup Time		6		ns
21	t_{HEN}	Register Enable Hold Time		0		ns
22	t_{STS}	TSEL Setup Time		6		ns
23	t_{HTS}	TSEL Hold Time		0		ns
Common Parameters						
24	t_{PP}	PSEL0 - PSEL1 to P_0-P_{31} (Note 2)	To Active State Only			ns
25	t_{PPP}	PSEL0 - PSEL1 to PP_0-PP_3 (Note 2)	To Active State Only			ns
26	t_{OEP1}	$\overline{OE}$ to P_0-P_{31}, PP_0-PP_3 Output Enable			8	ns
27	t_{OD}	$\overline{OE}$ or PSEL0 - PSEL1 to P_0-P_{31}, PP_0-PP_3 Output Disable			8	ns
28	t_{DPE}	Data to $\overline{PARERR}$			11	ns
29	t_{DHE}	Data to $\overline{HARDERR}$	Slave = HIGH		10	ns

Notes: 1. Instruction signals are XSEL, YSEL, TCX, TCY, ACC0, ACC1, and RND.
2. This specification applies only to transitions between active states; i.e., states for which the output is not disabled. In order for this specification to apply, only one of the two PSEL signals can be changed at any given time. For example, this specification will apply for a transition between PSEL1 = H, PSEL0 = L and PSEL1 = L, PSEL0 = L, but not for a transition between PSEL1 = H, PSEL1 = L and PSEL1 = L, PSEL0 = H.

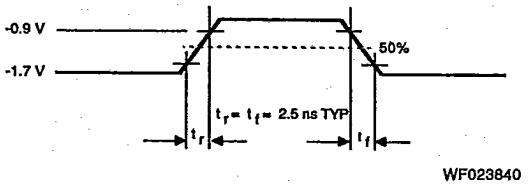
SWITCHING TEST CIRCUIT



TC000233

R_T = 50 Ω termination of measurement system
C_L = 30 pF (including stray jig capacitance)

SWITCHING TEST WAVEFORM (Note 4)



WF023840

All propagation delays relative to 50% point

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

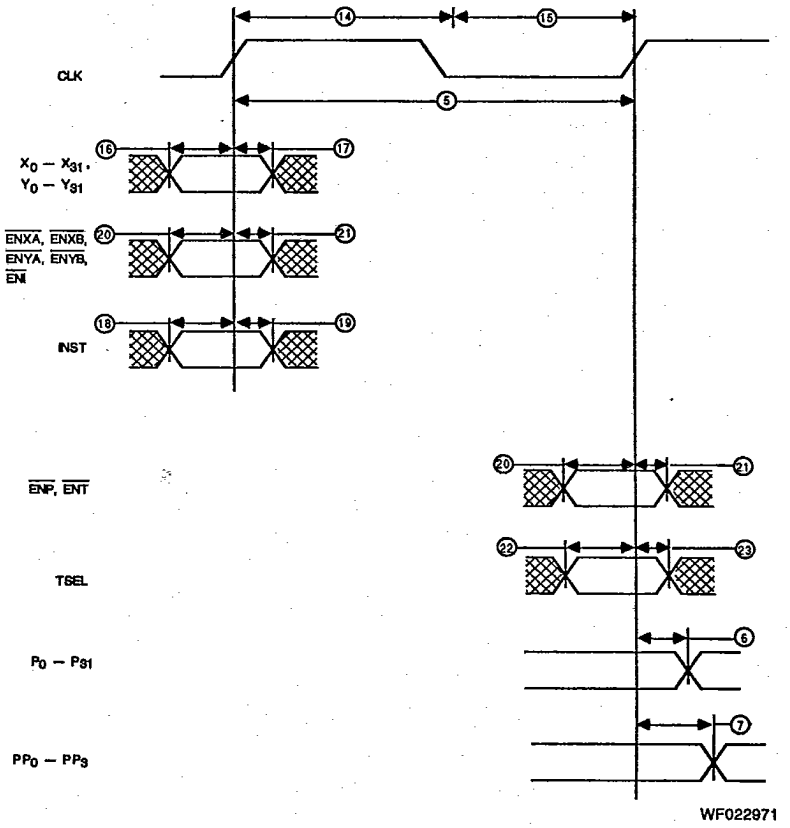
1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} and V_{EE} current when the device switches may cause erroneous function failures due to V_{CC} and V_{EE} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, V_{EE} current may change by as much as 50 mA in 5-8 ns. Inductance in the V_{EE} cable may allow the ground pins at the device to rise by 10s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using solid V_{IL} and V_{IH} levels.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Genrad-16 programs, under license.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

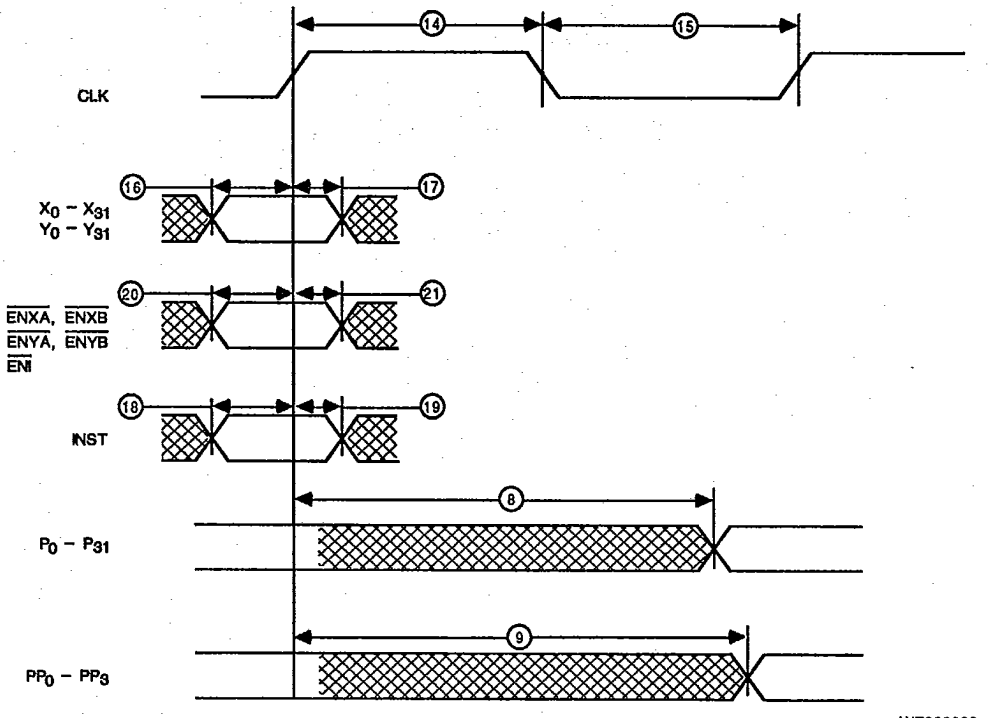


WF022971

Clocked Operation: FTX, Y, P, I = LOW

SWITCHING WAVEFORMS (Cont'd.)

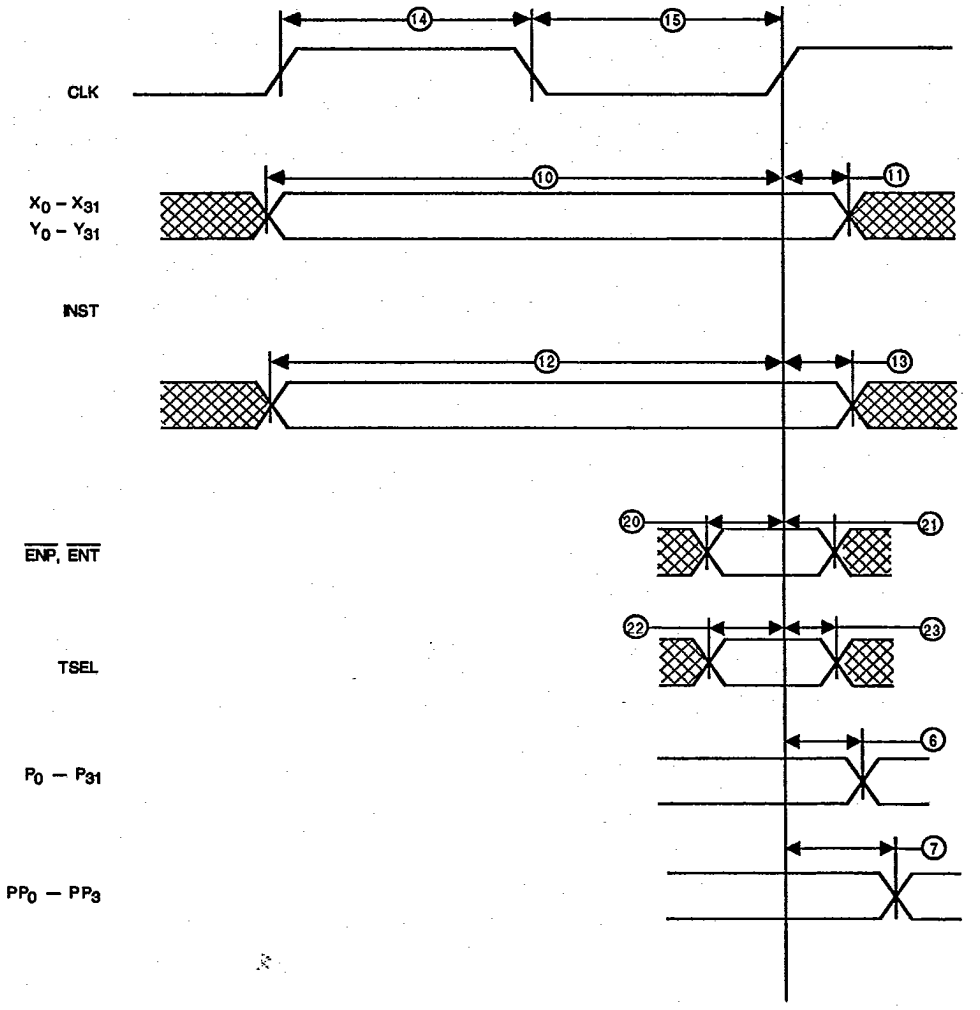
T-45-07



Clocked Operation: Output Taken from Adder
(FTX, Y, I = LOW; FTP = HIGH; PSEL1 ≠ PSEL0)

SWITCHING WAVEFORMS (Cont'd.)

T-45-07

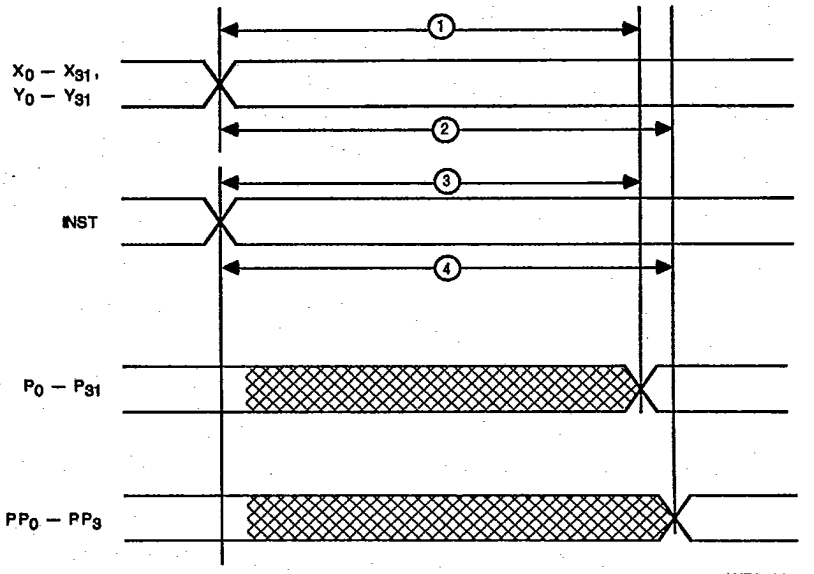


WF022982

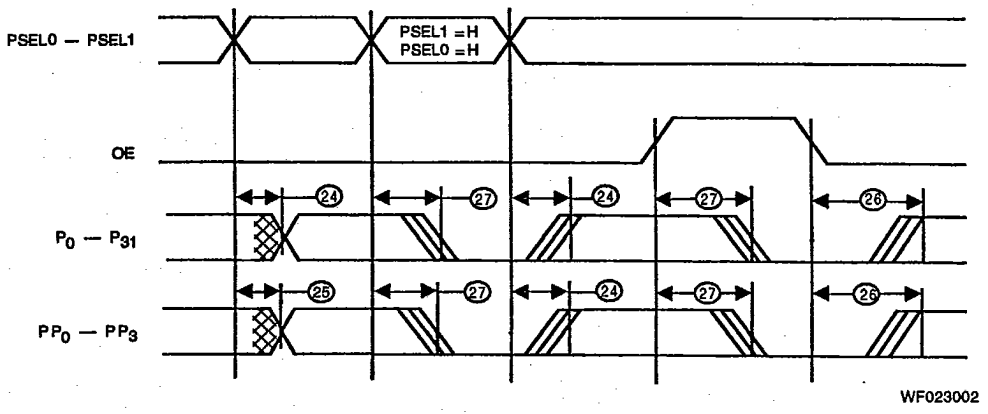
Clocked Operation: Input Registers Bypassed (FTX, Y, I = HIGH; FTP = LOW)

SWITCHING WAVEFORMS (Cont'd.)

T-45-07



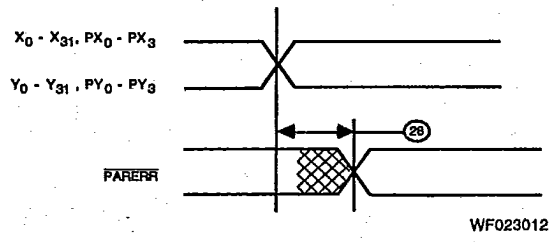
Unclocked Mode: FTX, Y, I, P = HIGH



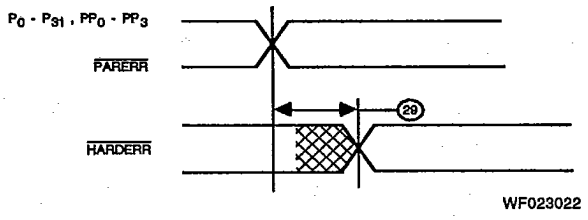
Output Select Timing

SWITCHING WAVEFORMS (Cont'd.)

T-45-07



$\overline{\text{PARERR}}$ Timing

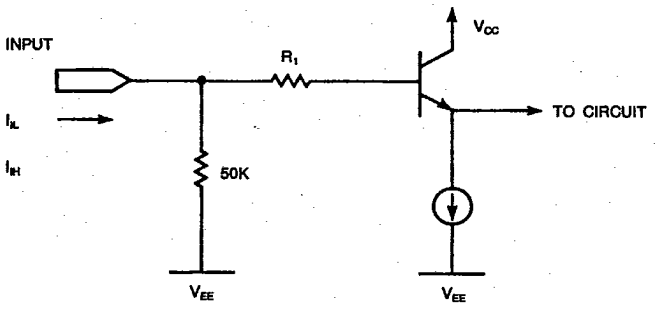


Slave Mode Timing

INPUT/OUTPUT CIRCUIT DIAGRAM

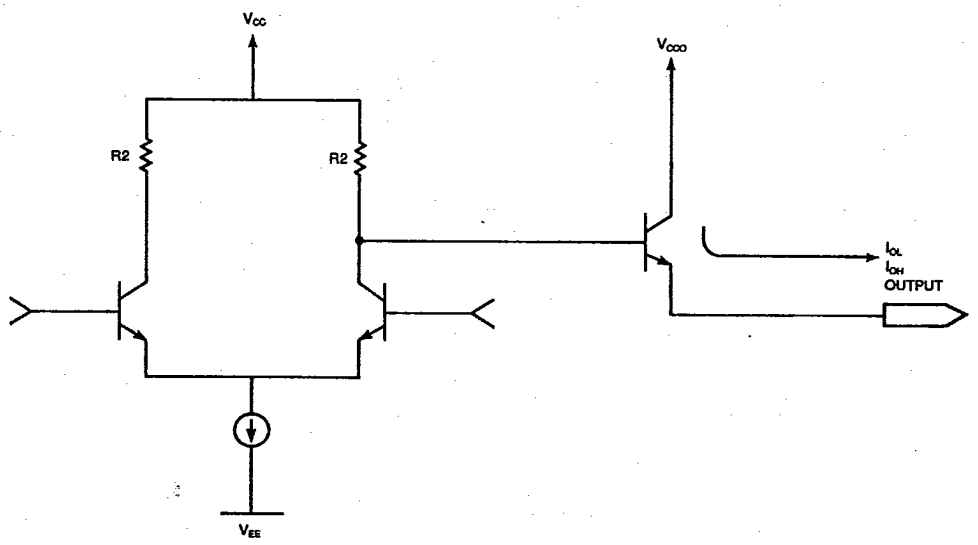
T-45-07

Input Circuit



IC000922

Output Circuit

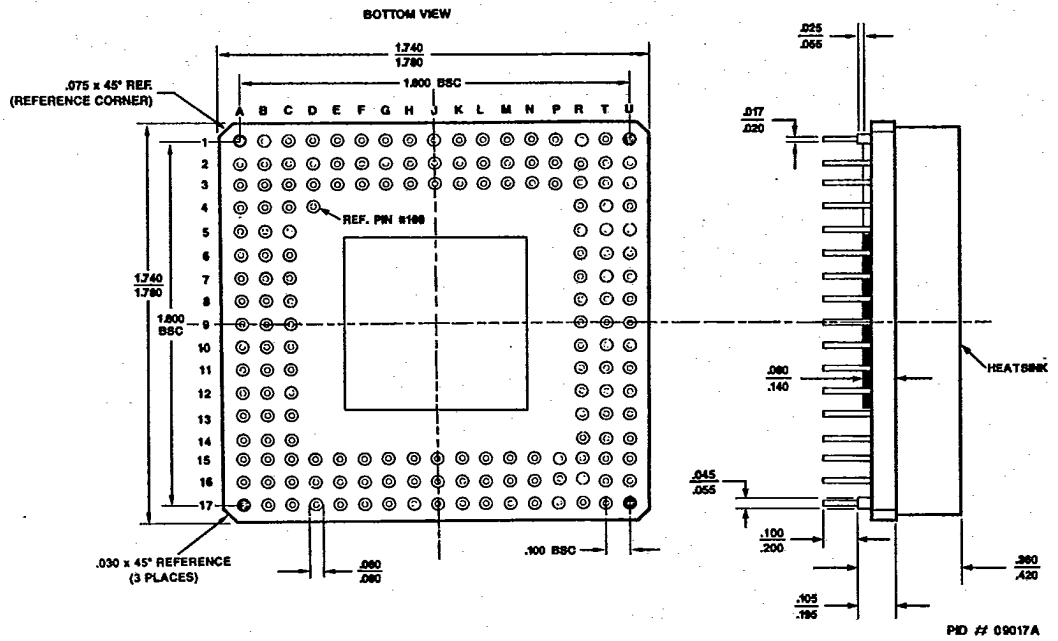


IC000931

PHYSICAL DIMENSIONS*

T-45-07

CG 169



*For reference only