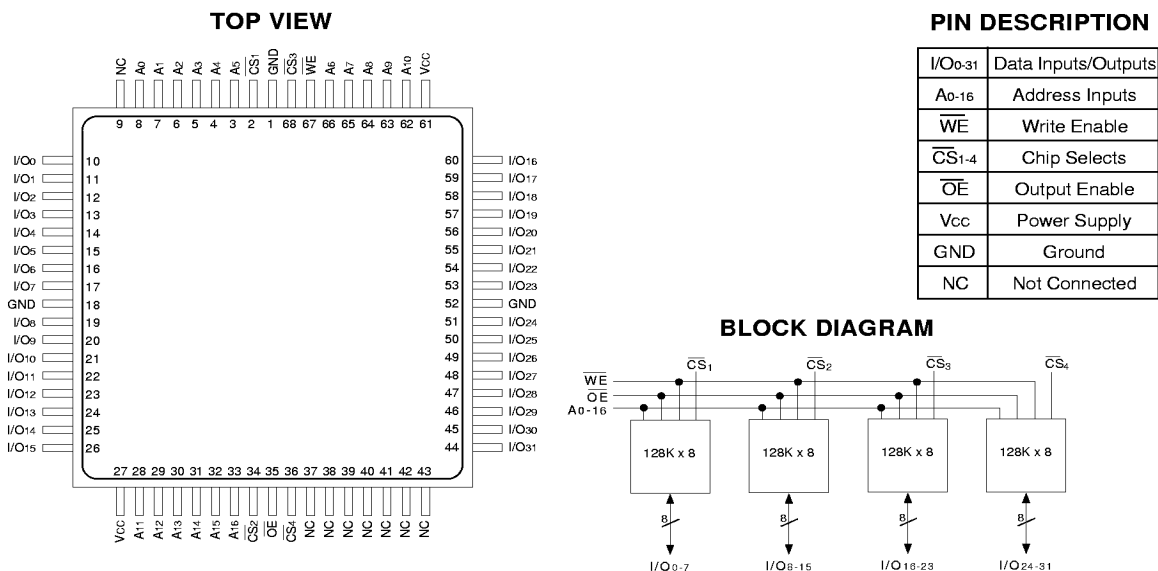
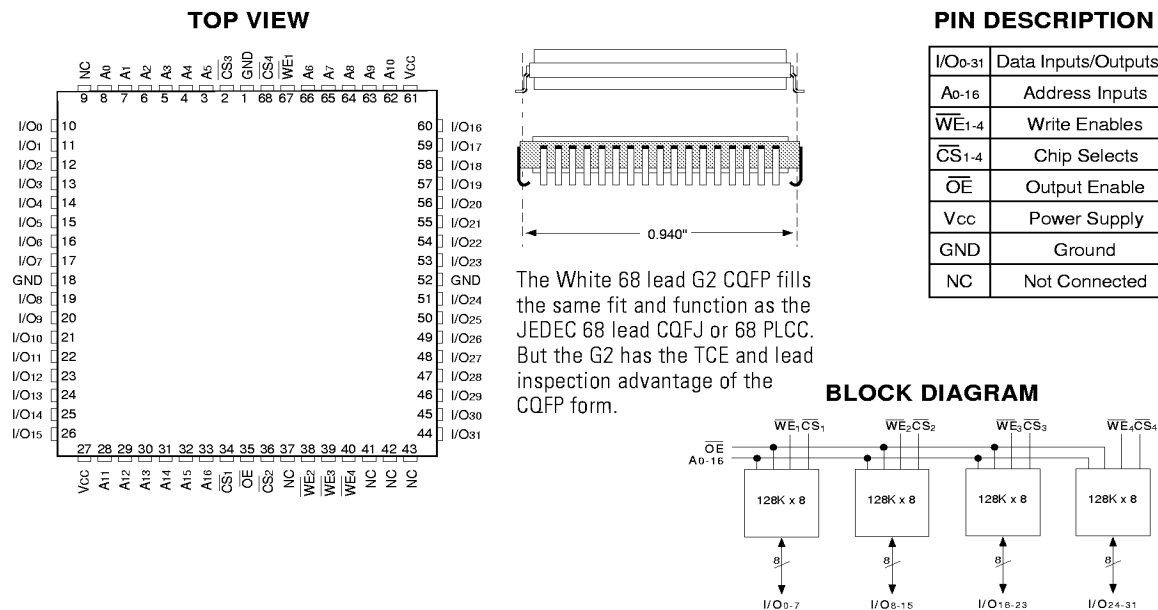




**FIG. 2 PIN CONFIGURATION FOR WS128K32-15G4TX, Package to be developed****FIG. 3 PIN CONFIGURATION FOR WS128K32-15G2X**



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-40	+85	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Ind.)	T _A	-40	+85	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA)	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4T			50	
CQFP G2			20	
$\overline{CS}$ 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Sym	Conditions	-15		Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC}	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		750	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		80	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{CC} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V



AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter Read Cycle	Symbol	-15		Units
		Min	Max	
Read Cycle Time	t _{RC}	15		nS
Address Access Time	t _{AA}		15	nS
Output Hold from Address Change	t _{OH}	0		nS
Chip Select Access Time	t _{ACS}		15	nS
Output Enable to Output Valid	t _{OE}		10	nS
Chip Select to Output in Low Z	t _{CLZ} ¹	3		nS
Output Enable to Output in Low Z	t _{OLZ} ¹	0		nS
Chip Disable to Output in High Z	t _{CHZ} ¹		12	nS
Output Disable to Output in High Z	t _{OHZ} ¹		12	nS

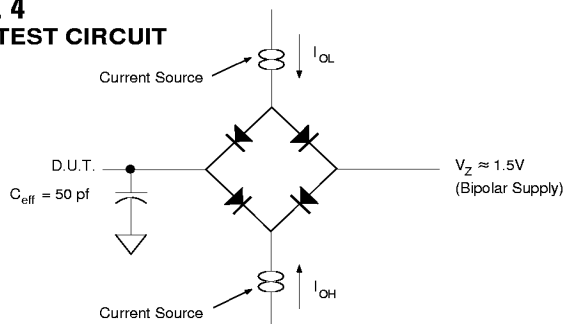
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter Write Cycle	Symbol	-15		Units
		Min	Max	
Write Cycle Time	t _{WC}	15		nS
Chip Select to End of Write	t _{CW}	14		nS
Address Valid to End of Write	t _{AW}	14		nS
Data Valid to End of Write	t _{DW}	10		nS
Write Pulse Width	t _{WP}	14		nS
Address Setup Time	t _{AS}	0		nS
Address Hold Time	t _{AH}	0		nS
Output Active from End of Write	t _{OW} ¹	3		nS
Write Enable to Output in High Z	t _{WHZ} ¹		10	nS
Data Hold Time	t _{DH}	0		nS

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



FIG. 5
TIMING WAVEFORM - READ CYCLE

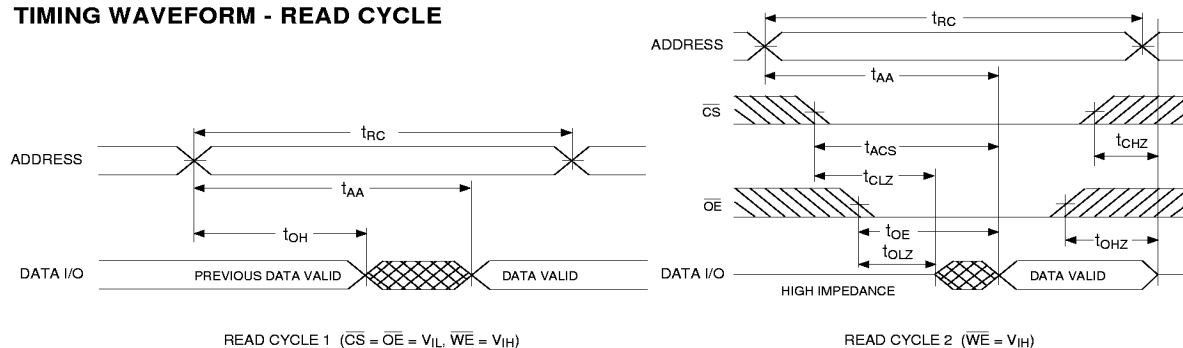


FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED

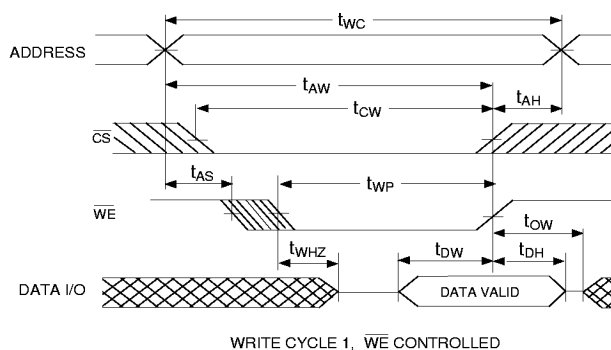
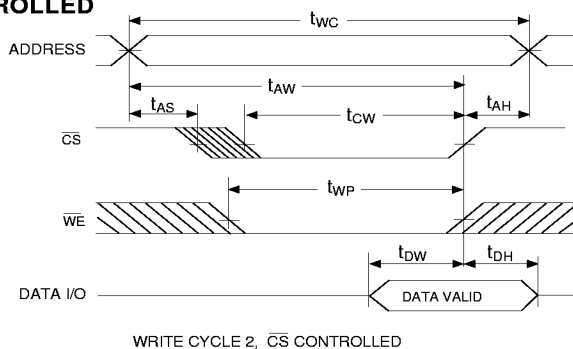
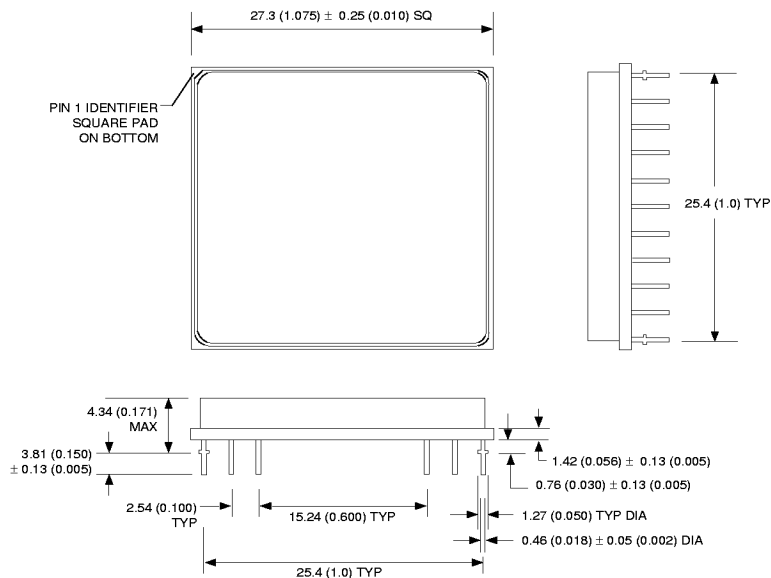
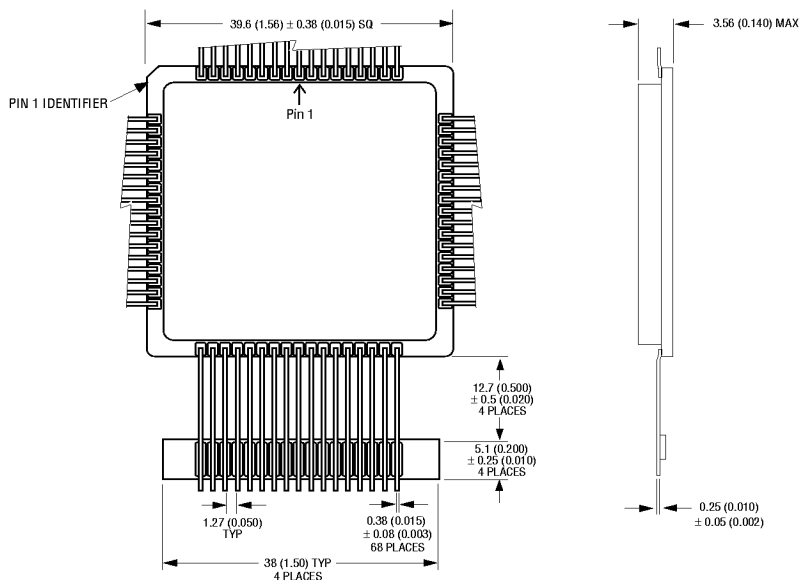


FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**

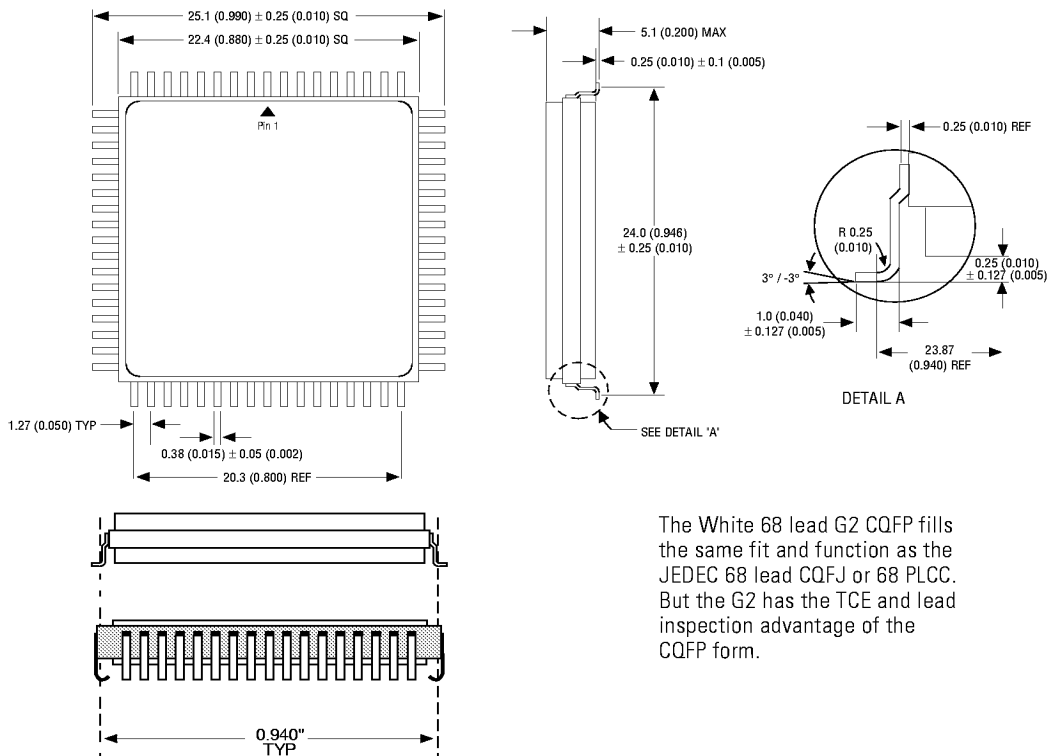
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)



The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION****W S 128K 32 X - 15 X X****DEVICE GRADE:**

I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:

H1 = Ceramic Hex-In-line Package, HIP (Package 400)
G2 = 22 mm Ceramic Quad Flat Pack, CQFP (Package 500)
G4T = 40 mm Low Profile CQFP (Package 502)

ACCESS TIME in nS**IMPROVEMENT MARK:**

N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades

ORGANIZATION, 128Kx32

User configurable as 256Kx16 or 512Kx8

SRAM**WHITE MICROELECTRONICS**