PLC16V8 Series
Erasable and OTP PAL®-Type Device

Signetics Programmable Logic
Product Specification

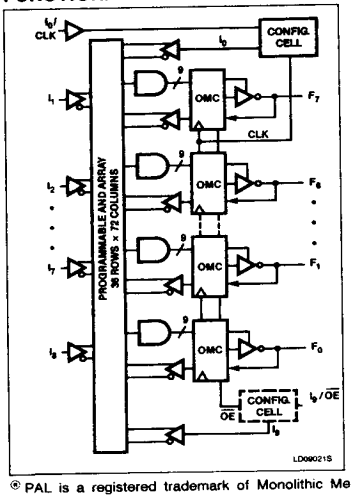
Application Specific Products
- **Series 20**

DESCRIPTION

The PLC16V8 Programmable Array Logic device is a 20-pin CMOS PLD designed to replace full-power as well as quarter-power and half-power Series 20 PAL® devices. Available in four speed/power configurations, the generic PLC16V8 device can be configured to emulate 22 different PAL devices in multiple speed/power configurations. The more complex AND/OR logic functions can be easily implemented with the flexibility inherent to its generic Output Macro Cell architecture.

The PLC16V8 is a two-level logic element comprised of 10 inputs, 72 AND gates and 8 Output Macro Cells (OMC). Each Output Macro Cell can be individually configured as a dedicated input, a dedicated output, a bidirectional I/O or as a registered output with feedback. This generic architecture provides a means of reducing documentation, inventory and manufacturing related costs. Furthermore, the PLC16V8 series devices are designed to accept both TTL and CMOS input levels to facilitate logic integration in almost any system environment.

FUNCTIONAL DIAGRAM



FEATURES

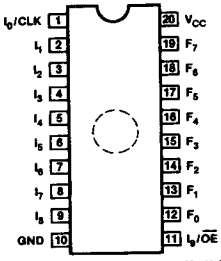
- **100% functional replacement for Series 20 PAL devices**
  $-I_{OL}$ = 24mA
- **Low power performance:**
  50 and 90mA max
  - **All inputs and outputs switching at 15MHz**
- **Equivalent bipolar performance**
  - **35 and 45ns t_{PD}**
  - **28.5 and 22.2MHz f_{MAX} (async)**
- **EPROM cell technology**
  - **Erasable**
  - **100% testable**
  - **Reconfigurable (quartz window package only)**
- **TTL and CMOS compatible**
- **Security fuse**
- **Available in 300mil-wide DIP with quartz window, plastic DIP (OTP), or PLCC (OTP)**

PIN LABEL DESCRIPTIONS

I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)

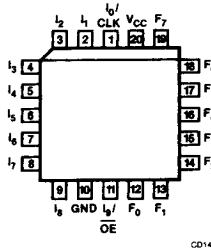
PIN CONFIGURATIONS

N and FA Packages



N = Plastic
FA = Ceramic with Quartz Window

A Package



A = Plastic Leaded Chip Carrier

PAL DEVICE TO PLC16V8 OUTPUT PIN CONFIGURATION CROSS REFERENCE

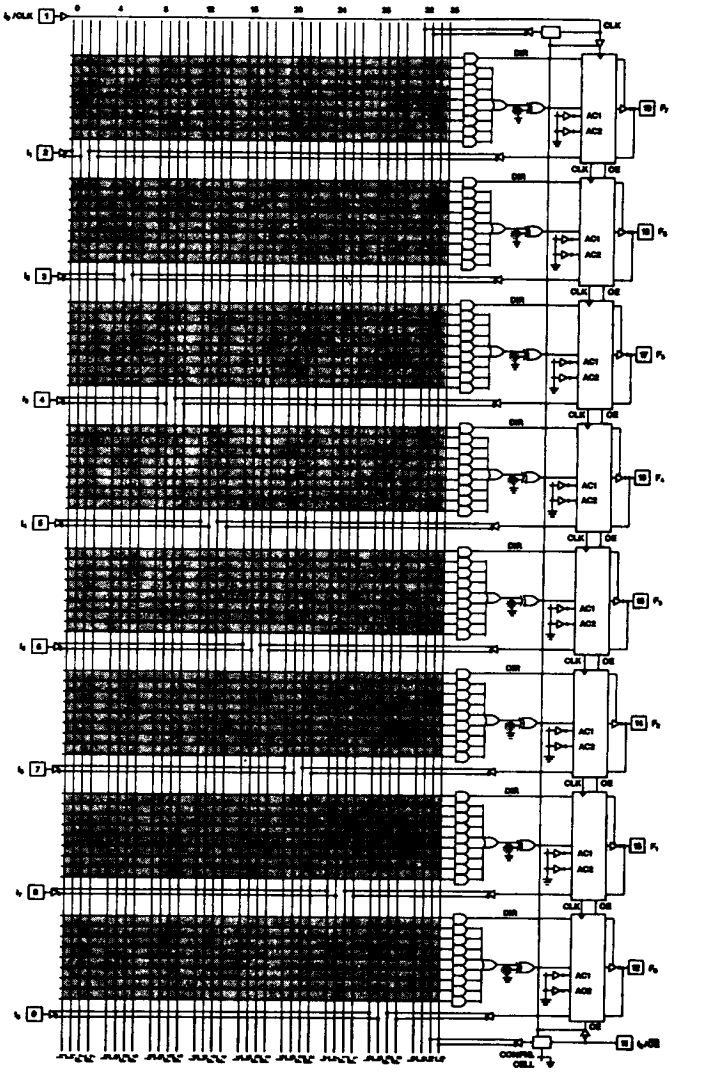
PIN NO.	PLC 16V8	16L8 16H8 16P8 18P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	$I_9/\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

® PAL is a registered trademark of Monolithic Memories, Inc., a wholly owned subsidiary of Advanced Micro Devices, Inc.

Erasable and OTP PAL®-Type Device

PLC16V8 Series

LOGIC DIAGRAM



NOTES:

In the unprogrammed or virgin state:

All cells are in a conductive state.
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is non-inverting.

Pins 1 and 11 are configured as inputs 0 and 9, respectively, via the configuration cell. The clock and $\overline{OE}$ functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
□ Denotes a programmable cell location.

Erasable and OTP PAL®-Type Device

PLC16V8 Series

The Signetics state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at one-quarter to one-half the power consumption. The erasable nature of the EPROM process enables Signetics to functionally test the devices prior to shipment to the customer. Additionally, this allows Signetics to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

Signetics' AMAZE PLD design software supports all aspects of design, simulation and programming. For simple conversion of existing PAL device codes into the PLC16V8 series format, a PAL-to-V8 Converter is also available. This stand-alone, single-disk software package translates a PAL device code (from a device or a JEDEC standard fuse map) into an equivalent PLC16V8 series JEDEC format. The PAL-to-V8 converter, which runs on an IBM PC or compatible, includes the necessary programmer interface software for most commercially available programmers.

THE OUTPUT MACRO CELL (OMC)

The PLC16V8 has 8 individually programmable Output Macro Cells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the table, 4 different configurations may be implemented.

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common — from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

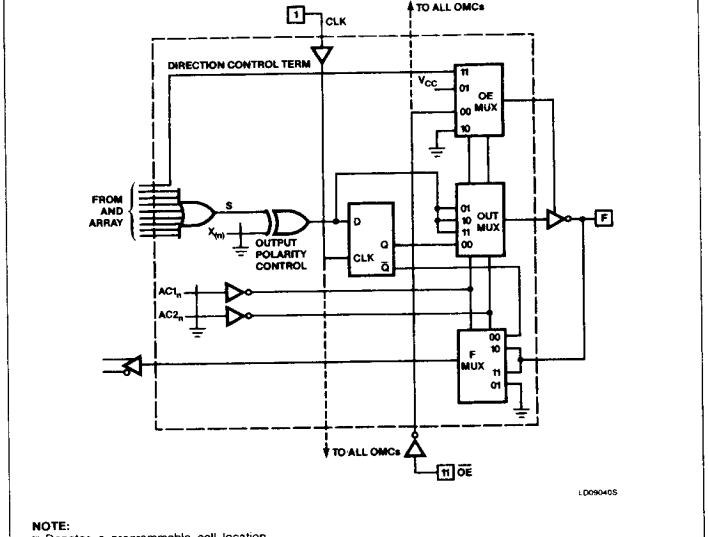
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follow:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_n$	$AC2_n$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registered OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

OUTPUT MACRO CELL (OMC)



NOTE:
□ Denotes a programmable cell location.

Erasable and OTP PAL®-Type Device

PLC16V8 Series

ORDERING INFORMATION

DESCRIPTION			ORDER CODE
Propagation Delay (Max)		I_{CC} (Active at 15MHz)	
t_{PD} = 35ns	f_{MAX} = 18.1MHz (Synchronous)	50mA	PLC16V8Q35
		90mA	PLC16V8H35
t_{PD} = 45ns	f_{MAX} = 13.3MHz (Synchronous)	50mA	PLC16V8Q45
		90mA	PLC16V8H45
Package Type			PACKAGE[1]
20-pin Plastic DIP (one time programmable; OTP)			N
20-pin Plastic Leaded Chip Carrier			A
20-pin Ceramic DIP with quartz window (reprogrammable)			FA

NOTE:
1. The package order code directly follows the device order code, i.e., PLC16V8Q35N for Plastic DIP (OTP).

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V_{DC}
V_{IN}	Input voltage	−0.5 to V_{CC} +0.5	V_{DC}
V_{OUT}	Output voltage	−0.5 to V_{CC} +0.5	V_{DC}
I_{IN}	Input currents	−10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

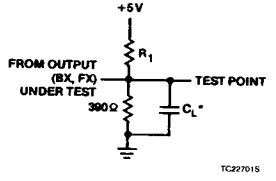
NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLC16V8 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

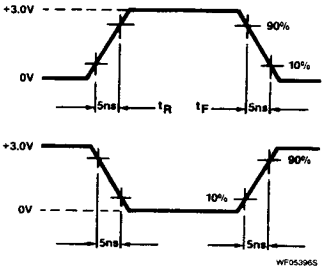
AC TEST CONDITIONS



*C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

Test Load Circuit

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Erasable and OTP PAL®-Type Device

PLC16V8 Series

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION		LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Input voltage[2]							
V_{IL}	Low	V_{CC} = Min		−0.3		0.8	V
V_{IH}	High	V_{CC} = Max		2.0		V_{CC} + 0.3	V
Output voltage[2]							
V_{OL}	Low	V_{CC} = Min I_{OL} = 24mA				0.5	V
V_{OH}	High	I_{OH} = −3.2mA		2.4			V
Input current							
I_{IL}	Low[6]	V_{IN} = GND				−10	μA
I_{IH}	High	V_{IN} = V_{CC}				10	μA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND				10 −10	μA μA
I_{OS}	Short-circuit[3, 7]	V_{OUT} = GND				−130	mA
I_{CC}	V_{CC} supply current (Active)[4]	I_{OUT} = 0mA f = 15MHz[5]	Quarter power (Q)			50	mA
			Half power (H)			90	mA
Capacitance							
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V			12		pF
C_B	I/O	V_B = 2.0V			15		pF

NOTES:
1. All typical values are at V_{CC} = 5V. T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all inputs and outputs switching.
5. Refer to Figure 1, ΔI_{CC} vs Frequency (worst case). (Referenced from 15MHz)
6. I_{IL} for Pin 1 (I_0/CLK) is ±10μA with V_{IN} = 0.4V.
7. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.

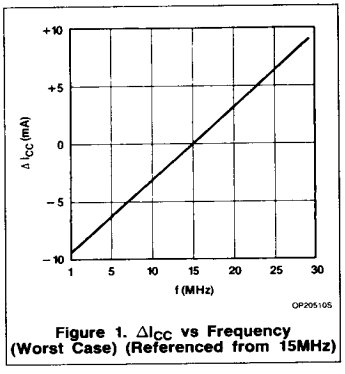


Figure 1. ΔI_{CC} vs Frequency (Worst Case) (Referenced from 15MHz)

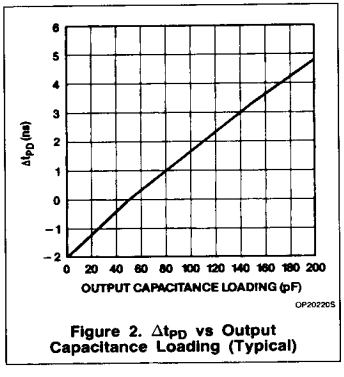


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$ $R_2 = 390\Omega$

SYMBOL	PARAMETER	TO	FROM	TEST CONDITION[1]		PLC16V8Q-35 PLC16V8H-35		PLC16V8Q-45 PLC16V8H-45		UNIT
				R_1 (Ω)	C_L (pF)	Min	Max	Min	Max	
Pulse width										
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +			55		75		ns
t_{CKH}	Clock width High	CLK –	CLK +			20		25		ns
t_{CKL}	Clock width Low	CLK +	CLK –			20		25		ns
Hold time										
t_{IH}	Input or feedback data hold time	Input ±	CLK +			0		0		ns
Setup time										
t_{IS}	Input or feedback data setup time	CLK +	I ±, F ±			30		40		ns
Propagation delay										
t_{PD}	Delay from input to active output	F ±	I ±, F ±	200	50		35		45	ns
t_{CKO}	Clock High to output valid access Time	F ±	CLK +	200	50		25		35	ns
t_{OE1}[3]	Product term enable to active output	F ±	I ±, F ±	Active-High R = 1.5k Active-Low R = 550	50		35		45	ns
t_{OD1}[2]	Product term disable to outputs off	F ±	I ±, F ±	From V_{OH} R = ∞ From V_{OL} R = 200	5		35		45	ns
t_{OD2}[2]	Pin 11 output disable High to outputs off	F ±	OE –	From V_{OH} R = ∞ From V_{OL} R = 200	5		25		30	ns
t_{OE2}[3]	Pin 11 output enable to active output	F ±	OE +	Active-High R = 1.5k Active-Low R = 550	50		25		30	ns
t_{PPR}	Power-up reset	F +	V_{CC} +				35		45	ns
Frequency of operation ($t_{IS} + t_{CKO}$)										
f_{MAX}	Maximum frequency	Synch. Asynch.		200	50		18.1 28.5		13.3 22.2	MHz

NOTES:
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. 3-State levels are measured ± 0.5V from the active steady-state level.
3. Resistor values of 1.5k and 550Ω provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.

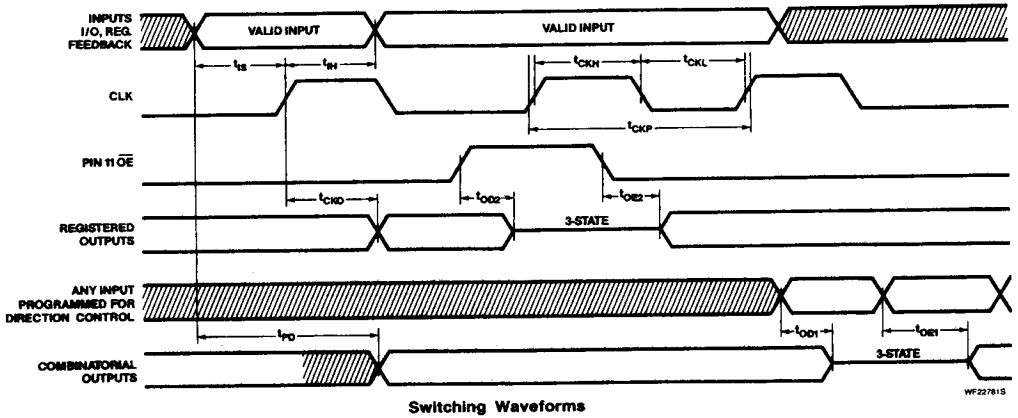
POWER-UP RESET

In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC16V8. All internal registers will reset to active-Low (logical "0") after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an active-High on the associated output pin because of the inverted output buffer. The internal feedback ($\overline{Q}$) of a registered OMC will also be set High. The programmed polarity of OMC will not affect the active-High output condition during a system power-up condition.

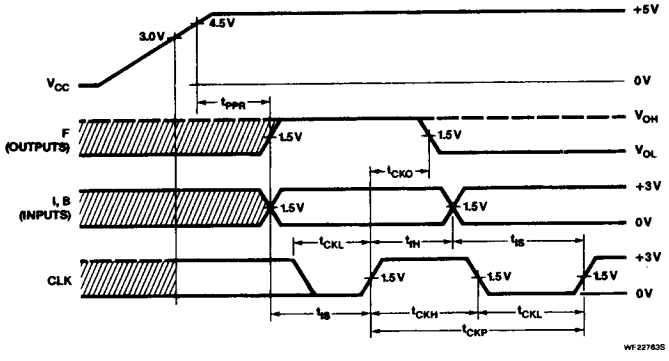
The following conditions must be considered when the asynchronous power-up reset occurs. V_{CC} rise to 4.5V (90%) must be monotonic. The clock input must stabilize to a valid TTL level prior to the V_{CC} rise to 60% (3.0V). All input setup and hold times (t_{IS} and t_{IH}) must be adhered to prior to clocking the device.

3

TIMING DIAGRAMS



Switching Waveforms



NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output conditon (enabled or disabled).

Power-Up Reset

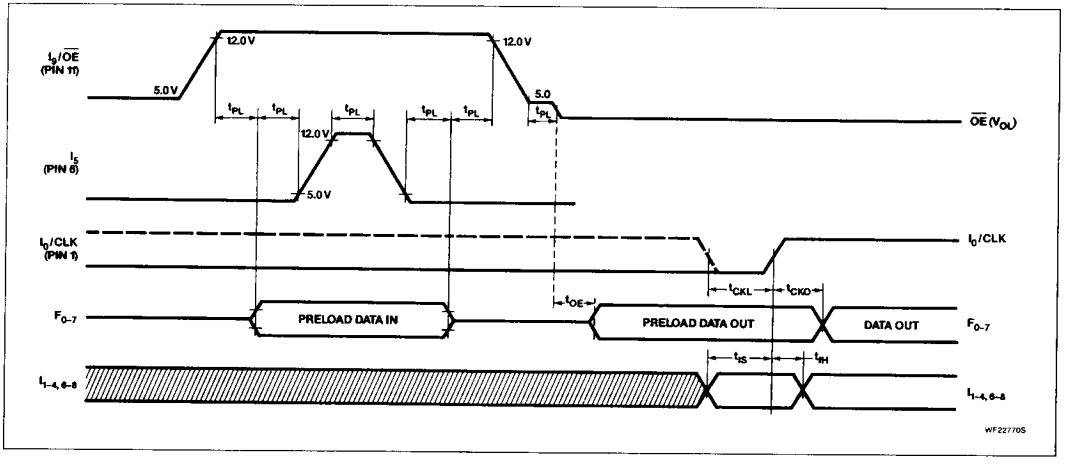
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC16V8 series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_9/\overline{OE}$ and I_5). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register $\overline{Q}$ output via the feedback path will reflect the complement of the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references.

REGISTER PRELOAD (DIAGNOSTIC MODE)



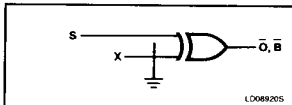
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic Programming equipment.

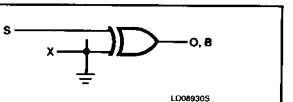
With Logic programming, the AND/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2, as shown below. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY — (O, B)

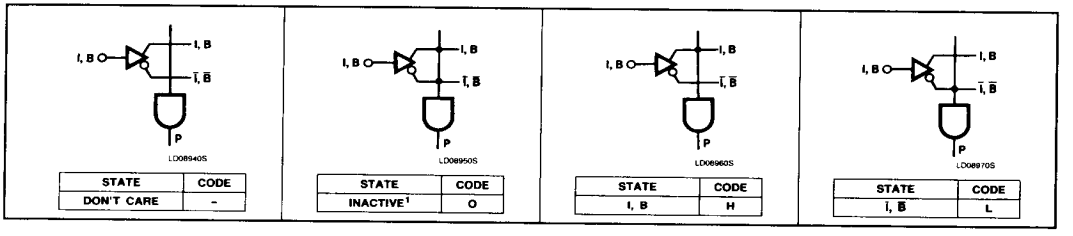


ACTIVE LEVEL	CODE
INVERTING	L



ACTIVE LEVEL	CODE
NON-INVERTING	H

"AND" ARRAY — (I, B)



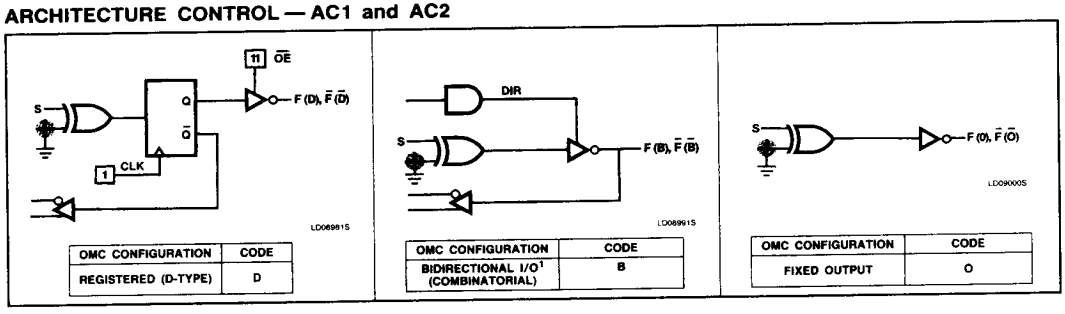
STATE	CODE
DON'T CARE	-

STATE	CODE
INACTIVE[1]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I}$, $\overline{B}$	L

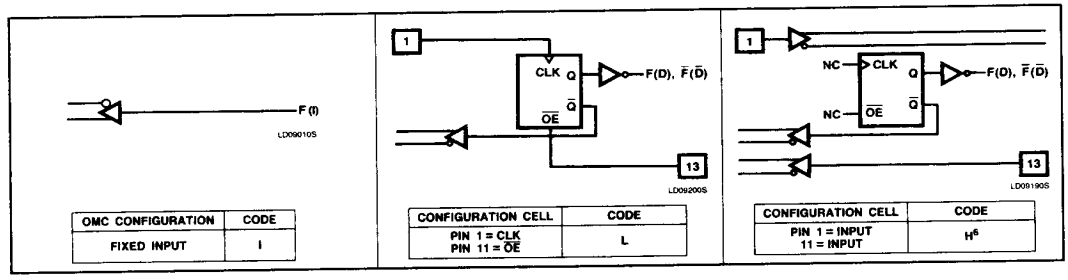
ARCHITECTURE CONTROL — AC1 and AC2



OMC CONFIGURATION	CODE
REGISTERED (D-TYPE)	D

OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O[1] (COMBINATORIAL)	B

OMC CONFIGURATION	CODE
FIXED OUTPUT	O



OMC CONFIGURATION	CODE
FIXED INPUT	I

CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = $\overline{OE}$	L

CONFIGURATION CELL	CODE
PIN 1 = INPUT 11 = INPUT	H[6]

NOTE:

A factory shipped unprogrammed device is configured such that:

1. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is non-inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC16V8 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC16V8 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC16V8 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC16V8 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000μW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000μW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAM TABLE