P4C218
LATCHED HIGH-SPEED 16Kx16 STATIC RAM

ADVANCE INFORMATION

FEATURES

- Full CMOS Design
- Supports Processor Speeds to 60MHz
- On-Chip Address and Chip Enable Latch
- On-Chip Input Data Latch
- Byte Write Strobe Controls
- Dual Chip Enable for Depth Expansion
- Power Down Mode When Deselected
- 5V ±10% Power Supply
- Output Enable Control
- TTL-Compatible I/O
- Outputs Drive up to 85pF
- 52-Pin PLCC Package

DESCRIPTION

The P4C218 is a 262,144-bit CMOS static RAM organized as 16K words, each 16 bits wide, for cache applications. The SCRAM contains on-chip address and chip enable latches controlled by ALE. A separate control, DL, latches the input data. All latches are transparent when the latch enable controls are HIGH, so the P4C218 can be used as a general-purpose asynchronous 16Kx16 SRAM by connecting ALE and DL to Vcc.

The address and chip enable latches make the P4C218 ideally suited for R3000 cache applications. Four units make up a 64KByte i- (or d-) cache; the two chip enable controls facilitate easy expansion to 128KBytes. Individual byte write operations are possible using $\overline{BWL}$ and $\overline{BWH}$ strobes to qualify the $\overline{WE}$ control, a useful feature for ix86 cache applications.

Power dissipation is 2.0W (max.) when active, and only 200mW in standby mode. The P4C218 can be used as the secondary cache for low-cost R4000S workstations; 11 units form a 256KByte cache, expandable to 512KBytes with 22 units.

With access times of 15ns, the P4C218 can support all popular microprocessors to 60MHz while keeping chip count and power dissipation low. Outputs can drive up to 85pF loads, so no external buffers are required.

The P4C218 is manufactured using PACE III Technology, and is available in a 52-pin PLCC package, providing excellent board density.

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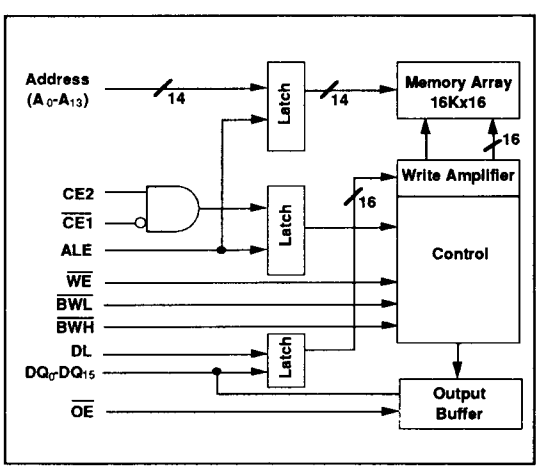
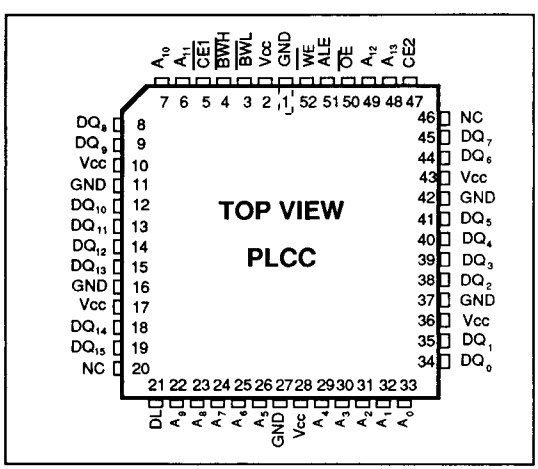
FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	–0.5 to +7.0	V
V_{IN}	DC Input Voltage	–0.5 to V_{CC} +0.5	V
$V_{I/O}$	DC Input Voltage Applied to Output in High-Z	–0.5 to V_{CC} +0.5	V
P_D	Power Dissipation	2	W
T_{OPR}	Operating Temperature	–55 to +125	°C

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
	ESD per MIL-STD-883C Method 3015	> 2001	V
	Latchup Current	> 200	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Military	–55 to +125°C	0V	5.0V ± 10%

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Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage

Symbol	Parameter	Test Conditions	P4C218		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage		–0.5[2]	0.8	V
I_{LI}	Input Leakage Current	GND < V_{IN} < V_{CC}	–10	+10	µA
I_{LO}	Output Leakage Current	GND < V_O < V_{CC}, Output Disabled	–10	+10	µA
I_{CC}	Vcc Operating Current	V_{CC} = Max., I_{OUT} = 0 mA		360	mA
I_{SB}	Standby Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE1} \le V_{IL}$, $CE2 \ge V_{IH}$		40	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4		V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., I_{OUT} = GND		–350	mA

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CAPACITANCES[3]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF

Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

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Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Transient inputs with V_{IL} & I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
3. This parameter is sampled and not 100% tested.
4. I_{CC} is measured with $\overline{OE} \ge$ 3.0V and input levels at 0V for all inputs.

AC ELECTRICAL CHARACTERISTICS – READ CYCLE

(Vcc = 5V ±10%, All Temperature Ranges)

Sym	Parameter	-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		25		ns
t_{AA}	Address Access Time		15		20		25	ns
t_{AC}	Chip Select Access Time		15		20		25	ns
t_{OE}	Output Enable to Output Valid		6		8		10	ns
t_{OH}	Output HOLD from address change	4		4		4		ns
t_{LZ}	Chip Enable to low-Z	2		2		2		ns
t_{OLZ}	Output Enable to low-Z	2		2		2		ns
t_{HZ}	Chip Enable to high-Z		7		9		10	ns
t_{OHZ}	Output Enable to high-Z		6		9		10	ns
t_{PALE}	ALE pulse width		5		5		5	ns
t_{SALE}	Address Setup to ALE Low		2		2		2	ns
t_{HALE}	Address Hold from ALE Low		3		3		3	ns

Notes: 1. $\overline{WE}$ must be HIGH for the Read Cycle.
2. Both $\overline{CE}1$ and CE2 must be active. Only $\overline{CE}1$ is shown in the timing diagrams.

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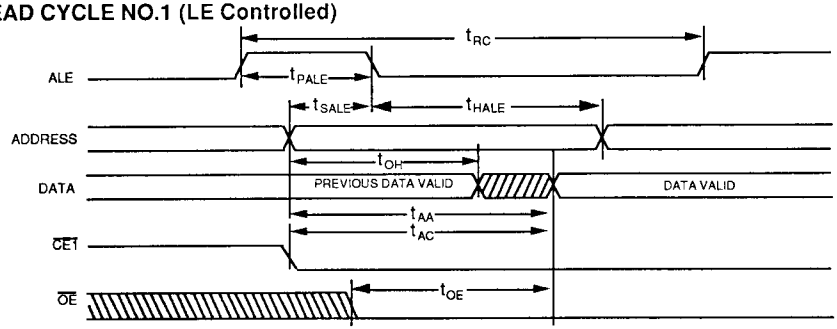
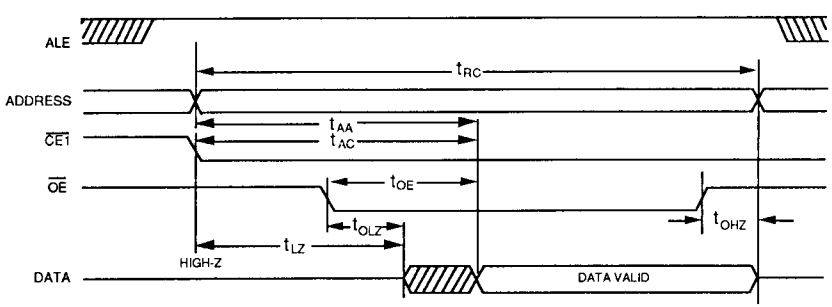
READ CYCLE NO.1 (LE Controlled)



READ CYCLE NO.2 (Address Controlled)



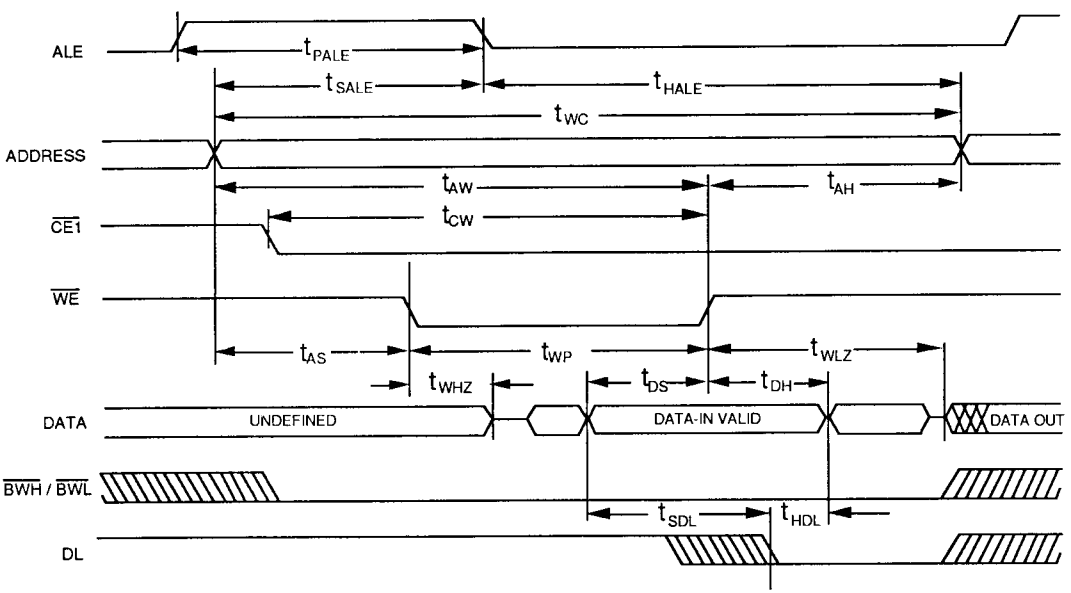
AC ELECTRICAL CHARACTERISTICS – WRITE CYCLE

(VCC= 5V ±10%, All Temperature Ranges)

Sym	Parameter	-15		-20		-25		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		20		25		ns
t_{AW}	Address Setup to End of Write	13		15		20		ns
t_{CW}	Chip Select to End of Write	13		15		20		ns
t_{DS}	Data Setup to End of Write	6		8		10		ns
t_{DH}	Data Hold from End of Write	0		0		0		ns
t_{WP}	Write Enable Pulse Width	12		15		20		ns
t_{AS}	Address Setup to Write Enable	0		0		0		ns
t_{AH}	Address Hold from Write Enable	0		0		0		ns
t_{WLZ}	Write Enable High to Low-Z	5		5		5		ns
t_{WHZ}	Write Enable Low to High-Z		8		9		10	ns
t_{PALE}	ALE Pulse Width		5		5		5	ns
t_{SDL}	Data Setup to DL Low	1		1		1		ns
t_{HDL}	Data Hold from DL Low	3		3		3		ns

Notes: 1. Both $\overline{CE1}$ and CE2 must be active. Only $\overline{CE1}$ is shown in the timing diagrams.
2.Input data can be optionally latched by DL. Setup and Hold times must be met.
3. $\overline{BWH}$, $\overline{BWL}$ control the specific byte being written to.

WRITE CYCLE



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 & 2

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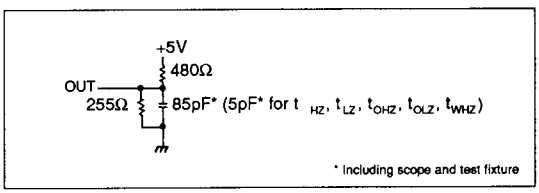

Figure 1. Output Load

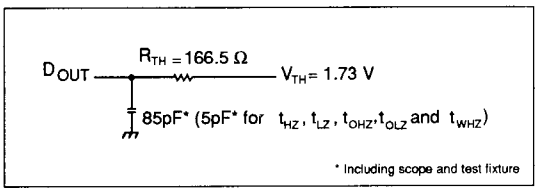

Figure 2. Thevenin Equivalent

Note:
Because of the ultra-high speed of the P4C218, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

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TRUTH TABLE

$\overline{CE}_1$	CE_2	$\overline{BWH}$	$\overline{BWL}$	$\overline{WE}$	$\overline{OE}$	Mode	Input/Output	
							Bits 15-8	Bits 7-0
H	X	X	X	X	X	Deselected Cycle	High Z	High Z
X	L	X	X	X	X			
L	H	X	X	H	H	Output Disabled	High Z	High Z
L	H	X	X	H	L	Read Word	Data Out	Data Out
L	H	L	H	L	X	Write High Byte	Data In	High Z
L	H	H	L	L	X	Write Low Byte	High Z	Data In
L	H	L	L	L	X	Write Word	Data In	Data In

Notes:
1. Power supply current is I_{SB} in the deselected cycle, I_{CC} in all other modes.
2. ALE and DL must be HIGH if the P4C218 is used in the unlatched mode, as a general purpose SRAM.
3. Addresses and CE controls are latched by the falling edge of ALE. Set-up and hold times requirements must be met if used in the latched mode for read and write operations.
4. Data In is latched by the falling edge of DL. Set-up and hold time requirements must be met if input data must be latched during the write operation.

APPLICATION EXAMPLES

Cache Ram Configurations for PR3000A and i386/i486

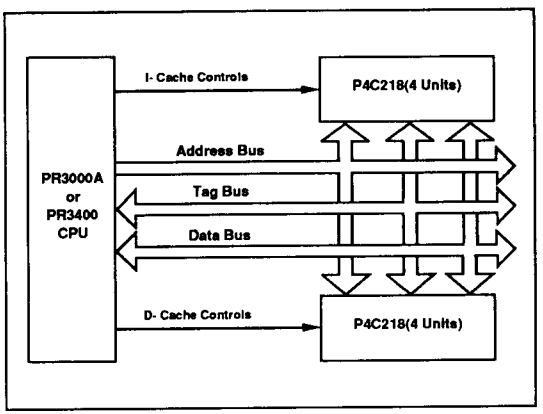

Figure 3 MIPS PR3000A or PR3400 (64KByte i- & d- Caches)

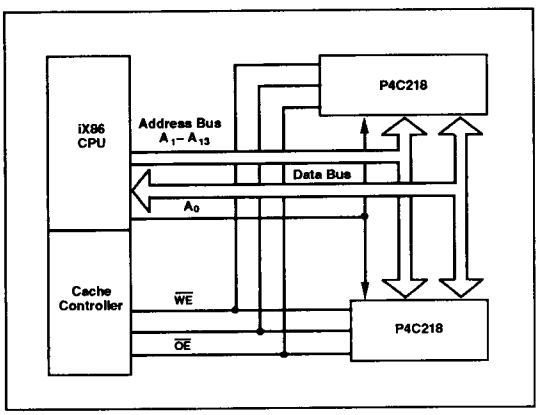

Figure 4 iX86 64KByte Cache

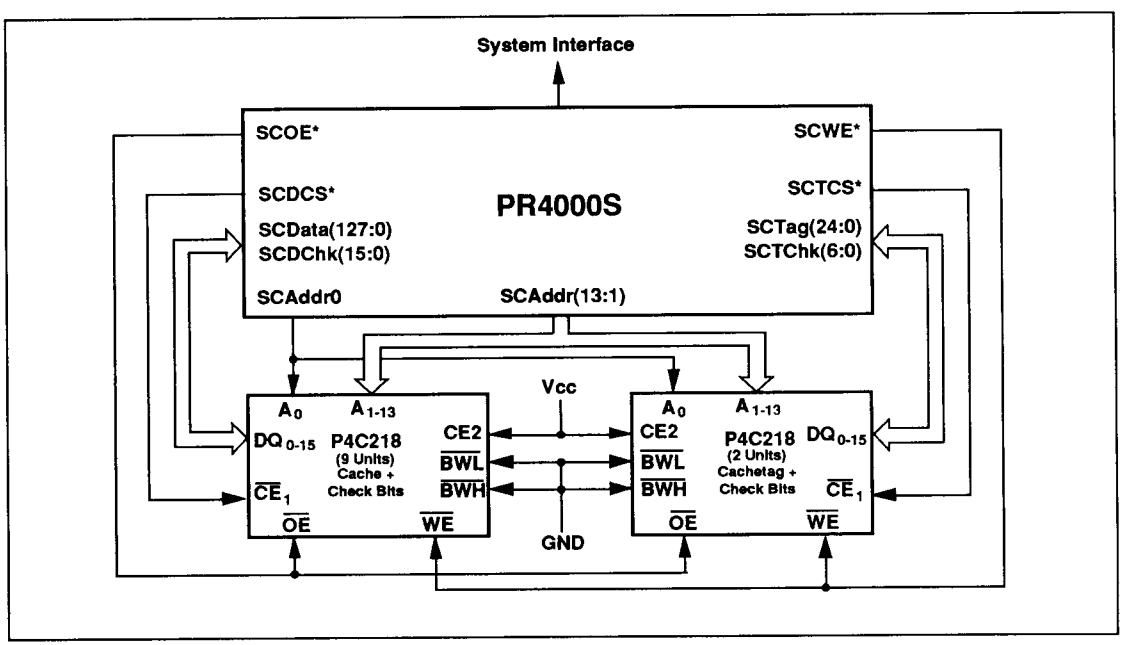

Figure 5 PR4000 Secondary Cache: 256 KByte cache in joint instruction-data configuration

PACKAGE SUFFIX

Package Suffix	Description
PP	Plastic Leaded Chip Carrier (PLCC)
GR	Quad Cerpak (J-Bend Leads)

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TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
B	–55°C to +125°C with MIL-STD-883C Class B compliance

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SELECTION GUIDE

The P4C218 is available in the following temperature, speed and package options.

Temperature Range	Package	15ns	20ns	25ns
Commercial	PLCC	-15 PP52C	-20 PP52C	-25 PP52C
Military Processed*	Quad CERPAK	N/A	N/A	-25 GR52B

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* Military temperature range with MIL-STD-883 Revision D, Class B processing.
N/A = Not available

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The P4C218 supports the high performance processor speeds of the i386 and i486, and the PR3000A/PR3400.

Processor	Frequency	Access Time	Output Enable	Performance Part Type
i386	40 MHz	20ns	8ns	P4C218 - 20
	33 MHz	25ns	10ns	P4C218 - 25
	25 MHz	35ns	13ns	P4C218 - 25
i486	50 MHz	15ns	7ns	P4C218 - 15
	33 MHz	20ns	8ns	P4C218 - 20
R3000	33 MHz	15ns	7ns	P4C218 - 15
	25 MHz	20ns	9ns	P4C218 - 20
	20 MHz	25ns	12ns	P4C218 - 25

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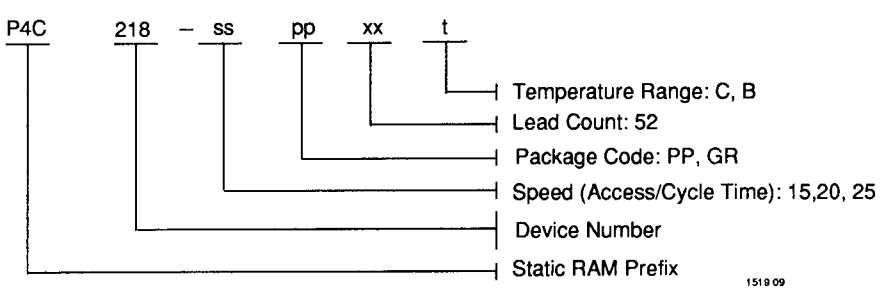
ORDERING INFORMATION

The following part numbering scheme is used for



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