HYUNDAI SEMICONDUCTOR

HYM5C9256

256K×9-Bit CMOS DRAM MODULE

M421202B-OCT91

T-46-23-17

DESCRIPTION

The HYM5C9256M is a 256K words by 9 bits dynamic RAM module and consists of nine HY53C256LF Fast Page mode CMOS DRAMs in 18 pin PLCC package mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the 256K DRAMs.

HYM5C9256M is suitable for easy interchange and addition of 256K bytes memory with parity RAM.

FEATURES

- **Fast Page Mode operation**
- **Fast access time**

	t_{RAC}	t_{CAC}	t_{PC}
HYM5C9256-70	70	15	50
HYM5C9256-80	80	20	55
HYM5C9256-10	100	25	60
HYM5C9256-12	120	30	70

- **Single power supply of 5V± 10%**
- **$\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.**
- **Low power operating**
  - **3.47W max.(HYM5C9256M-70)**
  - **2.97W max.(HYM5C9256M-80)**
  - **2.48W max.(HYM5C9256M-10)**
  - **2.23W max.(HYM5C9256M-12)**
- **TTL compatible inputs and outputs**
- **256 refresh cycles / 4ms**

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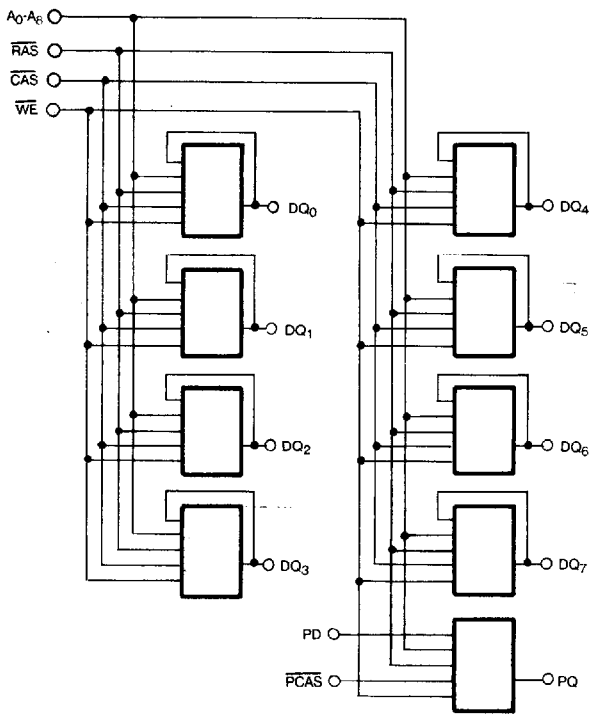
BLOCK DIAGRAM



PIN NAMES

A_0-A_8	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATA IN PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	$\overline{CAS}$ FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

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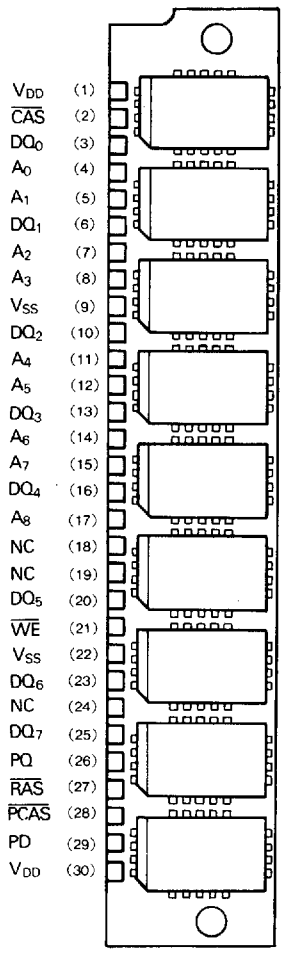
PIN CONNECTIONS

HYM5C9256M



NOTES :
1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out(DQ_0-DQ_7).

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	9	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM5C9256M		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			90	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70		630	mA	1, 2
			−80		540		
			−10		450		
			−12		405		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}			18	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70		630	mA	2
			−80		540		
			−10		450		
			−12		405		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70		405	mA	1, 2
			−80		360		
			−10		315		
			−12		270		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$, other inputs ≥ V_{SS}			9	mA	1
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70		630	mA	2
			−80		540		
			−10		450		
			−12		405		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :

1. I_{DD} is depends on output loading when the device output is selected. Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is depends upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

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AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM5C9256M								UNIT	NOTE
			70		80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	120	10K	ns	
2	t_{RC}	Read or Write Cycle Time	130		145		175		205		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50		55		65		75		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	15		15		15		20		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40		45		55		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	25	65	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		20		25		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	60	25	75	30	90	ns	2
11	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100		120	ns	3,4,5
12	t_{AA}	Access Time From Column Address		35		40		45		55	ns	5,6,12
13	t_{CAC}	Access Time from $\overline{CAS}$		15		20		25		30	ns	5,12
14	t_{CAS}	$\overline{CAS}$ Pulse Width	15	75K	20	75K	25	75K	30	75K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	15		20		25		30		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		5		ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		5		ns	7
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15		15		15		20		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	15	0	20	0	25	0	30	ns	8
21	t_{WP}	Write Command Pulse Width	15		15		20		25		ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	15		15		20		25		ns	
23	t_{AR}	Column Address Hold Time From $\overline{RAS}$	55		60		70		80		ns	
24	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	55		60		70		80		ns	
25	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	9,10
26	t_{WCH}	Write Command Hold Time	15		15		20		25		ns	
27	t_{DS}	Data In Set-up Time	0		0		0		0		ns	11
28	t_{DH}	Data In Hold Time	15		15		20		25		ns	11
29	t_{DHR}	Data In Hold Time Reference to $\overline{RAS}$	55		60		70		80		ns	
30	t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		55		65	ns	12

#	SYMBOL	PARAMETER	HYM5C9256M								UNIT	NOTE
			70		80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
31	t_{PC}	Fast Page Mode Cycle time	50		55		60		70		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		30		35		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		30		35		ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time, $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		10		10		ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time, $\overline{CAS}$ before $\overline{RAS}$ Refresh	20		25		30		40		ns	
37	t_T	Transition Time(Rise and Fail)	3	25	3	25	3	25	3	25	ns	
38	t_{REF}	Refresh Interval(256 cycle)		4		4		4		4	ms	

NOTES :

1. Operation within the t_{RAD}(max.)limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.)limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then the access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max.) and $t_{RAD} \leq t_{RAD}$(max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq t_{RAD}$(max.).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{OFF} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
10. t_{WCS} is not a ristrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min),the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
12. Access time is determined by the longer of t_{AA}, t_{CAC}, t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max).
14. AC measurements assume t_T=5ns.
15. An initial pause of 200μs is required after power-up and followed by at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

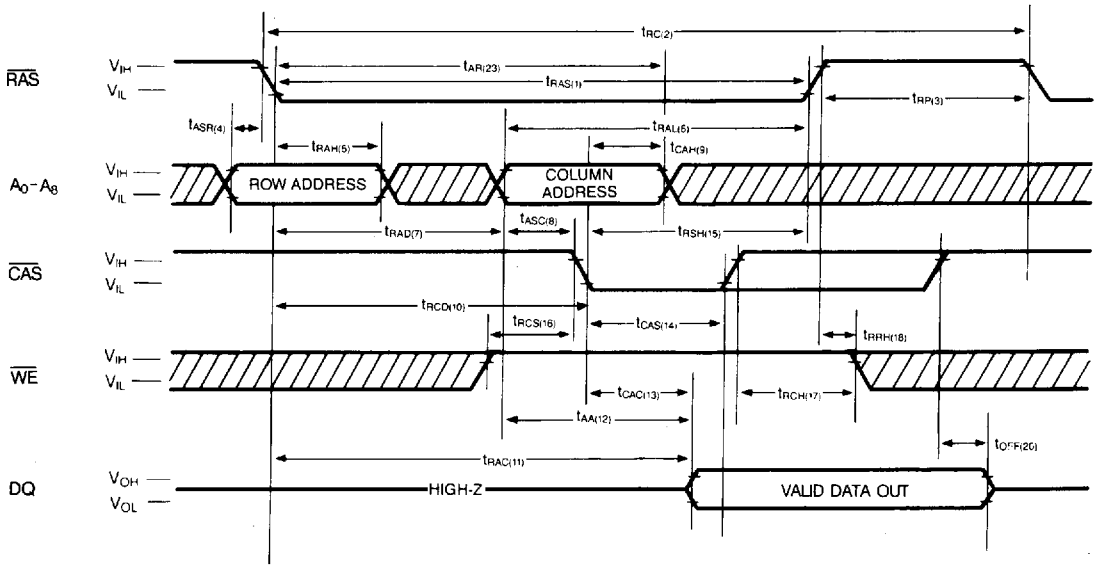
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_8, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

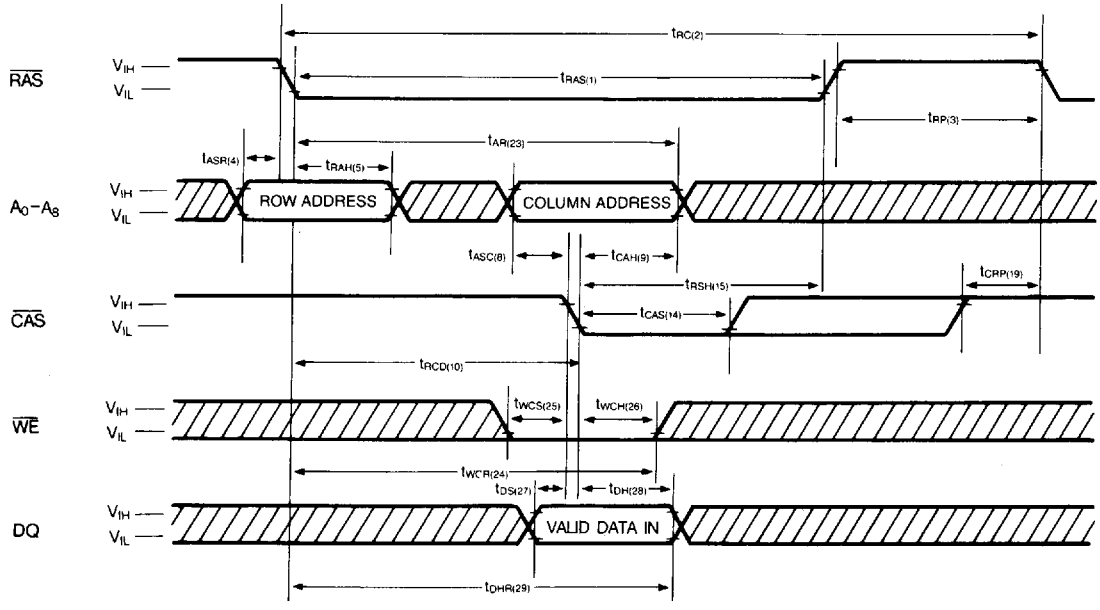
TIMING DIAGRAM

($\overline{CAS}$ includes $\overline{PCAS}$ and $\overline{CAS}$, D_{IN} includes DQ_0-DQ_7 and PD, D_{OUT} includes DQ_0-DQ_7 and PQ.)

READ CYCLE



EARLY WRITE CYCLE



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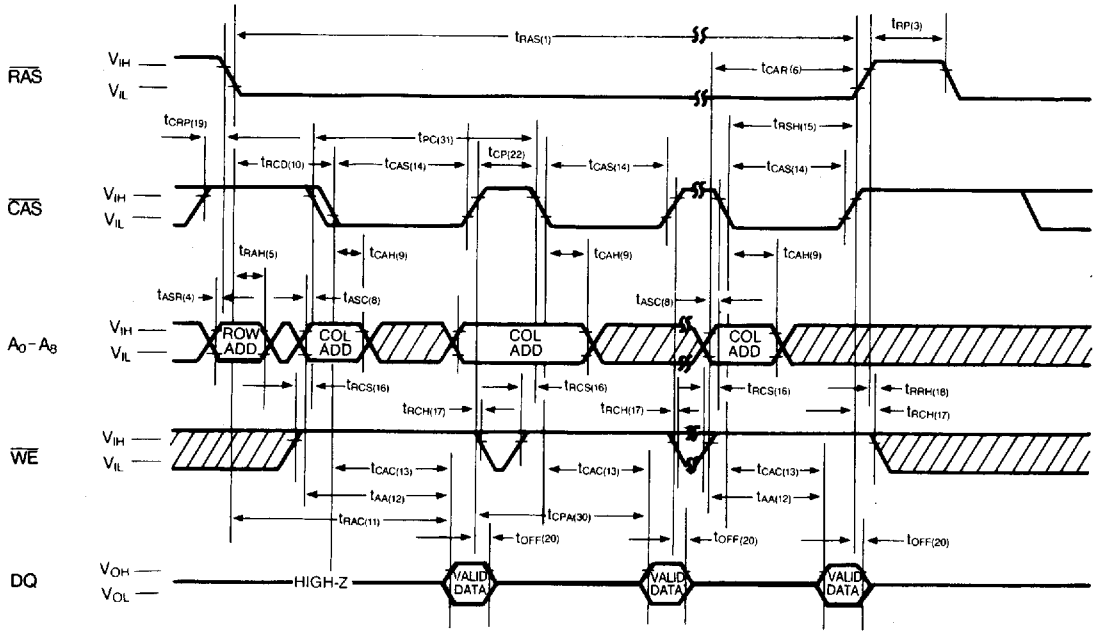
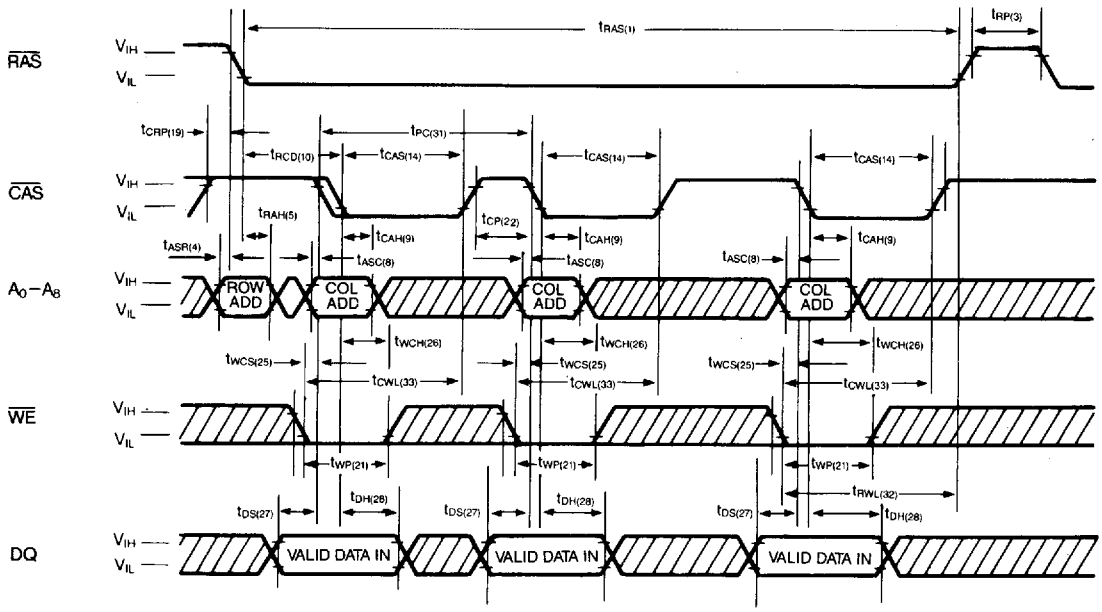
FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



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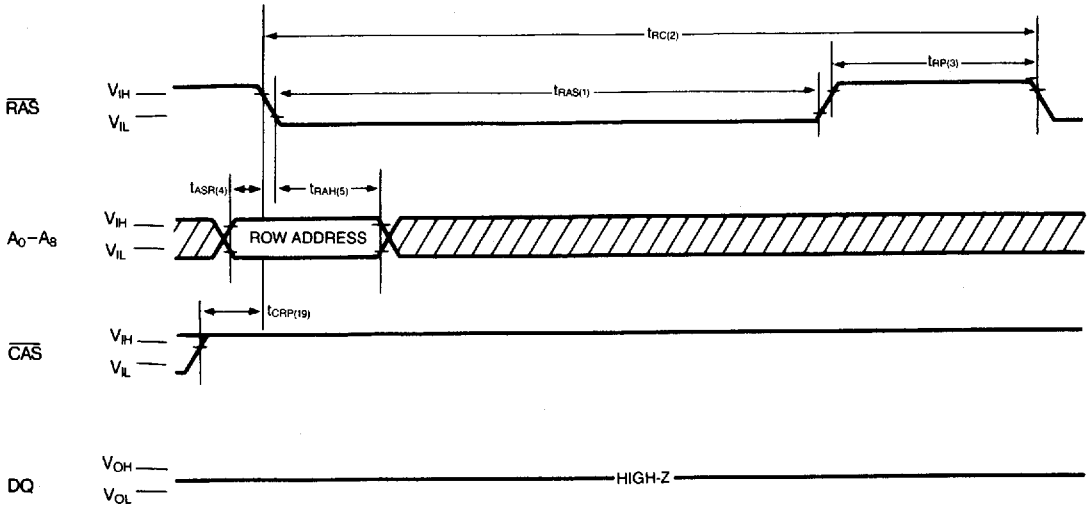
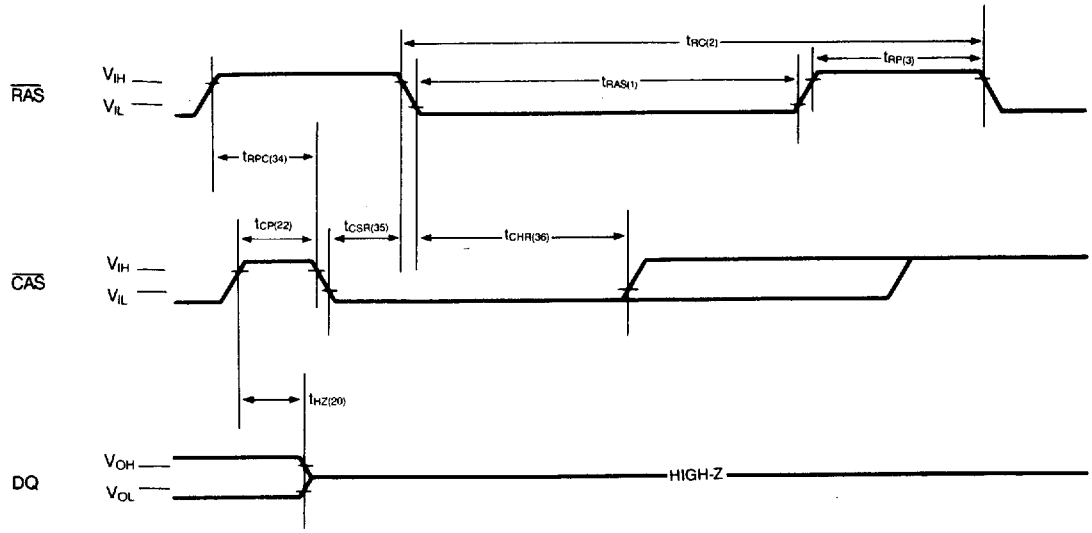
$\overline{RAS}$-ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



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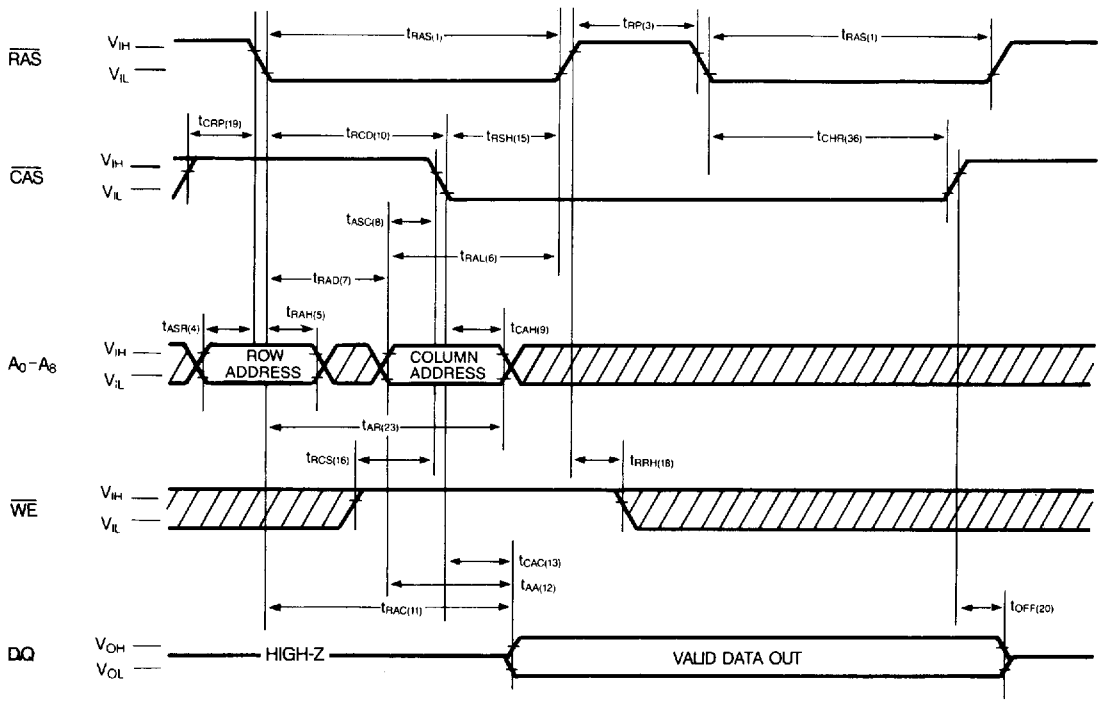
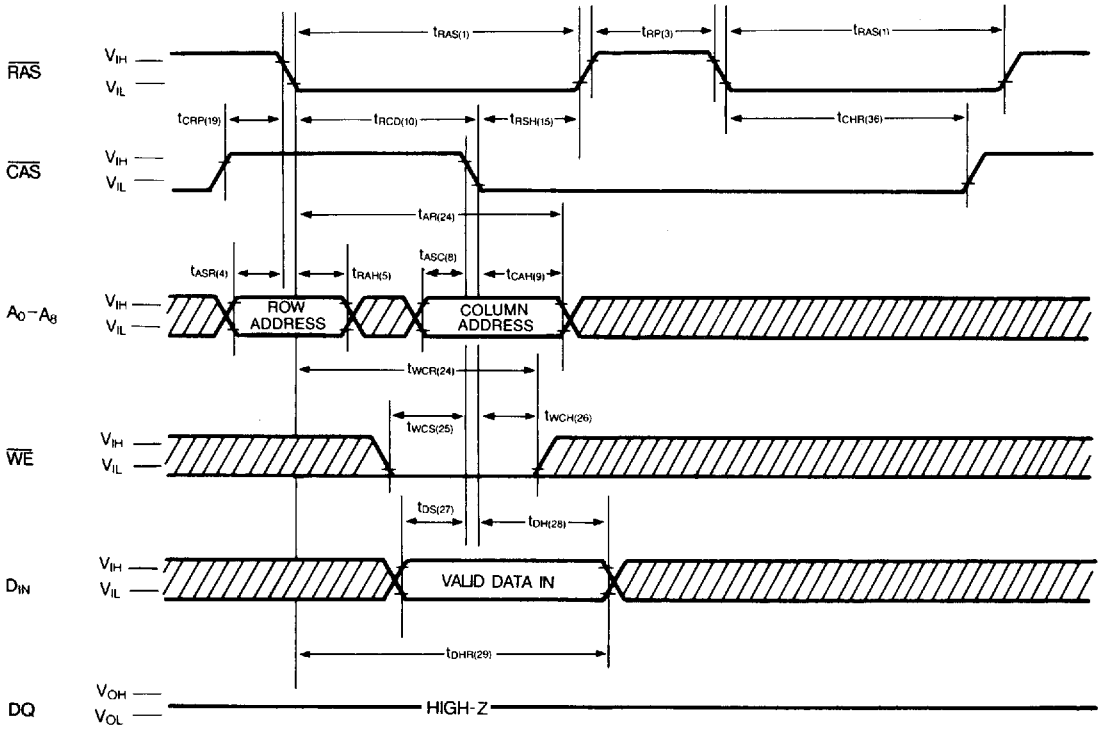
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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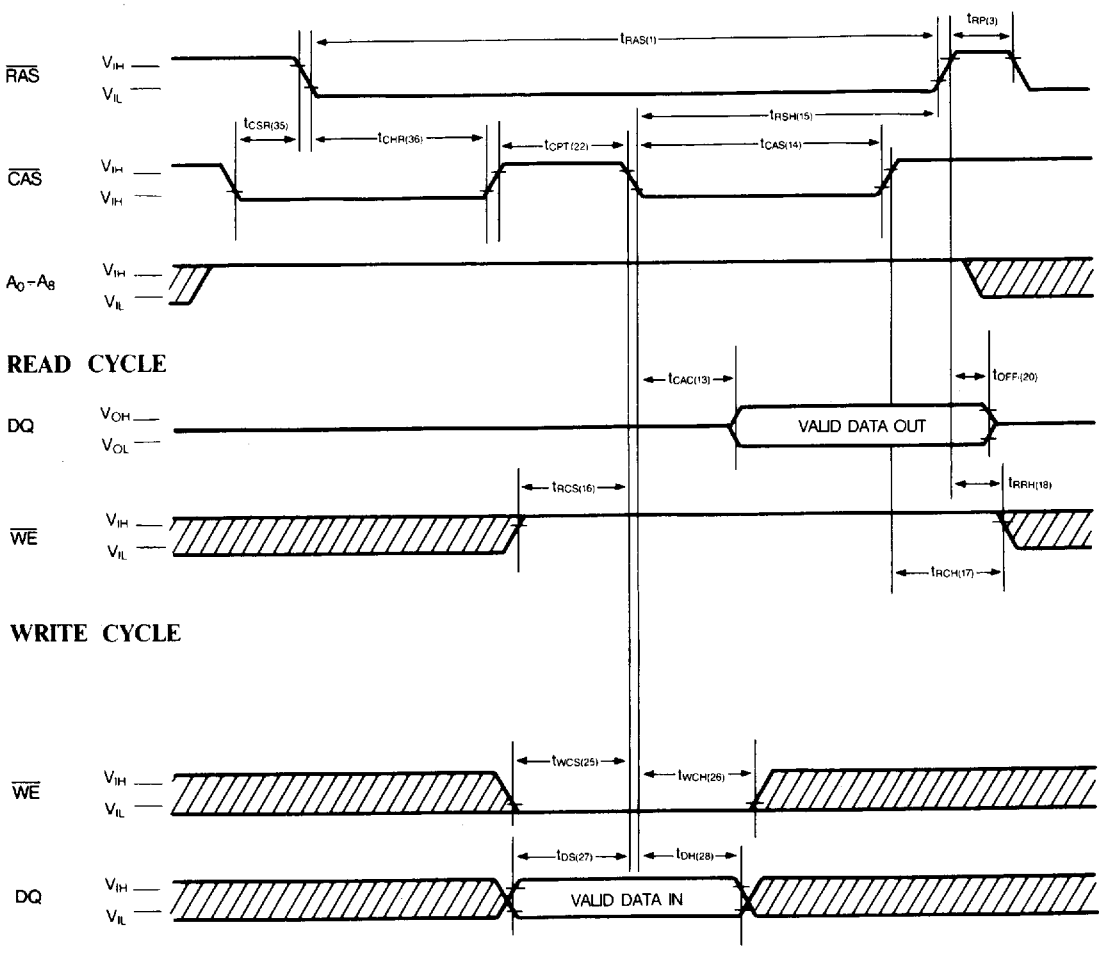
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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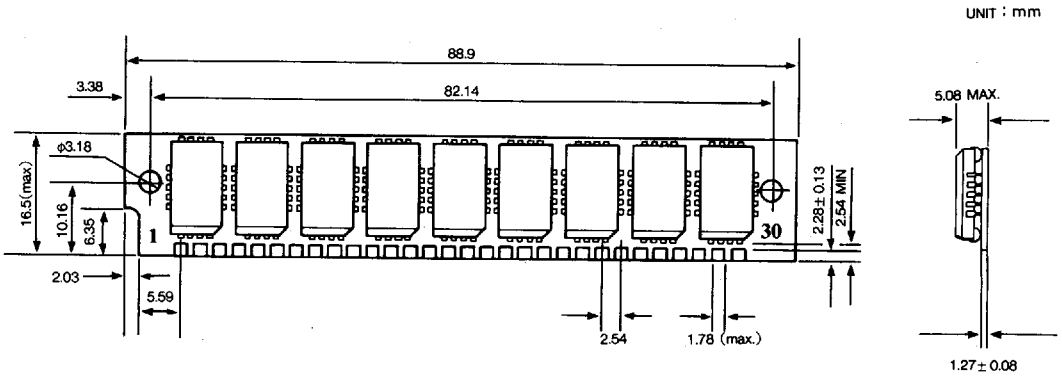
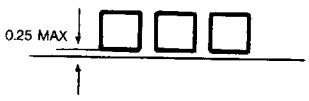
PACKAGE INFORMATION

HYM5C9256M



* DETAIL OF CONTACTS



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