SIEMENS

4M × 32 -Bit EDO-DRAM Module — HYM324025GD-50/-60
SMALL OUTLINE MEMORY MODULE — HYM324025GDL-50/-60

Preliminary Information

- 72-Pin Small Outline Dual-in-Line Memory Module
- 4 0194 034 words by 32-bit organization
- Hyper Page Mode - EDO - performance
- Performance:

		-50	-60	
t_{RAC}	$\overline{RAS}$ access time	50	60	ns
t_{CAC}	$\overline{CAS}$ access time	13	15	ns
t_{AA}	Access time from address	25	30	ns
t_{RC}	Read/Write cycle time	84	104	ns
t_{HPC}	Hyper page mode (EDO) cycle time	20	25	ns

- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation
  max. 2880 mW active (-50 version)
  max. 2592 mW active (-60 version)

  LVTLL - 57.6 mw standby
  LVCMOS– 28.8 mW standby
  LVCMOS– 5.76 mW standby (L-version)
- Low Power Versions with Self Refresh
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only-refresh
- 8 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully LV-TTL compatible
- Utilizes eight 4M × 4 -DRAMs in TSOPII-packages
- Card size 56.69mm x 25.40mm x 3.80 mm
- 12 / 10 Adressing (Row/Column)
- 4096 refresh cycles / 64 ms
- Gold contact pad

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The HYM 324025GD(L) -50/-60 are 16 MByte DRAM 72 pin small outline dual-in-line memory modules organized as 4M x 32, comprising eight HYB3116405BT(L) 4M × 4 EDO-DRAMs in 300 mil wide TSOPII-26/24 - packages mounted together with eight 0.2 µF ceramic decoupling capacitors on a PC board. These modules are optimized for use in byte-write non-parity applications. Each HYB 3116405BT(L) is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

These modules are ideal for portable systems applications where high memory capacity is needed.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 324025GD -50		L-DIM-72-3	50 ns EDO-DRAM module
HYM 324005GD -60		L-DIM-72-3	60 ns EDO-DRAM module
HYM 324025GDL -50		L-DIM-72-3	50 ns EOD-Low Power DRAM module
HYM 324005GDL -60		L-DIM-72-3	60 ns EDO- Low Power DRAM module

Pin Names

A0-A11	Row Address Input
A0-A9	Column Address Inputs
DQ0 - DQ31	Data Input/Output
RAS0, RAS2	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
WE	Read / Write Input
Vcc	Power (+3.3 Volt)
Vss	Ground
PD1 - PD7	Presence Detect Pins
N.C.	No Connection

Presence-Detect Truth Table *):

Module	PD1	PD2	PD3	PD4	PD5	PD6	PD7
HYM 324025GD -50	NC	NC	VSS	NC	VSS	VSS	NC
HYM 324025GD -60	NC	NC	VSS	NC	NC	NC	NC
HYM 324025GDL -50	NC	NC	VSS	NC	VSS	VSS	VSS
HYM 324025GDL -60	NC	NC	VSS	NC	NC	NC	VSS

*) note: PD1...PD4 : configuration
PD5..PD6 : speed
PD7 : refresh mode

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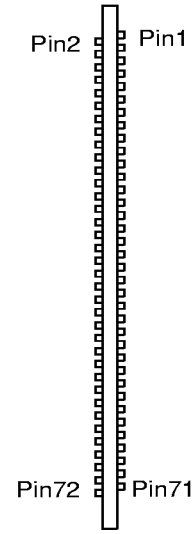
Pin Configuration

PIN	Name	PIN	NAME	PIN	NAME	PIN	NAME
1	VSS	37	DQ16	2	DQ0	38	DQ17
3	DQ1	39	VSS	4	DQ2	40	CAS0
5	DQ3	41	CAS2	6	DQ4	42	CAS3
7	DQ5	43	CAS1	8	DQ6	44	RAS0
9	DQ7	45	NC	10	VCC	46	NC
11	PD1	47	WRITE	12	A0	48	NC
13	A1	49	DQ18	14	A2	50	DQ19
15	A3	51	DQ20	16	A4	52	DQ21
17	A5	53	DQ22	18	A6	54	DQ23
19	A10	55	NC	20	NC	56	DQ24
21	DQ8	57	DQ25	22	DQ9	58	DQ26
23	DQ10	59	DQ28	24	DQ11	60	DQ27
25	DQ12	61	VCC	26	DQ13	62	DQ29
27	DQ14	63	DQ30	28	A7	64	DQ31
29	A11	65	NC	30	VCC	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	NC	69	PD5	34	RAS2	70	PD6
35	DQ15	71	PD7	36	NC	72	VSS
	Front Side				**Back Side**		



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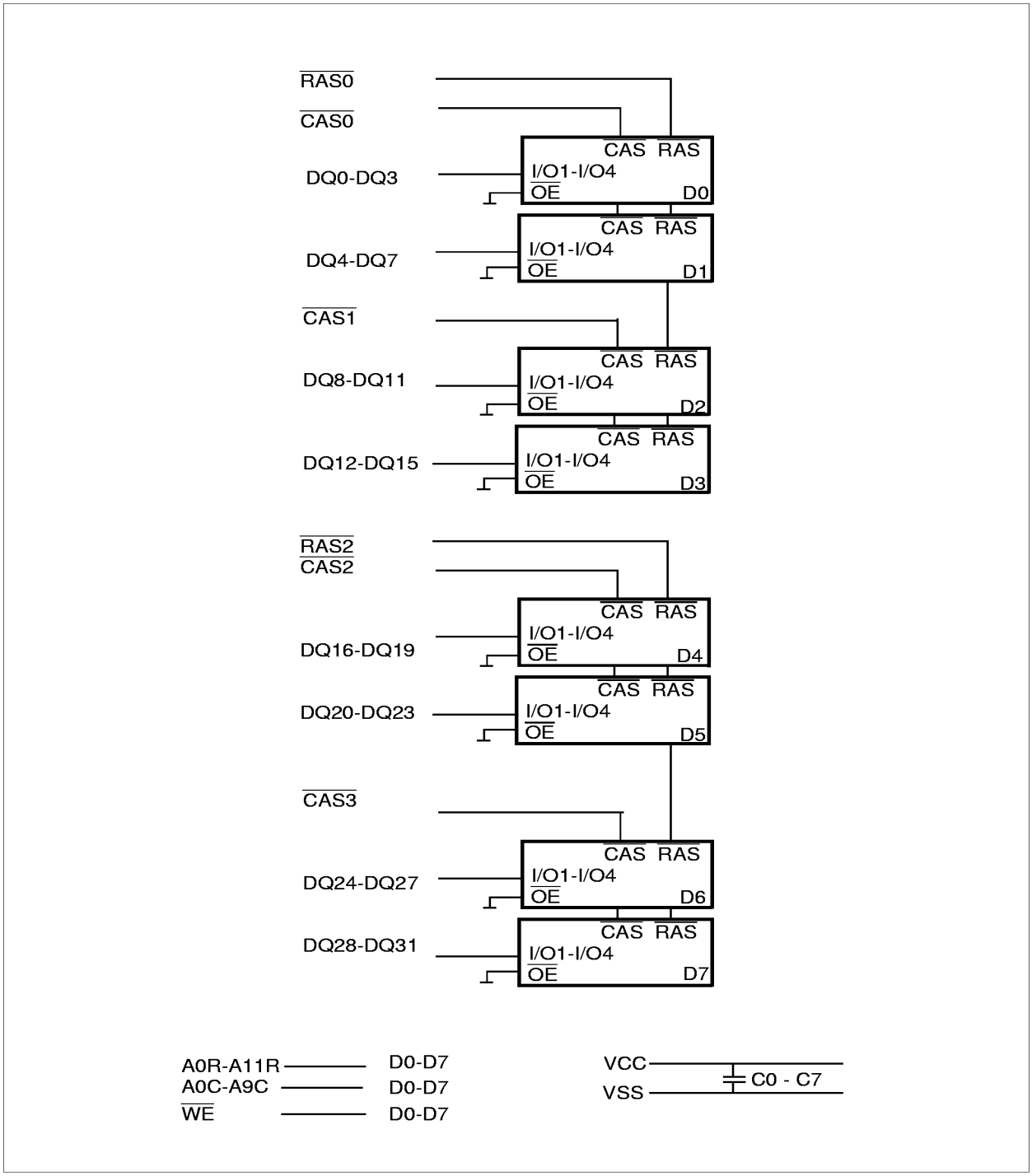

Block Diagram

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Absolute Maximum Ratings

Operating temperature range.....0 to 70 °C
Storage temperature range.....– 55 to 150 °C
Input/output voltage.....-0.5 to min (Vcc+0.5,4.6) V
Power supply voltage.....-0.5V to 4.6 V
Power dissipation.....1.0 W
Data out current (short circuit).....50 mA

DC Characteristics

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1)
Input low voltage	V_{IL}	– 0.3	0.8	V	1)
Output high voltage (LVTTL) Output „H“ level voltage (Iout = -2mA)	V_{OH}	2.4	–	V	1)
Output low voltage (LVTTL) Output „L“level voltage (Iout = +2mA)	V_{OL}	–	0.4	V	1)
Output high voltage (LVCMOS) Output „H“ level voltage (Iout = -100uA)	V_{OH}	Vcc-0.2	-	V	1)
Ouput low voltage (LVCMOS) Output „L“ level voltage (Iout = +100uA)	V_{OL}	-	0.2	V	!)
Input leakage current,any input (0 V < Vin < Vcc , all other pins = 0 V	$I_{I(L)}$	– 10	10	µA	
Output leakage current (DO is disabled, 0 V < $Vout$ < Vcc)	$I_{O(L)}$	– 10	10	µA	
Average Vcc supply current: -50 ns version -60 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling: tRC = tRC min.)	I_{CC1}	 – –	 800 720	 mA mA	 2) 3) 4)
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= Vih)	I_{CC2}	–	16	mA	–
Average Vcc supply current, during RAS-only refresh cycles: -50 ns version -60 ns version (RAS cycling: CAS = VIH: tRC = tRC min.)	I_{CC3}	 – –	 800 720	 mA mA	 2) 3)

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DC Characteristics (cont'd)
T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Average *V*cc supply current, during hyper page mode (EDO):	I_{CC4}				
-50 ns version		–	560	mA	2) 3)
-60 ns version		–	440	mA	4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: tHPC=tHPC min.)					
Standby Vcc supply current ($\overline{RAS}$=$\overline{CAS}$= *V*cc-0.2V)	I_{CC5}	–	8	mA	–
Standby Vcc supply current (L-version) ($\overline{RAS}$=$\overline{CAS}$= *V*cc-0.2V)	I_{CC5}	–	1.6	mA	–
Average Vcc supply current, during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				
-50 ns version		–	800	mA	2) 4)
-60 ns version		–	720	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling: tRC = tRC min.)					
Self Refresh Current (L-version only) $\overline{CBR}$ cycle with $\overline{RAS}$>$t_{RASS(min.)}$; $\overline{CAS}$ held low; $\overline{WE}$=Vcc-0.2V; Addresses and Di=Vcc-0.2V or 0.2V	I_{CC7}	–	2	mA	

Capacitance
T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, *f* = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,$\overline{WE}$)	C_{I1}	–	55	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	40	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	25	pF
I/O capacitance (DQ0-DQ31)	C_{IO}	–	15	pF

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AC Characteristics [5)6)]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ±0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
common parameters							
Random read or write cycle time	t_{RC}	84	–	104	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10k	10	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	8	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	7
Refresh period	t_{REF}	–	64	–	64	ms	
Refresh period for L-version	t_{REF}	–	256	–	256	ms	
Read Cycle							
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	ns	8,10
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	ns	12

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AC Characteristics (cont'd) [5)6)]

T_A = 0 to 70 °C, V_{CC} = 3.3 V ±0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values				Unit	Note
		-50		-60			
		min.	max.	min.	max.		
Early Write Cycle							
Write command hold time	t_{WCH}	8	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	ns	13
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	ns	
Data setup time	t_{DS}	0	–	0	–	ns	14
Data hold time	t_{DH}	8	–	10	–	ns	14
Hyper Page Mode (EDO) Cycle							
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	27	–	32	ns	7
Output data hold time	t_{COH}	5	–	5	–	ns	
$\overline{RAS}$ pulse width in hyper page mode	t_{RAS}	50	200k	60	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHCP}	27	–	32	–	ns	
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle							
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	10	–	ns	

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Notes:

1) All voltages are referenced to V_{SS}.
2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
4) Address can be changed once or less while RAS = Vil. In case of ICC4 it can be changed once or less during a hyper page mode (EDO) cycle
5) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-$\overline{RAS}$ initialization cycles instead of 8 RAS cycles are required.
6) AC measurements assume t_T = 2 ns.
7) $V_{IH\ (min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.
8) Measured with the specified current load and 100 pF at Vol = 0.8 V and Voh = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{AA},t_{CPA}, t_{OEA} . t_{CAC} is measured from tristate.
9) Operation within the $t_{RCD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RCD\ (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\ (max.)}$ limit, then access time is controlled by t_{CAC}.
10) Operation within the $t_{RAD\ (max.)}$ limit ensures that $t_{RAC\ (max.)}$ can be met. $t_{RAD\ (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\ (max.)}$ limit, then access time is controlled by t_{AA}.
11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12) $t_{OFF\ (max.)}$, $t_{OEZ\ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
13) Either t_{DZC} or t_{DZO} must be satisfied.
14) Either t_{CDD} or t_{ODD} must be satisfied.
15) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min.)}$, $t_{CWD} > t_{CWD\ (min.)}$ and $t_{AWD} > t_{AWD\ (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh

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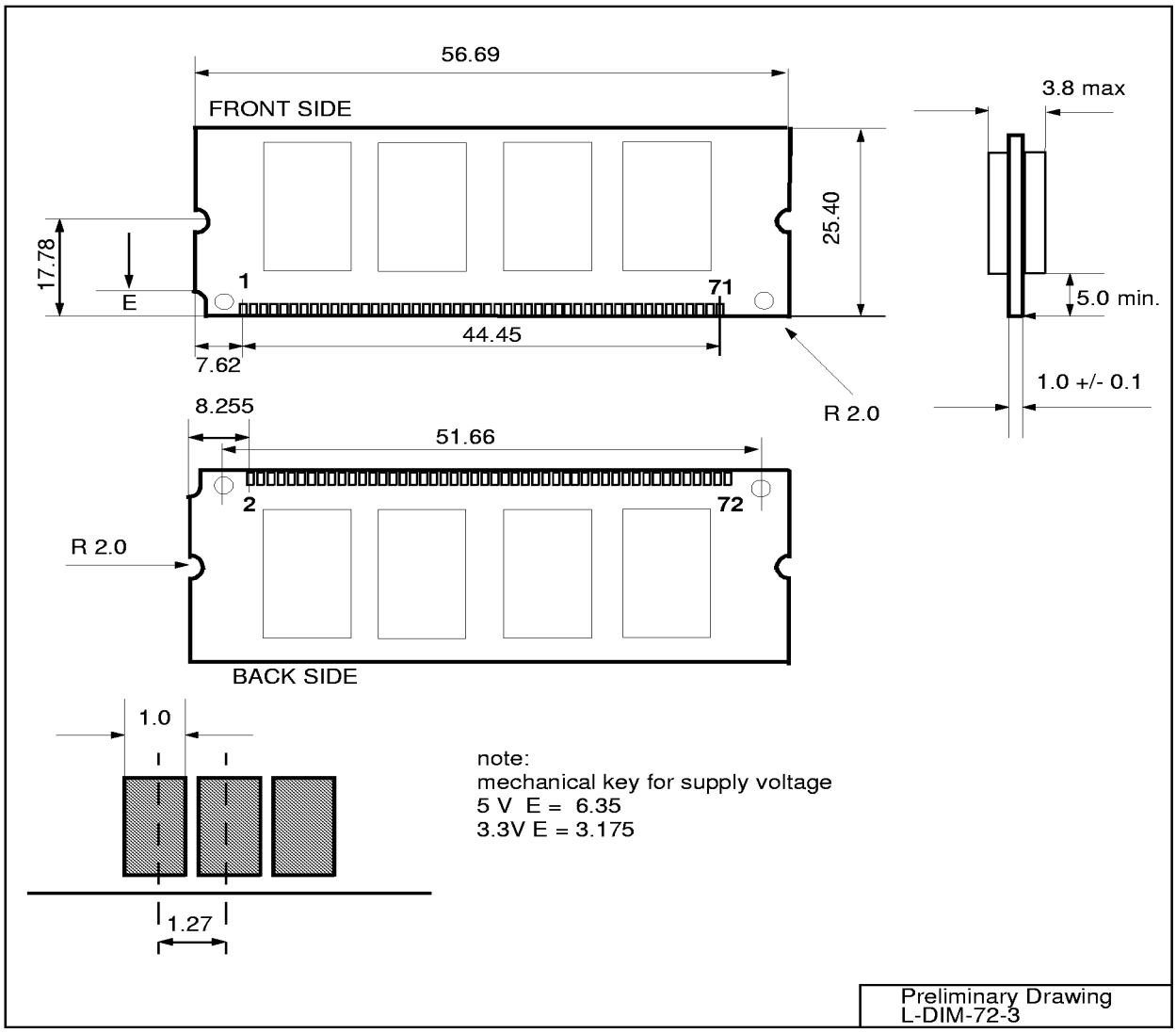
SO-DIMM PACKAGE OUTLINES



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