

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 4-channel 12-bit analog-to-digital converter which uses the successive approximation technique to provide a conversion time of 100 μ s per channel. Conversion results are available in two bytes, 8LSBs and 4MSBs, via an 8-bit three-state output bus.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
- 1	AD7582T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin Ceramic
E	E-28A	28-Contact LCC
Q	Q-28	28-Pin Cerdip

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND	-0.3V, +17V
V_{SS} to DGND	+0.3V, -7V
AGND to DGND	-0.3V, $V_{REF} + 0.3V$
V_{CC} to DGND	-0.3V, $V_{DD} + 0.3V$
V_{REF} to AGND	-0.3V, $V_{DD} + 0.3V$
AIN (0-3) to AGND	-0.3V, $V_{DD} + 0.3V$
Digital Input Voltage to DGND (Pins 18-21, 23-25)	-0.3V, $V_{DD} + 0.3V$
Digital Output Voltage to DGND (Pins 10-17, 22)	-0.3V, $V_{DD} + 0.3V$
Power Dissipation	
Up to $+75^\circ\text{C}$	1000mW
Derates above $+75^\circ\text{C}$	10mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C}/\text{W}$ for D-28, E-28A and Q-28.

$\theta_{JA} = 120^\circ\text{C}/\text{W}$ for D-28, E-28A and Q-28.

AD7582—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ^{1, 2}	Units
Resolution	RES	- 1	12				Bits
Total Unadjusted Error ³	TUE	- 1	1	1	1	All Channels, AIN0-AIN3	± LSB max
Differential Nonlinearity	DNL	- 1	1	1	1	No Missing Codes Guaranteed	± LSB max
Gain Error	AE	- 1	1/4	1/4	1/4	All Channels, AIN0-AIN3 Gain Error TC is 5ppm/°C typ.	± LSB max
Offset Error	V _{OS}	- 1	1/4	1/4	1/4	All Channels, AIN0-AIN3 Offset Error TC is 5ppm/°C typ.	± LSB max
Channel-to-Channel Mismatch	CCM	- 1	1/4				± LSB max
Analog Input Range	V _{IN}	- 1	0 5				V min V max
Input Leakage Current	I _{LIN}	- 1	100	10	100	AIN0-AIN3; 0 to +5V	nA max
Reference Voltage Range	V _{REF}	- 1	4 6			Degraded Transfer Accuracy	V min V max
V _{REF} Input Reference Current	I _{REF}	- 1	1	1	1		mA max
Digital Input High Level	V _{IH}	- 1	2.4	2.4	2.4	RD (Pin 18), CS (Pin 19) WR (Pin 20), BYSL (Pin 21) A0 (Pin 24), A1 (Pin 25)	V min
Digital Input Low Level	V _{IL}		0.8	0.8	0.8		V max
Digital Input Leakage Current ⁴	I _{IN}		10	1	10		± µA max
Digital Input Capacitance	C _{IN}		10				pF max
Digital Input High Level	V _{IH}	- 1	3.0	3.0	3.0	CLK (Pin 23)	V min
Digital Input Low Level	V _{IL}		0.8	0.8	0.8		V max
Digital Input Low Current	I _{IL}		10	10	10		± µA max
Digital Input High Current	I _{IH}		1.5	1.5	1.5		
Digital Output High Voltage ⁵	V _{OH}	- 1	4.0	4.0	4.0	V _{CC} = +4.75V, I _{SOURCE} = 200µA DB0-DB7 (Pin 10-17), BUSY (Pin 22)	V min
Digital Output Low Voltage ⁵	V _{OL}	- 1	0.4	0.4	0.4	V _{CC} = +5.25V, I _{SINK} = 1.6mA DB0-DB7 (Pin 10-17), BUSY (Pin 22)	V max
Floating State Leakage Current		- 1	1	1	1	DB0-DB7 (Pin 10-17) V _{OUT} = 0V and V _{CC}	± µA max
Floating State Output Capacitance	C _{OUT}	- 1	15				pF max
Conversion Time with External Clock ⁶		- 1	100	100	100	f _{CLK} = 140kHz	µs min
Conversion Time with Internal Clock at +25°C		- 1	100 150	100 150		Using Recommended Clock Circuit Shown in Figure 5.	µs min µs max
Supply Current ⁷	I _{DD}	- 1	7.5	7.5	7.5		mA max
Supply Current ⁷	I _{SS}	- 1	7.5	7.5	7.5		mA max
Supply Current ⁷	I _{CC}	- 1	1.0	1.0	1.0	V _{IN} = V _{IL} or V _{IH}	mA max
CS to WR Setup Time	t ₁	- 1	0				ns min
WR Pulse Width (Internal Clock Operation)	t ₂ (INT)	- 1	280			(200ns min at +25°C)	ns min
WR Pulse Width (External Clock Operation) ⁸	t ₂ (EXT)	- 1	10				ns min
CS to WR Hold Time	t ₃	- 1	0				ns min
WR to BUSY Propagation Delay	t ₄	- 1	300			(100ns max at +25°C)	ns max
A0, A1 Valid to WR Setup Time	t ₅	- 1	0				ns min
A0, A1 Valid to WR Hold Time	t ₆	- 1	20				ns min
BUSY to CS Setup Time	t ₇	- 1	0				ns min
CS to RD Setup Time	t ₈	- 1	0				ns min

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ^{1,2}	Units
BSYL to $\overline{RD}$ Hold Time	t_{12}	-1	0				ns min
$\overline{RD}$ to Valid Data (Bus Access Time) ⁹	t_{13}	-1	280			(150ns max at +25°C)	ns max
$\overline{RD}$ to Three-State Output (Bus Relinquish Time) ¹⁰	t_{14}	-1	20			(130ns max at +25°C)	ns min
			180				ns max

NOTES

¹ $V_{DD} = +15V$; $V_{CC} = +5V$; $V_{SS} = -5V$; $V_{REF} = +5V$; $f_{CLK} = 140kHz$ external.

²All input control signals are specified with $t_r = t_f = 20ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is time from V_{IH} , V_{IL} or V_{OH} , V_{OL} .

³Includes full scale error, offset error and relative accuracy.

⁴Digital inputs = 0V or +5V.

⁵ I_{SDRV} for Busy (Pin 22) is 1.0mA.

⁶Conversion time includes auto-zero cycle time.

⁷Power supply current is measured when the AD7582 is inactive i.e., $\overline{WR} = \overline{RD} = \overline{BSY} = \text{LOGIC HIGH}$.

⁸When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10 μs (see External Clock Operation).

⁹ t_{13} is defined as the time required for an output to cross 0.8V or 2.4V and is measured with the load circuits of Figure 3.

¹⁰ t_{14} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.

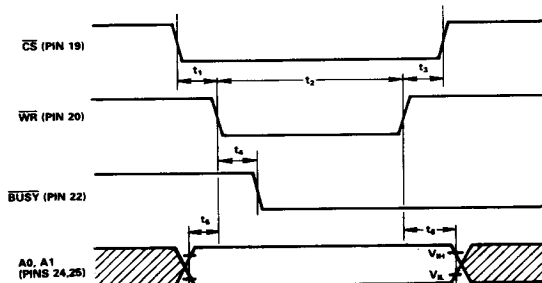
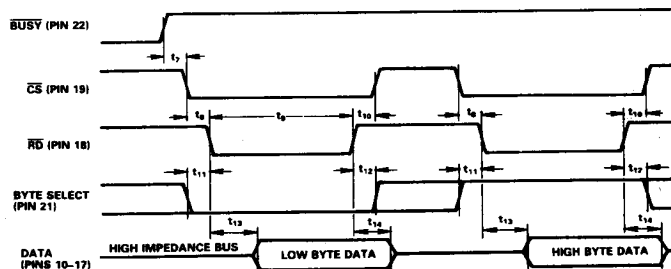
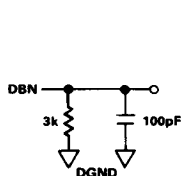


Figure 1. Start Cycle Timing

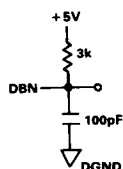


NOTES
THE TWO-BYTE CONVERSION RESULT CAN BE READ IN EITHER ORDER. FIGURE IS FOR LOW BYTE, HIGH BYTE ORDER.
IF BSYL CHANGES WHILE CS & RD ARE LOW THE DATA WILL CHANGE TO REFLECT THE BSYL INPUT.

Figure 2. Read Cycle Timing

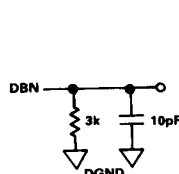


a. High-Z to V_{OH}

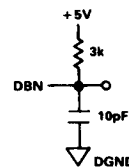


b. High-Z to V_{OL}

Figure 3. Load Circuits for Access Time Test (t_{13})



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 4. Load Circuits for Output Float Delay Test (t_{14})

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 5 and the AD7582 operating waveforms are shown in Figure 6.

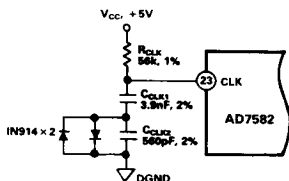


Figure 5. Circuitry Required for Internal Clock Operation

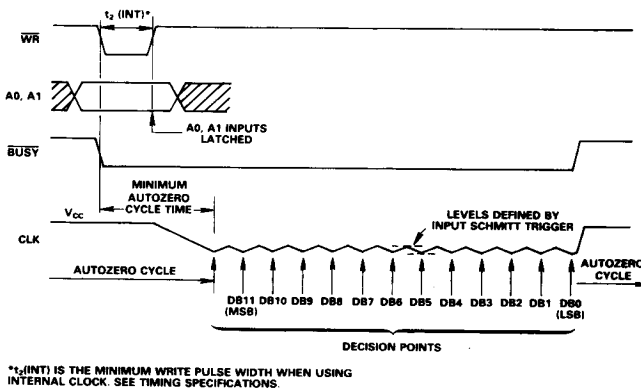


Figure 6. Operating Waveforms - Internal Clock

Between conversions ($\overline{\text{BUSY}} = \text{HIGH}$) the AD7582 is in the autozero cycle. When $\overline{\text{WR}}$ goes LOW (with $\overline{\text{CS}}$ LOW) to start a new conversion, the input multiplexer is switched to the selected channel N, via address inputs A0, A1. The autozero capacitor C_{AZ} now charges to $A_{IN} N - V_{OS}$ where V_{OS} is the input offset voltage of the autozero comparator.

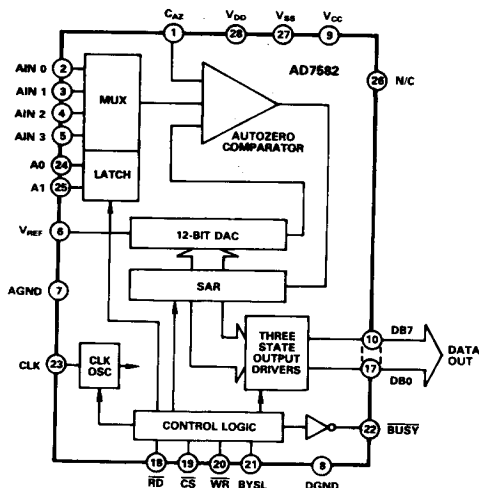
A minimum time of $10\mu\text{s}$ is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{\text{WR}}$ to remain LOW for this period of time since it is automatically provided by the AD7582. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2} , causing the voltage at the CLK input pin to slowly decay from V_{CC} . This occurs after $\overline{\text{WR}}$ returns HIGH; $\overline{\text{WR}}$ returning HIGH also latches the multiplexer address inputs A0, A1 (see Figure 6). The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK} . When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2} . The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 5 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

For external clock operation R_{CLK} , C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The AD7582 $\overline{WR}$ pulse width must now be extended to provide the minimum autozero cycle time of $10\mu s$ since this is no longer provided automatically by the AD7582. Referring to the operating waveforms of Figure 8, the minimum $\overline{WR}$ pulse width when using an external clock source is t_2 (EXT). Multiplexer address inputs A0 and A1, in addition to the $\overline{CS}$ input must now remain valid for the external $\overline{WR}$ pulse width. One approach to stretching the available μP signals is shown in the general 8-bit μP interface circuit of Figure 9. It is not necessary to synchronize the external clock source with the extended $\overline{WR}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{WR}$ input returns HIGH.

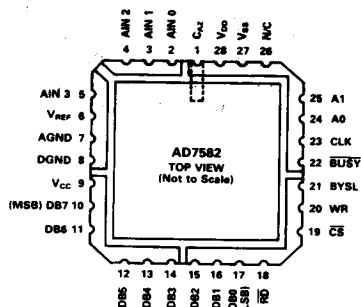


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3.2.1 Functional Block Diagram and Terminal Assignments.



E Package (LCC)

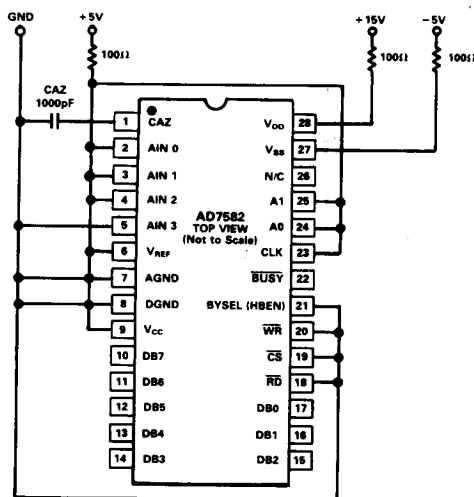


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ALL RESISTORS FOR PROTECTION ONLY
POWER μ P SEQUENCE: +15, +5, -5 IN THAT ORDER
-OR SIMULTANEOUSLY.