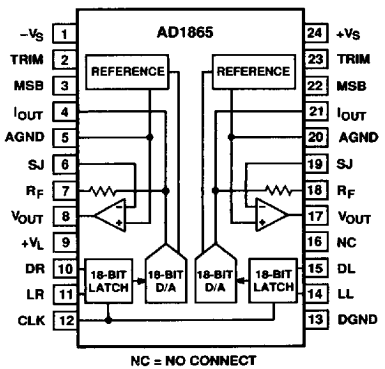
# Complete Dual 18-Bit 16 × $F_S$ Audio DAC

# AD1865*

**FEATURES**
**Dual Serial Input, Voltage Output DACs**
**No External Components Required**
**110 dB SNR**
**0.003% THD+N**
**Operates at 16 × Oversampling per Channel**
**±5 Volt Operation**
**Cophased Outputs**
**116 dB Channel Separation**
**Pin Compatible with AD1864**
**DIP or SOIC Packaging**

**APPLICATIONS**
**Multichannel Audio Applications:**
**Compact Disc Players**
**Multivoice Keyboard Instruments**
**DAT Players and Recorders**
**Digital Mixing Consoles**
**Multimedia Workstations**

**FUNCTIONAL BLOCK DIAGRAM**
**(DIP Package)**




NC = NO CONNECT

## PRODUCT DESCRIPTION

The AD1865 is a complete, dual 18-bit DAC offering excellent THD+N and SNR while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1865 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices' ABCMOS process.

The DACs on the AD1865 chip employ a partially segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1865 provides two ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1865 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout. At the same time, both channels of the AD1865 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

***Protected by U.S. Patents Nos.: RE 30,586; 3,961,326; 4,141,004; 4,349,811; 4,855,618. 4,857,862.**

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

A versatile digital interface allows the AD1865 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1865 operates with ±5 V power supplies. The digital supply, $V_L$, can be separated from the analog supplies, $V_S$ and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1865 typically dissipates only 225 mW, with a maximum power dissipation of 260 mW.

The AD1865 is packaged in both a 24-pin plastic DIP and a 28-pin SOIC package. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

## PRODUCT HIGHLIGHTS

1. The AD1865 is a Complete Dual 18-Bit Audio DAC.
2. 110 dB Signal-To-Noise Ratio for low noise operation.
3. THD+N is typically 0.003%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 16 × $F_S$.
8. Low Power—only 225 mW typ, 260 mW max.
9. Five-wire interface for individual DAC control.
10. 24-pin DIP or 28-pin SOIC packages available.





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# AD1865—SPECIFICATIONS ($T_A$ = +25°C, $+V_L$ = $+V_S$ = +5 V and $-V_S$ = −5 V, $F_S$ = 705.6 kHz, no MSB adjustment or deglitcher)

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | | 18 | | Bits |
| DIGITAL INPUTS | $V_{IH}$ | 2.0 | | $+V_L$ | V |
| | $V_{IL}$ | | | 0.8 | V |
| | $I_{IH}$, $V_{IH}$ = $+V_L$ | | | 1.0 | μA |
| | $I_{IL}$, $V_{IL}$ = 0.4 V | | | −10 | μA |
| Clock Input Frequency | | 13.5 | | | MHz |
| ACCURACY | | | | | |
| Gain Error | | | 0.2 | 1.0 | % of FSR |
| Interchannel Gain Matching | | | 0.3 | 0.8 | % of FSR |
| Midscale Error | | | 4 | | mV |
| Interchannel Midscale Matching | | | 5 | | mV |
| Gain Linearity (0 dB to −90 dB) | | | <2 | | dB |
| DRIFT (0°C to +70°C) | | | | | |
| Gain Drift | | | ±25 | | ppm of FSR/°C |
| Midscale Drift | | | ±4 | | ppm of FSR/°C |
| TOTAL HARMONIC DISTORTION + NOISE* | | | | | |
| 0 dB, 990.5 Hz | AD1865N, R | | 0.004 | 0.006 | % |
| | AD1865N-J, R-J | | 0.003 | 0.004 | % |
| −20 dB, 990.5 Hz | AD1865N, R | | 0.010 | 0.040 | % |
| | AD1865N-J, R-J | | 0.010 | 0.020 | % |
| −60 dB, 990.5 Hz | AD1865N, R | | 1.0 | 4.0 | % |
| | AD1865N-J, R-J | | 1.0 | 2.0 | % |
| CHANNEL SEPARATION* | | | | | |
| 0 dB, 990.5 Hz | | 110 | 116 | | dB |
| SIGNAL-TO-NOISE RATIO* (20 Hz to 30 kHz) | | 107 | 110 | | dB |
| D-RANGE* (with A-Weight Filter) | | | | | |
| −60 dB, 990.5 Hz | AD1865N, R | 88 | 100 | | dB |
| | AD1865N-J, R-J | 94 | 100 | | dB |
| OUTPUT | | | | | |
| Voltage Output Configuration | | | | | |
| Output Range (±1%) | | ±2.94 | ±3.0 | ±3.06 | V |
| Output Impedance | | | 0.1 | | Ω |
| Load Current | | ±8 | | | mA |
| Short Circuit Duration | | | Indefinite to Common | | |
| Current Output Configuration | | | | | |
| Bipolar Output Range (±30%) | | | ±1 | | mA |
| Output Impedance (±30%) | | | 1.7 | | kΩ |
| POWER SUPPLY | | | | | |
| $+V_L$ and $+V_S$ | | 4.75 | 5.0 | 5.25 | V |
| $-V_S$ | | −5.25 | −5.0 | −4.75 | V |
| +I, $+V_L$ and $+V_S$ = +5 V | | | 22 | 26 | mA |
| −I, $-V_S$ = −5 V | | | −23 | −26 | mA |
| POWER DISSIPATION, $+V_L$ = $+V_S$ = +5 V, $-V_S$ = −5 V | | | 225 | 260 | mW |
| TEMPERATURE RANGE | | | | | |
| Specification | | 0 | +25 | +70 | °C |
| Operation | | −25 | | +70 | °C |
| Storage | | −60 | | +100 | °C |
| WARMUP TIME | | 1 | | | min |

Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.
*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.
Specifications subject to change without notice.



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**ABSOLUTE MAXIMUM RATINGS***

| | |
|---|---|
| $V_L$ to DGND | 0 to 6.0 V |
| $V_S$ to AGND | 0 to 6.0 V |
| $-V_S$ to AGND | −6.0 to 0 V |
| AGND to DGND | ±0.3 V |
| Digital Inputs to DGND | −0.3 to $V_L$ |
| Short Circuit Protection | Indefinite Short to Ground |
| Soldering | 300°C, 10 sec |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.


**ORDERING GUIDE**

| Model | Temperature Range | THD+N @ FS | Package Option* |
|---|---|---|---|
| AD1865N | −25°C to +70°C | 0.006% | N-24A |
| AD1865N-J | −25°C to +70°C | 0.004% | N-24A |
| AD1865R | −25°C to +70°C | 0.006% | R-28 |
| AD1865R-J | −25°C to +70°C | 0.004% | R-28 |

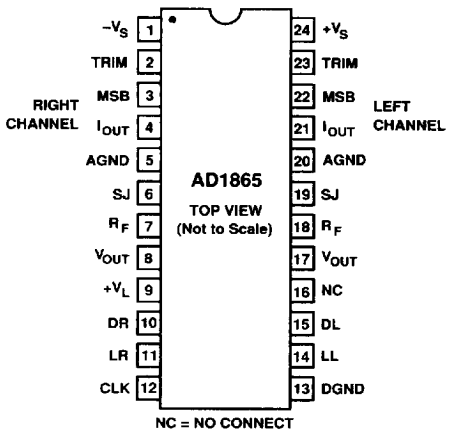
*N = Plastic DIP, R = Small Outline IC Package. For outline information see Package Information section.

**PIN DESIGNATIONS**

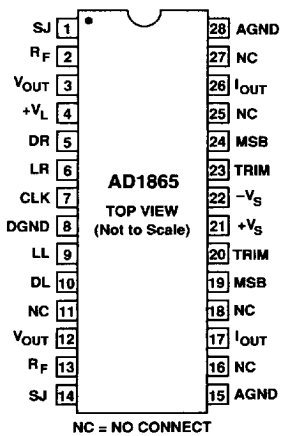
| DIP | SOIC | | |
|---|---|---|---|
| 1 | 22 | $-V_S$ | Negative Analog Supply |
| 2 | 23 | TRIM | Right Channel Trim Network Connection |
| 3 | 24 | MSB | Right Channel Trim Potentiometer Wiper Connection |
| 4 | 26 | $I_{OUT}$ | Right Channel Output Current |
| 5 | 28 | AGND | Analog Common Pin |
| 6 | 1 | SJ | Right Channel Amplifier Summing Junction |
| 7 | 2 | $R_F$ | Right Channel Feedback Resistor |
| 8 | 3 | $V_{OUT}$ | Right Channel Output Voltage |
| 9 | 4 | $+V_L$ | Positive Digital Supply |
| 10 | 5 | DR | Right Channel Data Input Pin |
| 11 | 6 | LR | Right Channel Latch Pin |
| 12 | 7 | CLK | Clock Input Pin |
| 13 | 8 | DGND | Digital Common Pin |
| 14 | 9 | LL | Left Channel Latch Pin |
| 15 | 10 | DL | Left Channel Data Input Pin |
| 16 | 11, 16, 18 25, 27 | NC | No Internal Connection* |
| 17 | 12 | $V_{OUT}$ | Left Channel Output Voltage |
| 18 | 13 | $R_F$ | Left Channel Feedback Resistor |
| 19 | 14 | SJ | Left Channel Amplifier Summing Junction |
| 20 | 15 | AGND | Analog Common Pin |
| 21 | 17 | $I_{OUT}$ | Left Channel Output Current |
| 22 | 19 | MSB | Left Channel Trim Potentiometer Wiper Connection |
| 23 | 20 | TRIM | Left Channel Trim Network Connection |
| 24 | 21 | $+V_S$ | Positive Analog Supply |

*Pin 16 has no internal connection; $-V_L$ from AD1864 DIP socket can be safely applied.

**PINOUT**
**(24-Pin DIP Package)**




**(28-Pin SOIC Package)**

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