Features

- PC603e™ Microprocessor (Embedded PowerPC™ Core) at 133 - 300 MHz
  - 280 MIPS at 200 MHz (Dhrystone 2.1)
  - 520 MIPS at 300 MHz (Dhrystone 2.1)
  - High-performance, Superscalar Microprocessor
  - Disable CPU Mode
  - Improved Low-power Core
  - 16-Kbyte Data and 16-Kbyte Instruction Cache, Four-way Set Associative
  - Memory Management Unit (MMU)
  - Floating Point Unit (FPU)
  - Common On-chip Processor (COP)
- Two Bus Architectures: One 64-bit PowerPC and One 32-bit PCI or Local Bus
- System Integration Unit (SIU)
  - Memory Controller, Including Two Dedicated SDRAM Machines
  - PCI up to 66 MHz
  - Hardware Bus Monitor and Software Watchdog Timer
  - IEEE 1149.1 JTAG Test Access Port
- High-performance Communications Processor Module (CPM)
  - CPM Frequency Up to 200 MHz
  - PowerPC and CPM May Run at Different Frequencies
  - Parallel I/O Registers
  - On-board 32 KBytes of Dual-port RAM
  - Two Multi-channel Controllers (MCCs) Each Supporting 128 Full-duplex, 64-Kbps, HDLC Lines
  - Virtual DMA Functionality
  - 3 FCCs Supporting:
    - Up to 155 Mbps ATM SAR, Maximum of Two (AAL0, AAL1, AAL2, AAL5)
    - 10/100 Mbps Ethernet, Up to Three (IEEE 802.3X with Flow Control)
    - 45 Mbps HDLC/Transparent (Up to Three)
- Two UTOPIA Level-2 Master/Slave Ports, Both with Multi-PHY Support. One Can Support 8/16 bit Data
- Three MII Interfaces
- Eight TDM Interfaces (T1/E1), Two TDM Ports Can Be Glueless to T3/E3
- Power Consumption: 2.5W at 300 MHz

Description

The PC8265A PowerQUICC II™ is a versatile communications processor that integrates on one chip, a high-performance PowerPC (PC603e) RISC microprocessor, a highly flexible system integration unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the PC603e microprocessor, specifically referred to later in this document as the EC603e, with 16 Kbytes of instruction cache and 16 Kbytes of data cache and floating-point unit (FPU). The system interface unit (SIU) consists of a flexible memory controller that interfaces to almost any user-defined memory system, a 60x-to-PCI bus bridge and many other peripherals, making this device a complete system on a chip.

The communications processor module (CPM) includes all the peripherals found in the PC860, with the addition of three high-performance communication channels that support new emerging protocols (for example, 155-Mbps ATM and Fast Ethernet).

Equipped with dedicated hardware, the PC8265A can handle up to 256 full-duplex, time-division, multiplexed logical channels.

PowerPC™-based Communications Processor

PC8265A

PowerQUICC II™ Preliminary Specification Alpha Site

5336A–HIREL–08/03

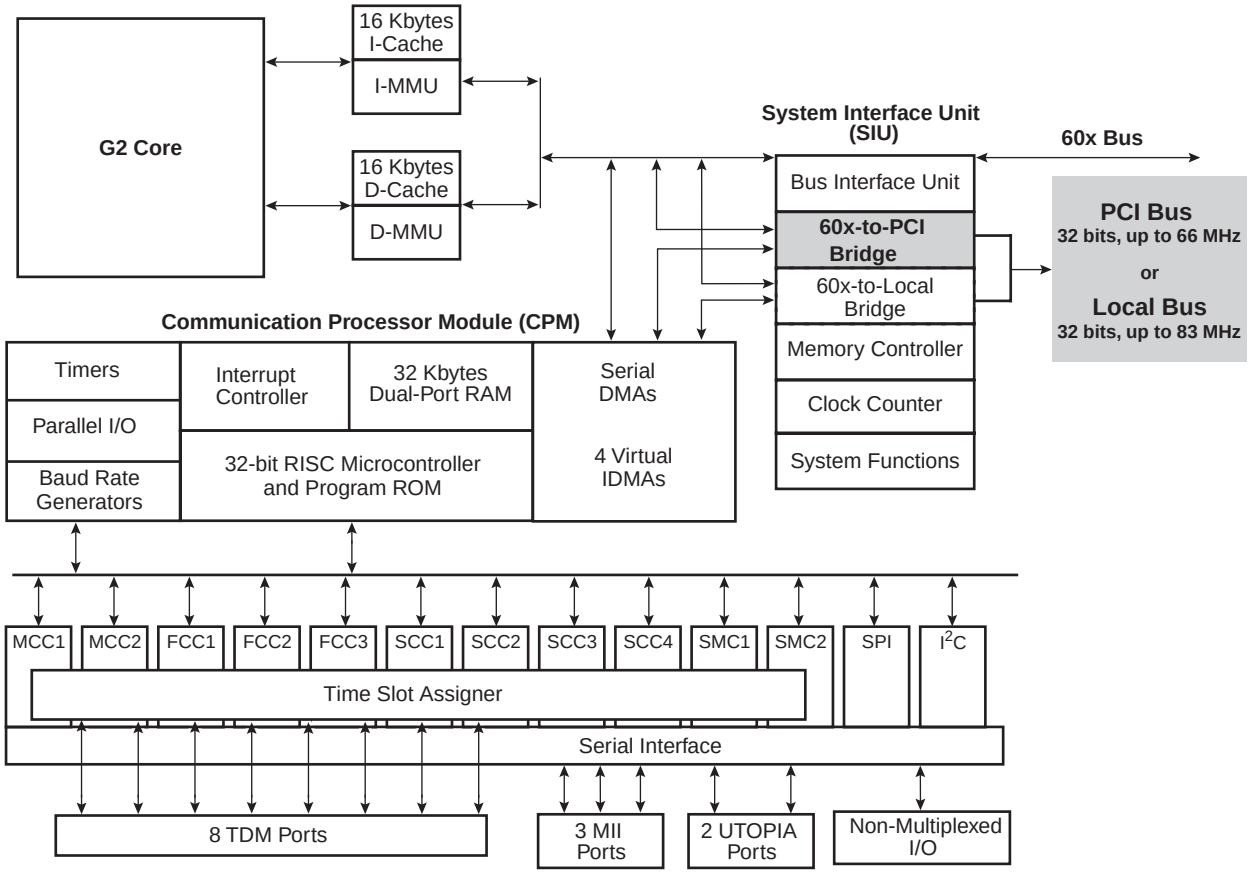
Screening Quality Packaging

This product is manufactured in full compliance with:

- Upscreening based upon Atmel standards
- Military temperature range (T_C = -55°C, T_C = +125°C)
- 480-ball Tape Ball Grid Array package (TBGA 37.5 x 37.5 mm)

PC8265A Architecture General Overview

Figure 1. PC8265A Block Diagram



Features

The major features of the PC8265A family are as follows:

- Dual-issue integer core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 150 – 300 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - PowerPC architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface

High-performance (6.6 - 7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPs/MHz without inlining and 1.90 Dhrystones MIPS/MHz with inlining)

Supports bus snooping for data cache coherency

Floating-point unit (FPU)

- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM

  G2 core and CPM can run at different frequencies for power/performance optimization

  Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios

  Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus

  Bus supports multiple master designs

  Supports single- and four-beat burst transfers

  64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller

  Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus

  Single-master bus, supports external slaves

  Eight-beat burst transfers

  32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge

  Programmable host bridge and agent

  32-bit data bus, 66 MHz, 3.3V

  Synchronous and asynchronous 60x and PCI clock modes

  All internal address space available to external PCI host

  DMA for memory block transfers

  PCI-to-60x address remapping
- System interface unit (SIU)

  Clock synthesizer

  Reset controller

  Real-time clock (RTC) register

  Periodic interrupt timer

  Hardware bus monitor and software watchdog timer

  IEEE 1149.1 JTAG test access port
- Twelve-bank memory controller

  Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals

  Byte write enables and selectable parity generation

  32-bit address decoder with programmable bank size

  Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine

  Byte selects of 64 bus width (60x) and byte selects for 32 bus width (local)

  Dedicated interface logic for SDRAM

- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)

  Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support of communications protocols

  Interfaces to G2 core through an on-chip 32-Kbyte dual-port RAM and DMA controller

  Serial DMA channels for receive and transmit on all serial channels

  Parallel I/O registers with open-drain and interrupt capability

  Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers

  Three fast communications controllers supporting the following protocols:
  - 10/100-Mbit Ethernet/IEEE 802.3 CDMA/CS interface through a media independent interface (MII)
  - ATM – Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
  - Transparent
  - HDLC – Up to T3 rates (clear channel)

  Two multichannel controllers (MCCs)
  - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each
  - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC

  Four serial communications controllers (SCCs) identical to those on the PC860, supporting the digital portions of the following protocols:
  - Ethernet/IEEE 802.3 CDMA/CS
  - HDLC/SDLC and HDLC bus
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Binary synchronous (BISYNC) communications
  - Transparent

  Two serial management controllers (SMCs), identical to those of the PC860
  - Provides management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
  - Transparent
  - UART (low-speed operation)

  One serial peripheral interface identical to the PC860 SPI

  One inter-integrated circuit (I2C) controller (identical to the PC860 I2 C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes

  Up to eight TDM interfaces
  - Supports two groups of four TDM channels for a total of eight TDMs
  - 2,048 bytes of SI RAM
  - Bit or byte resolution

  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Motorola interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces

  Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels

  Four independent 16-bit timers that can be interconnected as two 32-bit timers

- CPM

  32-Kbyte dual-port RAM

  Additional MCC host commands

- CPM multiplexing

  FCC2 can also be connected to the TC layer

- PCI bridge

  PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz

  On-chip arbitration

  Support for PCI to 60x memory and 60x memory to PCI streaming

  PCI Host Bridge or Peripheral capabilities

  Includes 4 DMA channels for the following transfers:

  - PCI-to-60x to 60x-to-PCI
  - 60x-to-PCI to PCI-to-60x
  - PCI-to-60x to PCI-to-60x
  - 60x-to-PCI to 60x-to-PCI

  Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the PC8265A) required by the PCI standard as well as message and doorbell registers

  Supports the I2O standard

  Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)

  Support for 66 MHz, 3.3V specification

  60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port

  Makes use of the local bus signals, so there is no need for additional pins

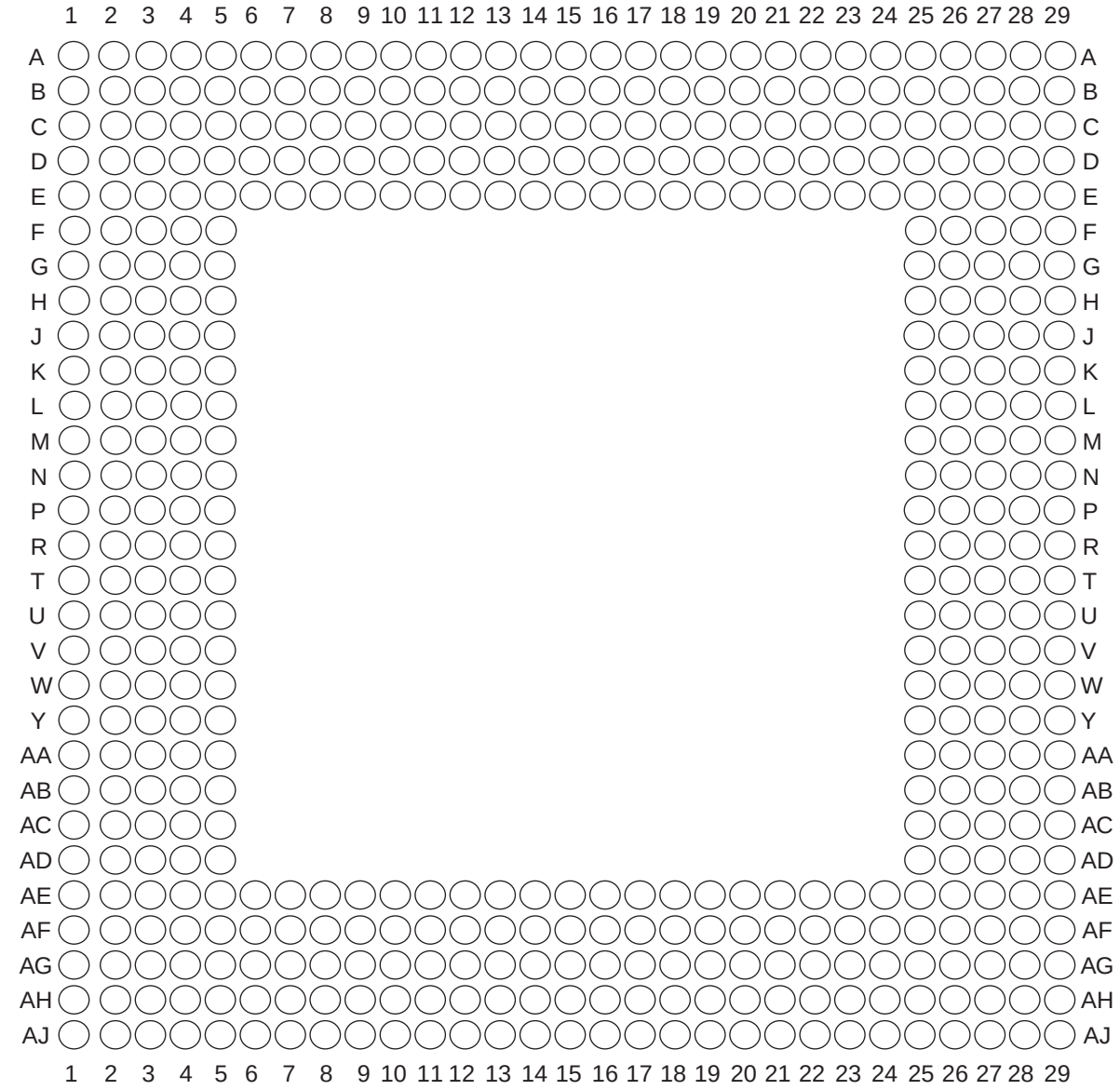
Pinout

This section provides the pin assignments and pinout list for the PC8265A.

Pin Assignments

Figure 2 shows the pinout of the PC8265A's 480 TBGA package as viewed from the top surface.

Figure 2. Pinout of the 480 TBGA Package as Viewed from the Top Surface



Not to Scale

Figure 3 shows the side profile of the TBGA package to indicate the direction of the top surface view.

Figure 3. Side View of the TBGA Package

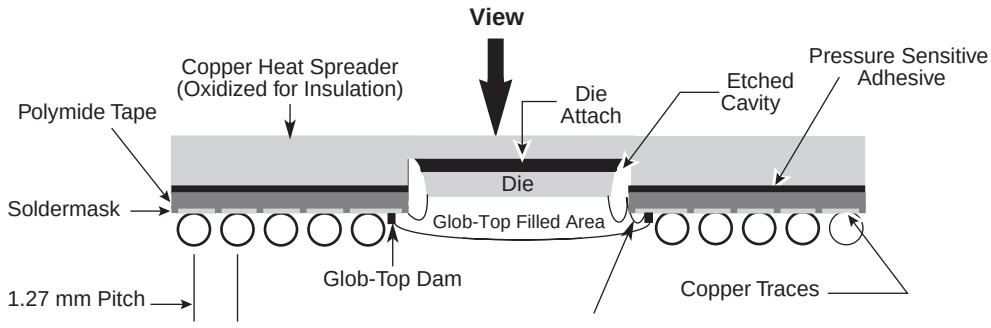


Table 1 shows the pinout list of the PC8265A. Table 2 on page 31 defines conventions and acronyms used in Table 1.

Table 1. Pinout List

Pin Name	Ball
$\overline{BR}$	W5
$\overline{BG}$	F4
$\overline{ABB}$ $\overline{IRQ2}$	E2
$\overline{TS}$	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1
A13	L5
A14	L4
A15	L3
A16	L2

Table 1. Pinout List (Continued)

Pin Name	Ball
A17	L1
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
$\overline{\text{TBST}}$	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
$\overline{\text{AACK}}$	F3
$\overline{\text{ARTRY}}$	E1
$\overline{\text{DBG}}$	V1
DBB $\overline{\text{IRQ3}}$	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9

Table 1. Pinout List (Continued)

Pin Name	Ball
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17

Table 1. Pinout List (Continued)

Pin Name	Ball
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0 RSRV $\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$ DP1 $\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$ DP2 $\overline{\text{TLBISYNC}}$ $\overline{\text{EXT\_DBG2}}$	E21
$\overline{\text{IRQ3}}$ DP3 $\overline{\text{CKSTP\_OUT}}$ $\overline{\text{EXT\_BR3}}$	D21

Table 1. Pinout List (Continued)

Pin Name	Ball
$\overline{\text{IRQ4}}$ DP4 $\overline{\text{CORE\_SRESET}}$ $\overline{\text{EXT\_BG3}}$	C21
$\overline{\text{IRQ5}}$ DP5 $\overline{\text{TBEN}}$ $\overline{\text{EXT\_DBG3}}$	B21
$\overline{\text{IRQ6}}$ DP6 CSE0	A21
$\overline{\text{IRQ7}}$ DP7 CSE1	E20
$\overline{\text{PSDVAL}}$	V3
$\overline{\text{TA}}$	C22
$\overline{\text{TEA}}$	V5
$\overline{\text{GBL}}$ $\overline{\text{IRQ1}}$	W1
$\overline{\text{CI}}$ BADDR29 $\overline{\text{IRQ2}}$	U2
$\overline{\text{WT}}$ BADDR30 $\overline{\text{IRQ3}}$	U3
$\overline{\text{L2\_HIT}}$ $\overline{\text{IRQ4}}$	Y4
$\overline{\text{CPU\_BG}}$ BADDR31 $\overline{\text{IRQ5}}$	U4
$\overline{\text{CPU\_DBG}}$	R2
$\overline{\text{CPU\_BR}}$	Y3
$\overline{\text{CS0}}$	F25
$\overline{\text{CS1}}$	C29
$\overline{\text{CS2}}$	E27
$\overline{\text{CS3}}$	E28
$\overline{\text{CS4}}$	F26
$\overline{\text{CS5}}$	F27
$\overline{\text{CS6}}$	F28
$\overline{\text{CS7}}$	G25

Table 1. Pinout List (Continued)

Pin Name	Ball
$\overline{CS8}$	D29
$\overline{CS9}$	E29
$\overline{CS10}$ $\overline{BCTL1}$	F29
$\overline{CS11}$ AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
$\overline{BCTL0}$	A27
$\overline{PWE0}$ $\overline{PSDDQM0}$ $\overline{PBS0}$	C25
$\overline{PWE1}$ $\overline{PSDDQM1}$ $\overline{PBS1}$	E24
$\overline{PWE2}$ $\overline{PSDDQM2}$ $\overline{PBS2}$	D24
$\overline{PWE3}$ $\overline{PSDDQM3}$ $\overline{PBS3}$	C24
$\overline{PWE4}$ $\overline{PSDDQM4}$ $\overline{PBS4}$	B26
$\overline{PWE5}$ $\overline{PSDDQM5}$ $\overline{PBS5}$	A26
$\overline{PWE6}$ $\overline{PSDDQM6}$ $\overline{PBS6}$	B25
$\overline{PWE7}$ $\overline{PSDDQM7}$ $\overline{PBS7}$	A25
PSDA10 PGPL0	E23
$\overline{PSDWE}$ PGPL1	B24
$\overline{POE}$ $\overline{PSDRAS}$ PGPL2	A24

Table 1. Pinout List (Continued)

Pin Name	Ball
$\overline{\text{PSDCAS}}$ PGPL3	B23
$\overline{\text{PGTA}}$ PUPMWAIT PGPL4 $\overline{\text{PPBS}}$	A23
PSDAMUX PGPL5	D22
$\overline{\text{LWE0}}$ $\overline{\text{LSDDQM0}}$ $\overline{\text{LBS0}}$ PCI_CFG0	H28
$\overline{\text{LWE1}}$ $\overline{\text{LSDDQM1}}$ $\overline{\text{LBS1}}$ PCI_CFG1	H27
$\overline{\text{LWE2}}$ $\overline{\text{LSDDQM2}}$ $\overline{\text{LBS2}}$ PCI_CFG2	H26
$\overline{\text{LWE3}}$ $\overline{\text{LSDDQM3}}$ $\overline{\text{LBS3}}$ PCI_CFG3	G29
LSDA10 LGPL0 PCI_MODCKH0	D27
$\overline{\text{LSDWE}}$ LGPL1 PCI_MODCKH1	C28
$\overline{\text{LOE}}$ $\overline{\text{LSDRAS}}$ LGPL2 PCI_MODCKH2	E26
$\overline{\text{LSDCAS}}$ LGPL3 PCI_MODCKH3	D25
$\overline{\text{LGTA}}$ LUPMWAIT LGPL4 $\overline{\text{LPBS}}$	C26

Table 1. Pinout List (Continued)

Pin Name	Ball
LGPL5 LSDAMUX PCI_MODCK	B27
$\overline{\text{LWR}}$	D28
L_A14 PAR	N27
L_A15 $\overline{\text{FRAME}}$ $\overline{\text{SMI}}$	T29
L_A16 $\overline{\text{TRDY}}$	R27
L_A17 $\overline{\text{IRDY}}$ $\overline{\text{CKSTP\_OUT}}$	R26
L_A18 $\overline{\text{STOP}}$	R29
L_A19 $\overline{\text{DEVSEL}}$	R28
L_A20 IDSEL	W29
L_A21 $\overline{\text{PERR}}$	P28
L_A22 $\overline{\text{SERR}}$	N26
L_A23 $\overline{\text{REQ0}}$	AA27
L_A24 $\overline{\text{REQ1}}$ HSEJSW	P29
L_A25 $\overline{\text{GNT0}}$	AA26
L_A26 $\overline{\text{GNT1}}$ HSLED	N25
L_A27 $\overline{\text{GNT2}}$ $\overline{\text{HSENUM}}$	AA25
L_A28 $\overline{\text{RST}}$ $\overline{\text{CORE\_SRESET}}$	AB29
L_A29 $\overline{\text{INTA}}$	AB28

Table 1. Pinout List (Continued)

Pin Name	Ball
L_A30 $\overline{\text{REQ2}}$	P25
L_A31 DLLOUT	AB27
LCL_D0 AD0	H29
LCL_D1 AD1	J29
LCL_D2 AD2	J28
LCL_D3 AD3	J27
LCL_D4 AD4	J26
LCL_D5 AD5	J25
LCL_D6 AD6	K25
LCL_D7 AD7	L29
LCL_D8 AD8	L27
LCL_D9 AD9	L26
LCL_D10 AD10	L25
LCL_D11 AD11	M29
LCL_D12 AD12	M28
LCL_D13 AD13	M27
LCL_D14 AD14	M26
LCL_D15 AD15	N29
LCL_D16 AD16	T25
LCL_D17 AD17	U27

Table 1. Pinout List (Continued)

Pin Name	Ball
LCL_D18 AD18	U26
LCL_D19 AD19	U25
LCL_D20 AD20	V29
LCL_D21 AD21	V28
LCL_D22 AD22	V27
LCL_D23 AD23	V26
LCL_D24 AD24	W27
LCL_D25 AD25	W26
LCL_D26 AD26	W25
LCL_D27 AD27	Y29
LCL_D28 AD28	Y28
LCL_D29 AD29	Y25
LCL_D30 AD30	AA29
LCL_D31 AD31	AA28
LCL_DP0 C0 $\overline{BE0}$	L28
LCL_DP1 C1 $\overline{BE1}$	N28
LCL_DP2 C2 $\overline{BE2}$	T28
LCL_DP3 C3 $\overline{BE3}$	W28

Table 1. Pinout List (Continued)

Pin Name	Ball
$\overline{\text{IRQ0}}$ $\overline{\text{NMI\_OUT}}$	T1
$\overline{\text{IRQ7}}$ $\overline{\text{INT\_OUT}}$ $\overline{\text{APE}}$	D1
$\overline{\text{TRST}}$	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
$\overline{\text{TRIS}}$	AB4
$\overline{\text{PORESET}}$	AG6
$\overline{\text{HRESET}}$	AH5
$\overline{\text{SRESET}}$	AF6
$\overline{\text{QREQ}}$	AA3
$\overline{\text{RSTCONF}}$	AJ4
MODCK1 AP1 TC0 BNKSEL0	W2
MODCK2 AP2 TC1 BNKSEL1	W3
MODCK3 AP3 TC2 BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0 $\overline{\text{RESTART1}}$ DREQ3 FCC2_UTM_TXADDR2	AC29
PA1 $\overline{\text{REJECT1}}$ FCC2_UTM_TXADDR1 $\overline{\text{DONE3}}$	AC25

Table 1. Pinout List (Continued)

Pin Name	Ball
PA2 CLK20 FCC2_UTM_TXADDR0 $\overline{\text{DACK3}}$	AE28
PA3 CLK19 FCC2_UTM_RXADDR0 $\overline{\text{DACK4}}$ L1RXD1A2	AG29
PA4 $\overline{\text{REJECT2}}$ FCC2_UTM_RXADDR1 $\overline{\text{DONE4}}$	AG28
PA5 $\overline{\text{RESTART2}}$ DREQ4 FCC2_UTM_RXADDR2	AG26
PA6 L1RSYNCA1	AE24
PA7 SMSYN2 L1TSYNCA1 L1GNTA1	AH25
PA8 SMRXD2 L1RXD0A1 L1RXDA1	AF23
PA9 SMTXD2 L1TXD0A1	AH23
PA10 FCC1_UT8_RXD0 FCC1_UT16_RXD8 MSNUM5	AE22
PA11 FCC1_UT8_RXD1 FCC1_UT16_RXD9 MSNUM4	AH22
PA12 FCC1_UT8_RXD2 FCC1_UT16_RXD10 MSNUM3	AJ21

Table 1. Pinout List (Continued)

Pin Name	Ball
PA13 FCC1_UT8_RXD3 FCC1_UT16_RXD11 MSNUM2	AH20
PA14 FCC1_UT8_RXD4 FCC1_UT16_RXD12 FCC1_RXD3	AG19
PA15 FCC1_UT8_RXD5 FCC1_UT16_RXD13 FCC1_RXD2	AF18
PA16 FCC1_UT8_RXD6 FCC1_UT16_RXD14 FCC1_RXD1	AF17
PA17 FCC1_UT8_RXD7 FCC1_UT16_RXD15 FCC1_RXD0 FCC1_RXD	AE16
PA18 FCC1_UT8_TXD7 FCC1_UT16_TXD15 FCC1_TXD0 FCC1_TXD	AJ16
PA19 FCC1_UT8_TXD6 FCC1_UT16_TXD14 FCC1_TXD1	AG15
PA20 FCC1_UT8_TXD5 FCC1_UT16_TXD13 FCC1_TXD2	AJ13
PA21 FCC1_UT8_TXD4 FCC1_UT16_TXD12 FCC1_TXD3	AE13
PA22 FCC1_UT8_TXD3 FCC1_UT16_TXD11	AF12
PA23 FCC1_UT8_TXD2 FCC1_UT16_TXD10	AG11

Table 1. Pinout List (Continued)

Pin Name	Ball
PA24 FCC1_UT8_TXD1 FCC1_UT16_TXD9 MSNUM1	AH9
PA25 FCC1_UT8_TXD0 FCC1_UT16_TXD8 MSNUM0	AJ8
PA26 FCC1_UTM_RXCLAV FCC1_UTS_RXCLAV FCC1_MII_RX_ER	AH7
PA27 FCC1_UT_RXSOC FCC1_MII_RX_DV	AF7
PA28 $\overline{\text{FCC1\_UTM\_RXENB}}$ $\overline{\text{FCC1\_UTS\_RXENB}}$ FCC1_MII_TX_EN	AD5
PA29 FCC1_UT_TXSOC FCC1_MII_TX_ER	AF1
PA30 FCC1_UTM_TXCLAV FCC1_UTS_TXCLAV FCC1_MII_CRS $\overline{\text{FCC1\_RTS}}$	AD3
PA31 $\overline{\text{FCC1\_UTM\_TXENB}}$ $\overline{\text{FCC1\_UTS\_TXENB}}$ FCC1_MII_COL	AB5
PB4 FCC3_TXD3 FCC2_UT8_RXD0 L1RSYNCA2 $\overline{\text{FCC3\_RTS}}$	AD28
PB5 FCC3_TXD2 FCC2_UT8_RXD1 L1TSYNCA2 L1GNTA2	AD26

Table 1. Pinout List (Continued)

Pin Name	Ball
PB6 FCC3_TXD1 FCC2_UT8_RXD2 L1RXDA2 L1RXD0A2	AD25
PB7 FCC3_TXD0 FCC3_TXD FCC2_UT8_RXD3 L1TXDA2 L1TXD0A2	AE26
PB8 FCC2_UT8_TXD3 FCC3_RXD0 FCC3_RXD TXD3 L1RSYNCD1	AH27
PB9 FCC2_UT8_TXD2 FCC3_RXD1 L1TXD2A2 L1TSYNCD1 L1GNTD1	AG24
PB10 FCC2_UT8_TXD1 FCC3_RXD2 L1RXDD1	AH24
PB11 FCC3_RXD3 FCC2_UT8_TXD0 L1TXDD1	AJ24
PB12 FCC3_MII_CRS L1CLKOB1 L1RSYNCC1 TXD2	AG22
PB13 FCC3_MII_COL $\overline{\text{L1RQB1}}$ L1TSYNCC1 L1GNTC1 L1TXD1A2	AH21

Table 1. Pinout List (Continued)

Pin Name	Ball
PB14 FCC3_MII_TX_EN RXD3 L1RXDC1	AG20
PB15 FCC3_MII_TX_ER RXD2 L1TXDC1	AF19
PB16 FCC3_MII_RX_ER L1CLKOA1 CLK18	AJ18
PB17 FCC3_MII_RX_DV L1RQA1 CLK17	AJ17
PB18 FCC2_UT8_RXD4 FCC2_RXD3 L1CLKOD2 L1RXD2A2	AE14
PB19 FCC2_UT8_RXD5 FCC2_RXD2 L1RQD2 L1RXD3A2	AF13
PB20 FCC2_UT8_RXD6 FCC2_RXD1 L1RSYNCD2 L1TXD1A1	AG12
PB21 FCC2_UT8_RXD7 FCC2_RXD0 FCC2_RXD L1TSYNCD2 L1GNTD2 L1TXD2A1	AH11
PB22 FCC2_UT8_TXD7 FCC2_TXD0 FCC2_TXD L1RXD1A1 L1RXDD2	AH16

Table 1. Pinout List (Continued)

Pin Name	Ball
PB23 FCC2_UT8_TXD6 FCC2_TXD1 L1RXD2A1 L1TXDD2	AE15
PB24 FCC2_UT8_TXD5 FCC2_TXD2 L1RXD3A1 L1RSYNCC2	AJ9
PB25 FCC2_UT8_TXD4 FCC2_TXD3 L1TSYNCC2 L1GNTC2 L1TXD3A1	AE9
PB26 FCC2_MII_CRS FCC2_UT8_TXD1 L1RXDC2	AJ7
PB27 FCC2_MII_COL FCC2_UT8_TXD0 L1TXDC2	AH6
PB28 FCC2_MII_RX_ER $\overline{\text{FCC2\_RTS}}$ L1TSYNCB2 L1GNTB2 TXD1	AE3
PB29 FCC2_UTM_RXCLAV FCC2_UTS_RXCLAV L1RSYNCB2 FCC2_MII_TX_EN	AE2
PB30 FCC2_MII_RX_DV FCC2_UT_TXSOC L1RXDB2	AC5
PB31 FCC2_MII_TX_ER FCC2_UT_RXSOC L1TXDB2	AC4

Table 1. Pinout List (Continued)

Pin Name	Ball
PC0 DREQ1 BRGO7 $\overline{\text{SMSYN2}}$ L1CLKOA2	AB26
PC1 DREQ2 BRGO6 $\overline{\text{L1RQA2}}$	AD29
PC2 $\overline{\text{FCC3\_CD}}$ FCC2_UT8_TXD3 $\overline{\text{DONE2}}$	AE29
PC3 $\overline{\text{FCC3\_CTS}}$ FCC2_UT8_TXD2 $\overline{\text{DACK2}}$ $\overline{\text{CTS4}}$	AE27
PC4 $\overline{\text{FCC2\_UTM\_RXENB}}$ $\overline{\text{FCC2\_UTS\_RXENB}}$ SI2_L1ST4 $\overline{\text{FCC2\_CD}}$	AF27
PC5 FCC2_UTM_TXCLAV FCC2_UTS_TXCLAV SI2_L1ST3 $\overline{\text{FCC2\_CTS}}$	AF24
PC6 $\overline{\text{FCC1\_CD}}$ L1CLKOC1 FCC1_UTM_RXADDR2 FCC1_UTS_RXADDR2 FCC1_UTM_RXCLAV1	AJ26
PC7 $\overline{\text{FCC1\_CTS}}$ $\overline{\text{L1RQC1}}$ FCC1_UTM_TXADDR2 FCC1_UTS_TXADDR2 FCC1_UTM_TXCLAV1	AJ25

Table 1. Pinout List (Continued)

Pin Name	Ball
PC8 $\overline{\text{CD4}}$ RENA4 FCC1_UT16_TXD0 SI2_L1ST2 $\overline{\text{CTS3}}$	AF22
PC9 $\overline{\text{CTS4}}$ CLSN4 FCC1_UT16_TXD1 SI2_L1ST1 L1TSYNCA2 L1GNTA2	AE21
PC10 $\overline{\text{CD3}}$ RENA3 FCC1_UT16_TXD2 SI1_L1ST4 FCC2_UT8_RXD3	AF20
PC11 $\overline{\text{CTS3}}$ CLSN3 L1CLKOD1 L1TXD3A2 FCC2_UT8_RXD2	AE19
PC12 $\overline{\text{CD2}}$ RENA2 SI1_L1ST3 FCC1_UTM_RXADDR1 FCC1_UTS_RXADDR1	AE18
PC13 $\overline{\text{CTS2}}$ CLSN2 $\overline{\text{L1RQD1}}$ FCC1_UTM_TXADDR1 FCC1_UTS_TXADDR1	AH18
PC14 $\overline{\text{CD1}}$ RENA1 FCC1_UTM_RXADDR0 FCC1_UTS_RXADDR0	AH17

Table 1. Pinout List (Continued)

Pin Name	Ball
PC15 $\overline{\text{CTS1}}$ CLSN1 SMTXD2 FCC1_UTM_TXADDR0 FCC1_UTS_TXADDR0	AG16
PC16 CLK16 TIN4	AF15
PC17 CLK15 TIN3 BRGO8	AJ15
PC18 CLK14 $\overline{\text{TGATE2}}$	AH14
PC19 CLK13 BRGO7	AG13
PC20 CLK12 $\overline{\text{TGATE1}}$	AH12
PC21 CLK11 BRGO6	AJ11
PC22 CLK10 $\overline{\text{DONE1}}$	AG10
PC23 CLK9 BRGO5 $\overline{\text{DACK1}}$	AE10
PC24 FCC2_UT8_TXD3 CLK8 $\overline{\text{TOUT4}}$	AF9
PC25 FCC2_UT8_TXD2 CLK7 BRGO4	AE8

Table 1. Pinout List (Continued)

Pin Name	Ball
PC26 CLK6 $\overline{\text{TOUT3}}$ TMCLK	AJ6
PC27 FCC3_TXD FCC3_TXD0 CLK5 BRGO3	AG2
PC28 CLK4 TIN1 $\overline{\text{TOUT2}}$ $\overline{\text{CTS2}}$ CLSN2	AF3
PC29 CLK3 TIN2 BRGO2 $\overline{\text{CTS1}}$ CLSN1	AF2
PC30 FCC2_UT8_TXD3 CLK2 $\overline{\text{TOUT1}}$	AE1
PC31 CLK1 BRGO1	AD1
PD4 BRGO8 L1TSYNCD1 L1GNTD1 $\overline{\text{FCC3\_RTS}}$ SMRXD2	AC28
PD5 FCC1_UT16_TXD3 $\overline{\text{DONE1}}$	AD27
PD6 FCC1_UT16_TXD4 $\overline{\text{DACK1}}$	AF29

Table 1. Pinout List (Continued)

Pin Name	Ball
PD7 SMSYN1 FCC1_UTM_TXADDR3 FCC1_UTS_TXADDR3 FCC1_TXCLAV2	AF28
PD8 SMRXD1 FCC2_UT_TXPRTY BRGO5	AG25
PD9 SMTXD1 FCC2_UT_RXPRTY BRGO3	AH26
PD10 L1CLKOB2 FCC2_UT8_RXD1 L1RSYNCB1 BRGO4	AJ27
PD11 $\overline{\text{L1RQB2}}$ FCC2_UT8_RXD0 L1TSYNCB1 L1GNTB1	AJ23
PD12 SI1_L1ST2 L1RXDB1	AG23
PD13 SI1_L1ST1 L1TXDB1	AJ22
PD14 FCC1_UT16_RXD0 L1CLKOC2 I2CSCL	AE20
PD15 FCC1_UT16_RXD1 $\overline{\text{L1RQC2}}$ I2CSDA	AJ20
PD16 FCC1_UT_TXPRTY L1TSYNCC1 L1GNTC1 SPIMISO	AG18

Table 1. Pinout List (Continued)

Pin Name	Ball
PD17 FCC1_UT_RXPRTY BRGO2 SPIMOSI	AG17
PD18 FCC1_UTM_RXADDR4 FCC1_UTS_RXADDR4 FCC1_UTM_RXCLAV3 SPICLK	AF16
PD19 FCC1_UTM_TXADDR4 FCC1_UTS_TXADDR4 FCC1_UTM_TXCLAV3 SPISEL BRGO1	AH15
PD20 $\overline{\text{RTS4}}$ TENA4 FCC1_UT16_RXD2 L1RSYNCA2	AJ14
PD21 TXD4 FCC1_UT16_RXD3 L1RXD0A2 L1RXDA2	AH13
PD22 RXD4 FCC1_UT16_TXD5 L1TXD0A2 L1TXDA2	AJ12
PD23 $\overline{\text{RTS3}}$ TENA3 FCC1_UT16_RXD4 L1RSYNCD1	AE12
PD24 TXD3 FCC1_UT16_RXD5 L1RXDD1	AF10
PD25 RXD3 FCC1_UT16_TXD6 L1TXDD1	AG9

Table 1. Pinout List (Continued)

Pin Name	Ball
PD26 $\overline{\text{RTS2}}$ TENA2 FCC1_UT16_RXD6 L1RSYNCC1	AH8
PD27 TXD2 FCC1_UT16_RXD7 L1RXDC1	AG7
PD28 RXD2 FCC1_UT16_TXD7 L1TXDC1	AE4
PD29 $\overline{\text{RTS1}}$ TENA1 FCC1_UTM_RXADDR3 FCC1_UTS_RXADDR3 FCC1_UTM_RXCLAV2	AG1
PD30 $\overline{\text{FCC2\_UTM\_TXENB}}$ $\overline{\text{FCC2\_UTS\_TXENB}}$ TXD1	AD4
PD31 RXD1	AD2
SYN	AB3
SYN1	B9
GNDSYN	AB1
CLKIN2(1)	AE11
SPARE4(2)	U5
$\overline{\text{PCI\_MODE}}$(3)	AF25
SPARE6(2)	V4
THERMAL0(4)	AA1
THERMAL1(4)	AG4

Table 1. Pinout List (Continued)

Pin Name	Ball
I/O Power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

Notes:
1. This pin should be used as CLKIN2
2. Must be pulled down or left floating
3. This pin should be asserted if the PCI function is desired or pulled up or left floating if PCI is not desired
4. For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.motorola.com/semiconductors

Symbols used in Table 1 are described in Table 2.

Table 2. Symbol Legend

Symbol	Meaning
$\overline{\text{OVERBAR}}$	Signals with overbars, such as $\overline{\text{TA}}$, are active low
UTM	Indicates that a signal is part of the UTOPIA master interface
UTS	Indicates that a signal is part of the UTOPIA slave interface
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface
MII	Indicates that a signal is part of the media independent interface

Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the PC8265A.

DC Electrical Characteristics

This section describes the DC electrical characteristics for the PC8265A. Table 3 shows the maximum electrical ratings.

Table 3. Absolute Maximum Ratings(1)

Rating	Symbol	Value	Unit
Core supply voltage(2)	V_{DD}	-0.3 – +2.5	V
PLL supply voltage(2)	SYN	-0.3 – +2.5	V
I/O supply voltage(3)	V_{DDH}	-0.3 – +4.0	V
Input voltage(4)	V_{IN}	GND(-0.3) – +3.6	V
Storage temperature range	T_{STG}	-55 – +150	°C

Notes:
1. Absolute maximum ratings are stress ratings only; functional operation (see Table 4) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.
2. Caution: VDD/SYN must not exceed V_{DDH} by more than 0.4V at any time, including during power-on reset.
3. Caution: V_{DDH} can exceed VDD/SYN by 3.3V during power on reset by no more than 100 ms. V_{DDH} should not exceed VDD/SYN by more than 2.5V during normal operation.
4. Caution: V_{IN} must not exceed V_{DDH} by more than 2.5V at any time, including during power-on reset.

Table 4 lists recommended operational voltage conditions.

Table 4. Recommended Operating Conditions(1)

Rating	Symbol	Value			Unit
Core supply voltage	V_{DD}	1.7 – 1.9(2)	1.7 – 2.1(3)	1.9 – 2.2(4)	V
PLL supply voltage	SYN	1.7 – 1.9(2)	1.7 – 2.1(3)	1.9 – 2.2(4)	V
CPU minimum frequency	Fmin	150	190	190	MHz
I/O supply voltage	V_{DDH}	3.135 – 3.465			V
Input voltage	V_{IN}	GND (-0.3) – 3.465			V
Tcase	T_C	-55 – +125			°C

Notes:
1. Caution: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed
2. CPU frequency less than or equal to 200 MHz
3. CPU frequency greater than 200 MHz but less than or equal 233 MHz
4. CPU frequency greater than 233 MHz

Note: V_{DDH} and V_{DD} must track each other and both must vary in the same direction – in the positive direction (+5% and +0.1 V_{DC}) or in the negative direction (-5% and -0.1 V_{DC}).

This device contains circuitry protection against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 5 shows DC Electrical Characteristics

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, $V_{IN} = V_{DDH}$	I_{IN}	–	10	µA
Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}$	I_{OZ}	–	10	µA
Signal low input current, $V_{IL} = 0.8V$	I_L	–	1	µA
Signal high input current, $V_{IH} = 2.0V$	I_H	–	1	µA
Output high voltage, $I_{OH} = -2$ mA except XFC, UTOPIA mode, and open drain pins In UTOPIA mode: $I_{OH} = -8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	–	V
In UTOPIA mode: $I_{OL} = 8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	–	0.5	V
$I_{OL} = 7.0$ mA $\overline{BR}$ $\overline{BG}$ $\overline{ABB/IRQ2}$ $\overline{TS}$ A[0-31] TT[0-4] $\overline{TBST}$ TSIZE[0–3] $\overline{AACK}$ $\overline{ARTRY}$ $\overline{DBG}$	V_{OL}	–	0.4	V

Table 5. DC Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Max	Unit
DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ				
I_{OL} = 5.3 mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3[(1)] LSDA10/LGPL0/PCI_MODCKH0[(1)] LSDWE/LGPL1/PCI_MODCKH1[(1)]	V_{OL}	–	0.4	V

Table 5. DC Electrical Characteristics (Continued)

Characteristic	Symbol	Min	Max	Unit
LOE/LSDRAS/LGPL2/PCI_MODCKH2(1)				
LSDCAS/LGPL3/PCI_MODCKH3(1)				
LGTA/LUPMWAIT/LGPL4/LPBS				
LSDAMUX/LGPL5/PCI_MODCK(1)				
LWR				
MODCK1/AP(1)/TC(0)/BNKSEL(0)				
MODCK2/AP(2)/TC(1)/BNKSEL(1)				
MODCK3/AP(3)/TC(2)/BNKSEL(2)				
I_{OL} = 3.2 mA				
L_A14/PAR(1)				
L_A15/FRAME(1)/SMI				
L_A16/TRDY(1)				
L_A17/IRDY(1)/CKSTP_OUT				
L_A18/STOP(1)				
L_A19/DEVSEL(1)				
L_A20/IDSEL(1)				
L_A21/PERR(1)				
L_A22/SERR(1)				
L_A23/REQ0(1)				
L_A24/REQ1(1)/HSEJSW(1)				
L_A25/GNT0(1)				
L_A26/GNT1(1)/HSLED(1)				
L_A27/GNT2(1)/HSENUM(1)				
L_A28/RST(1)/CORE_SRESET				
L_A29/INTA(1)				
L_A30/REQ2(1)				
L_A31				
LCL_D(0-31)/AD(0-31)(1)				
LCL_DP(0-3)/C/BE(0-3)(1)				
PA[0–31]				
PB[4–31]				
PC[0–31]				
PD[4–31]				
TDO				

Note: 1. The leakage current is measured for nominal V_{DDH} and V_{DD} or both V_{DDH} and V_{DD} must vary in the same direction; that is, V_{DDH} and V_{DD} either both vary in the positive direction (+5% and +0.1 V_{DC}) or both vary in the negative direction (-5% and -0.1 V_{DC})

Thermal Characteristics

Table 6 describes thermal characteristics.

Table 6. Thermal Characteristics for the 480 TBGA Package

Characteristics	Symbol	Value	Unit	Air Flow
Junction to ambient	Θ_{JA}	13.07(1)	°C/W	NC(2)
	Θ_{JA}	9.55(1)	°C/W	1 m/s
	Θ_{JA}	10.48(3)	°C/W	NC
	Θ_{JA}	7.78(3)	°C/W	1 m/s
Junction to board(4)	Θ_{JB}	6	°C/W	–
Junction to case(5)	Θ_{JC}	2	°C/W	–

Notes:
1. Assumes a single layer board with no thermal vias
2. Natural convection
3. Assumes a four layer board
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1)

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C
Θ_{JA} = package thermal resistance, junction to ambient, °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)
$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is as follows:

$$P_D = K/(T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Layout Practices

Each pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the chip. The power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to the chip and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as GND planes.

All output pins on the PC8265A have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses.

Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 7 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3W (when the ambient temperature is 70°C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 7. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W)[2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	–	–	2.3	2.9
66.66	3	4.5	200	300	–	–	2.4	3.1
83.33	2	3	166	250	–	–	2.2	2.8
83.33	2	3	166	250	–	–	2.2	2.8
83.33	2.5	3.5	208	291	–	–	2.4	3.1

Notes: 1. Test temperature = room temperature (25°C)
2. $P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz PC8265A device. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in Table 8.

Table 8. Output Buffer Impedances(1)

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory Controller	40
Parallel I/O	46
PCI	25

Note: 1. These are typical values at 65°C. The impedance may vary by ±25% with process and temperature.

Table 9 lists CPM output characteristics.

Table 9. AC Characteristics for CPM Outputs(1)

		Max Delay (ns)		Min Delay (ns)	
Spec_num Max/Min	Characteristic	66 MHz	83 MHz	66 MHz	83 MHz
sp36a/sp37a	FCC outputs – internal clock (NMSI)	6	5.5	1	1
sp36b/sp37b	FCC outputs – external clock (NMSI)	14	12	2	1
sp38a/sp39a	SCC/SMC/SPI/I2C outputs – internal clock (NMSI)	19	16	1	0.5
sp38b/sp39b	Ex_SCC/SMC/SPI/I2C outputs – external clock (NMSI)	19	16	2	1
sp42/sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a/sp43a	PIO outputs	14	11	0.5	0.5

Note: 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 10 lists CPM input characteristics.

Table 10. AC Characteristics for CPM Inputs(1)

		Setup (ns)		Hold (ns)	
Spec_num	Characteristic	66 MHz	83 MHz	66 MHz	83 MHz
sp16a/sp17a	FCC inputs – internal clock (NMSI)	10	8	0	0
sp16b/sp17b	FCC inputs – external clock (NMSI)	3	2.5	3	2
sp20/sp21	TDM inputs/SI	15	12	12	10
sp18a/sp19a	SCC/SMC/SPI/I2C inputs – internal clock (NMSI)	20	16	0	0
sp18b/sp19b	SCC/SMC/SPI/I2C inputs – external clock (NMSI)	5	4	5	4
sp22/sp23	PIO/TIMER/IDMA inputs	10	8	3	3

Note: 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 4 shows the FCC external clock.

Figure 4. FCC External Clock Diagram

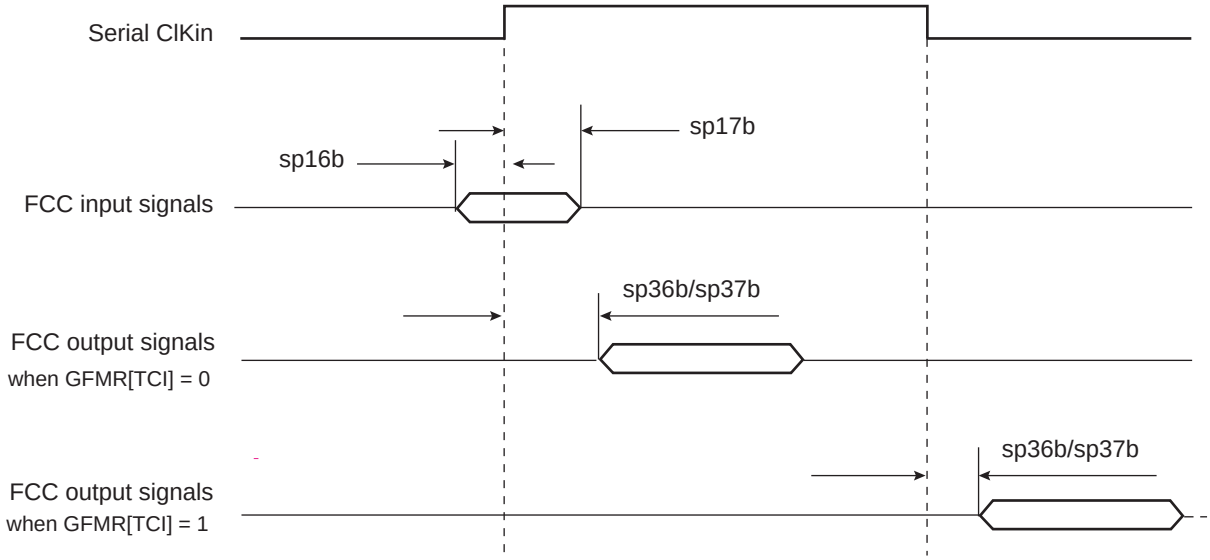


Figure 5 shows the FCC internal clock.

Figure 5. FCC Internal Clock Diagram

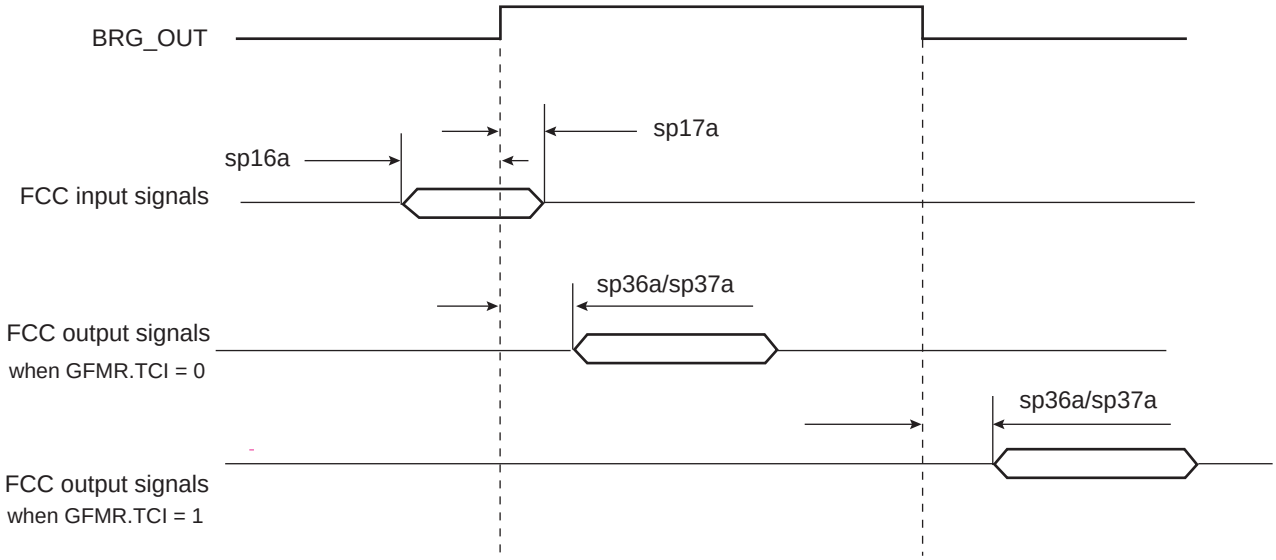
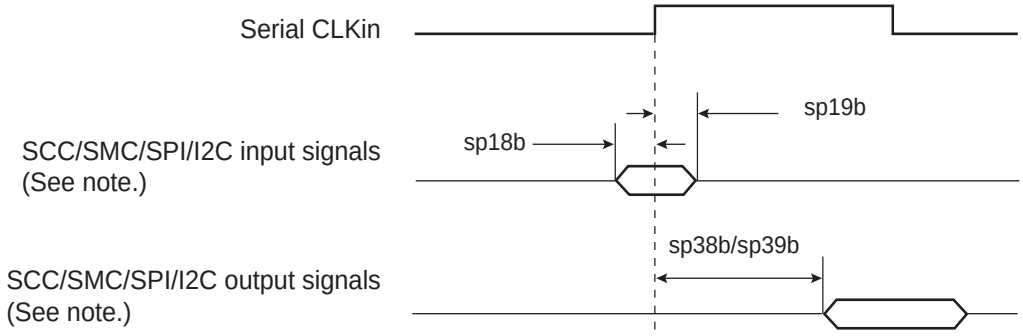


Figure 6 shows the SCC/SMC/SPI/I^{2}C external clock.

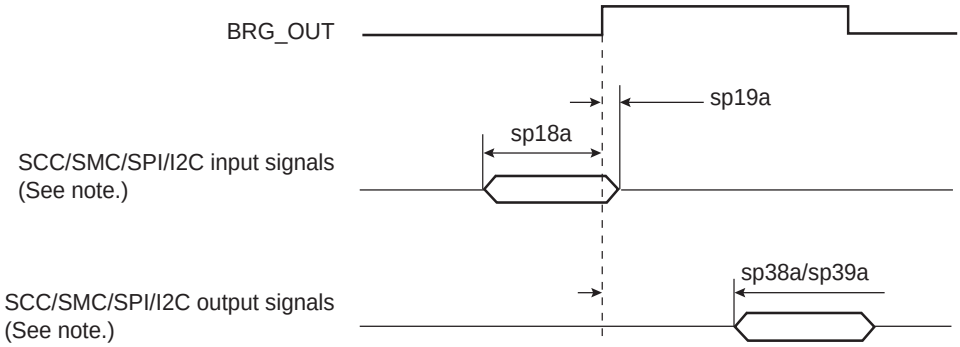
Figure 6. SCC/SMC/SPI/I^{2}C External Clock Diagram



Note: The clock edge is selectable on SCC and SPI.

Figure 7 shows the SCC/SMC/SPI/I^{2}C internal clock.

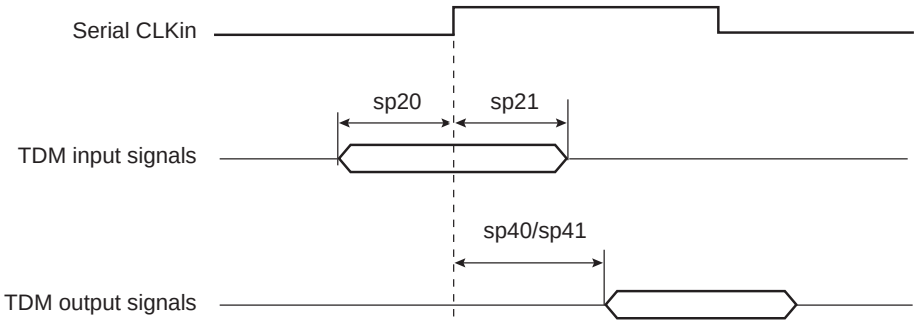
Figure 7. SCC/SMC/SPI/I^{2}C Internal Clock Diagram



Note: The clock edge is selectable on SCC and SPI

Figure 8 shows TDM input and output signals.

Figure 8. TDM Signals Diagram



There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown)
2. Input sampled on the rising edge and output driven on the falling edge
3. Input sampled on the falling edge and output driven on the falling edge
4. Input sampled on the falling edge and output driven on the rising edge

Figure 9 shows PIO, timer, and DMA signals.

Figure 9. PIO, Timer, and DMA Signal Diagram

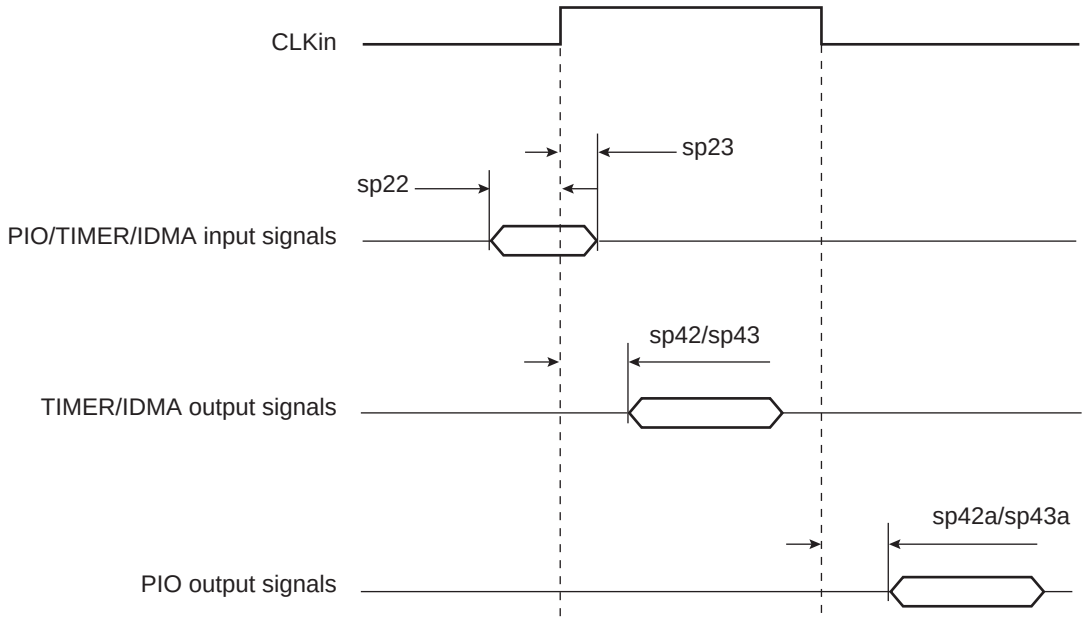


Table 11 lists SIU input characteristics.

Table 11. AC Characteristics for SIU Inputs[1]

Spec_num	Characteristic	Setup (ns)		Hold (ns)	
		66 MHz	83 MHz	66 MHz	83 MHz
sp11/sp10	$\overline{\text{AACK}}/\overline{\text{ARTRY}}/\overline{\text{TA}}/\overline{\text{TS}}/\overline{\text{TEA}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}$	6	5	1	1
sp12/sp10	Data bus in normal mode	5	4	1	1
sp13/sp10	Data bus in ECC and PARITY modes	8	6	1	1
sp14/sp10	DP pins	7	6	1	1
sp15/sp10	All other pins	5	4	1	1

Note: 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 12 lists SIU output characteristics.

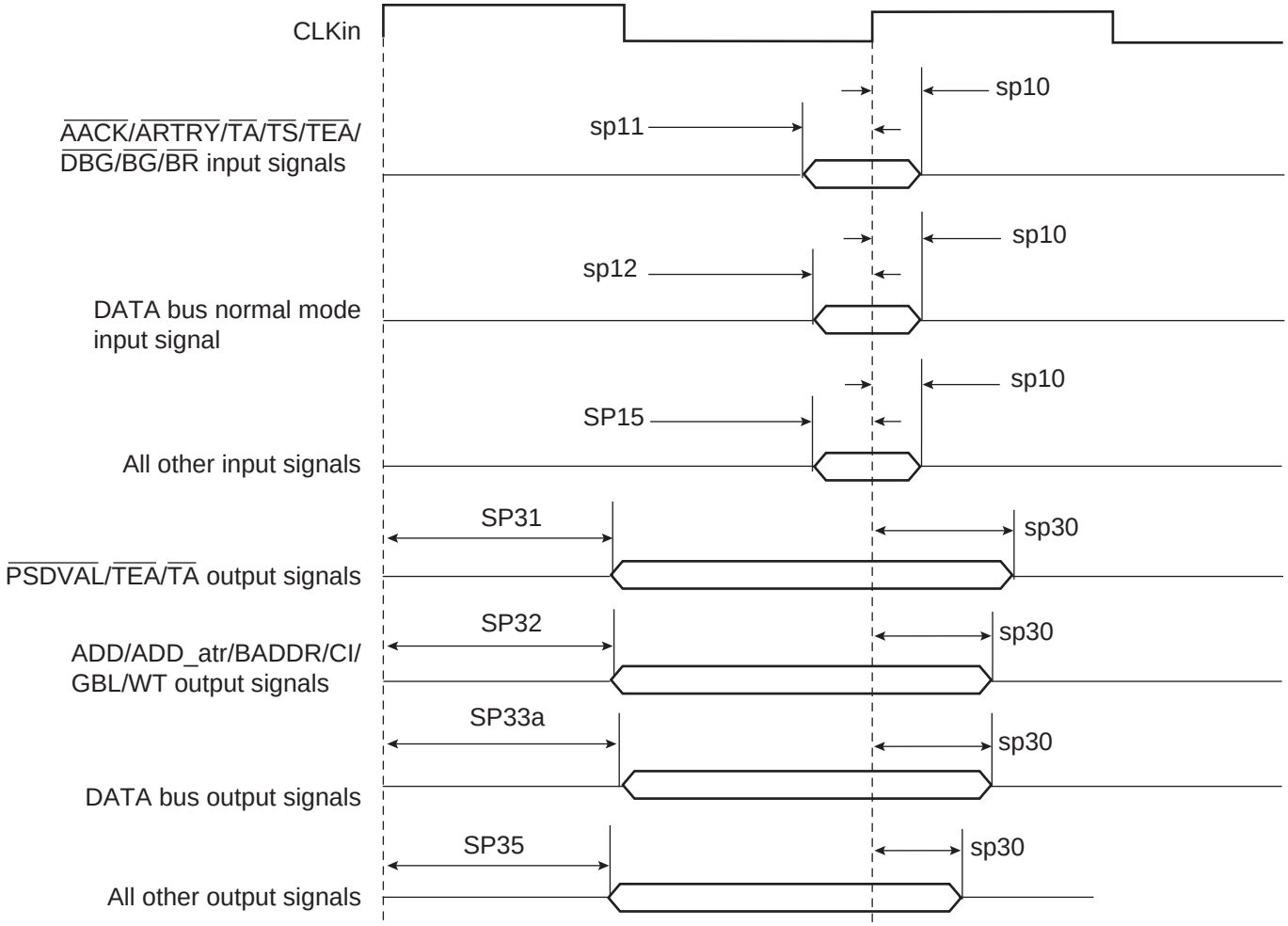
Table 12. AC Characteristics for SIU Outputs[1]

Spec_num Max/Min	Characteristic	Setup (ns)		Hold (ns)	
		66 MHz	83 MHz	66 MHz	83 MHz
sp31/sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32/sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a/sp30	Data bus	6.5	6.5	0.5	0.5
sp33b/sp30	DP	8	7	0.5	0.5
sp34/sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35/sp30	All other signals	6	5.5	0.5	0.5

Note: 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Figure 10 shows the interaction of several bus signals.

Figure 10. Bus Signals



Note: Activating data pipelining (setting BR x [DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 11 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

Figure 11. Parity Mode Diagram

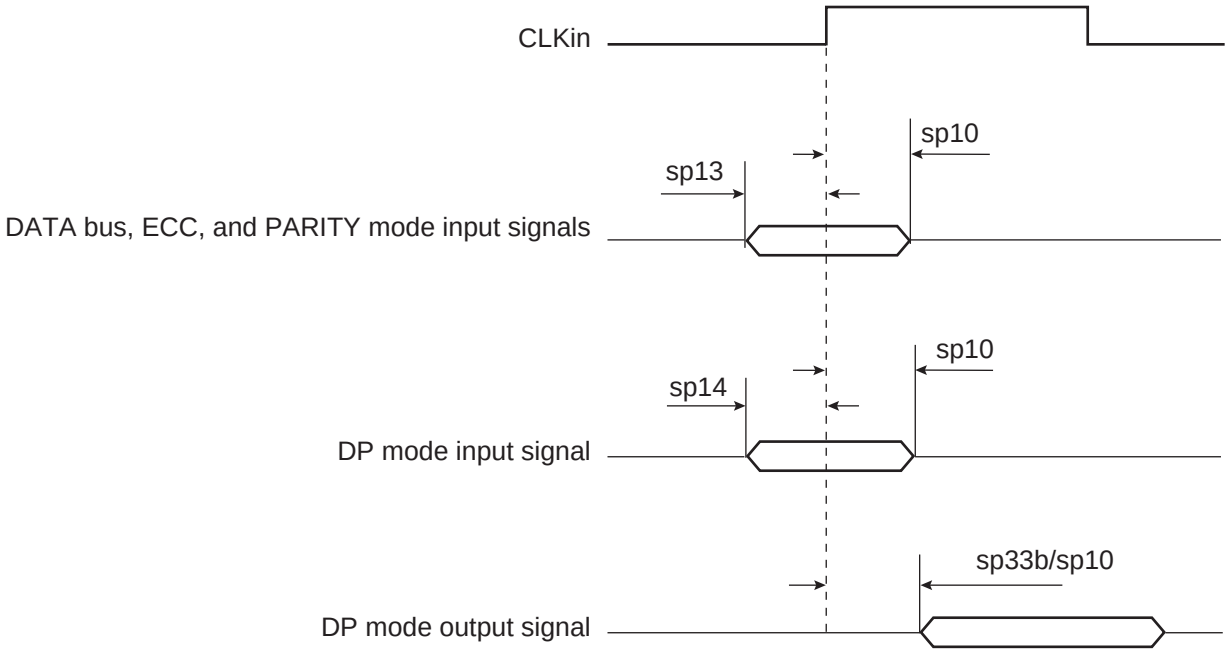
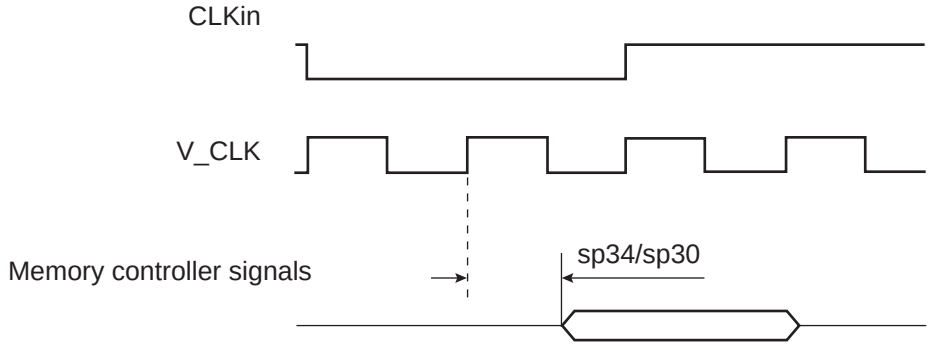


Figure 12 shows signal behavior in MEMC mode.

Figure 12. MEMC Mode Diagram



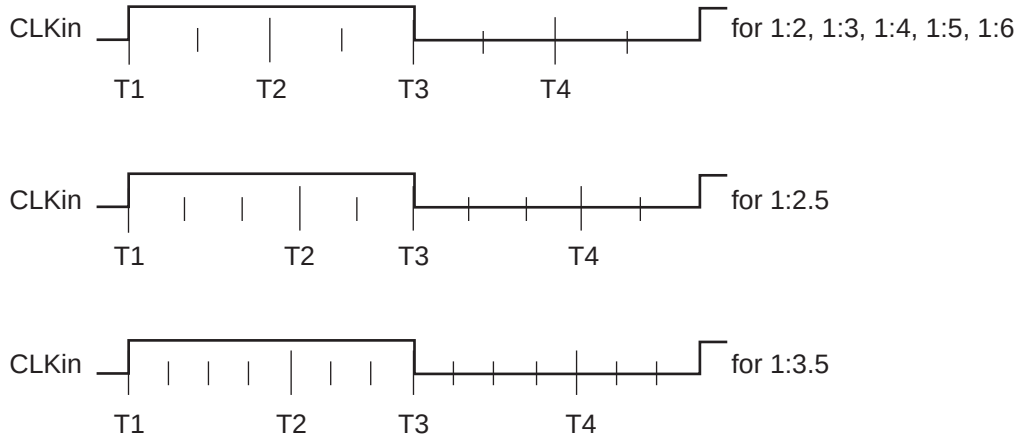
Note: Generally, all PC8265A bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 13.

Table 13. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 13 is a graphical representation of Table 13.

Figure 13. Internal Tick Spacing for Memory Controller Signals



Note: The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

Clock Configuration Modes

To configure the main PLL multiplication factor and the core, the CPM, and 60x bus frequencies, the MODCK[1:3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 14 shows the eight basic configuration modes. Another 49 modes are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

Local Bus Mode

Table 14 describes default clock modes for the PC8265A.

Table 14. Clock Default Modes

MODCK[1–3]	Input Clock Frequency (MH)z	CPM Multiplication Factor	CPM Frequency (MHz)	Core Multiplication Factor	Core Frequency (MHz)
000	33	3	100	4	133
001	33	3	100	5	166
010	33	4	133	4	133
011	33	4	133	5	166
100	66	2	133	2.5	166
101	66	2	133	3	200
110	66	2.5	166	2.5	166
111	66	2.5	166	3	200

Table 15 describes all possible clock configurations when using the hard reset configuration sequence.

Note that the clock configuration changes only after $\overline{\text{POR}}$ is asserted. Note also that basic modes are shown in boldface type.

Table 15. Clock Configuration Modes[1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2][3] (MHz)	CPM Multiplication Factor[2]	CPM Frequency[2] (MHz)	Core Multiplication Factor[2]	Core Frequency[2] (MHz)
0001_000	33	2	66	4	133
0001_001	33	2	66	5	166
0001_010	33	2	66	6	200
0001_011	33	2	66	7	233
0001_100	33	2	66	8	266
0001_101	33	3	100	4	133
0001_110	33	3	100	5	166
0001_111	33	3	100	6	200
0010_000	33	3	100	7	233
0010_001	33	3	100	8	266
0010_010	33	4	133	4	133
0010_011	33	4	133	5	166

Table 15. Clock Configuration Modes[1] (Continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2][3] (MHz)	CPM Multiplication Factor[2]	CPM Frequency[2] (MHz)	Core Multiplication Factor[2]	Core Frequency[2] (MHz)
0010_100	33	4	133	6	200
0010_101	33	4	133	7	233
0010_110	33	4	133	8	266
0010_111	33	5	166	4	133
0011_000	33	5	166	5	166
0011_001	33	5	166	6	200
0011_010	33	5	166	7	233
0011_011	33	5	166	8	266
0011_100	33	6	200	4	133
0011_101	33	6	200	5	166
0011_110	33	6	200	6	200
0011_111	33	6	200	7	233
0100_000	33	6	200	8	266
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66	2	133	2	133
0101_110	66	2	133	2.5	166
0101_111	66	2	133	3	200
0110_000	66	2	133	3.5	233
0110_001	66	2	133	4	266
0110_010	66	2	133	4.5	300

Table 15. Clock Configuration Modes[1] (Continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2][3] (MHz)	CPM Multiplication Factor[2]	CPM Frequency[2] (MHz)	Core Multiplication Factor[2]	Core Frequency[2] (MHz)
0110_011	66	2.5	166	2	133
0110_100	66	2.5	166	2.5	166
0110_101	66	2.5	166	3	200
0110_110	66	2.5	166	3.5	233
0110_111	66	2.5	166	4	266
0111_000	66	2.5	166	4.5	300
0111_001	66	3	200	2	133
0111_010	66	3	200	2.5	166
0111_011	66	3	200	3	200
0111_100	66	3	200	3.5	233
0111_101	66	3	200	4	266
0111_110	66	3	200	4.5	300
0111_111	66	3.5	233	2	133
1000_000	66	3.5	233	2.5	166
1000_001	66	3.5	233	3	200
1000_010	66	3.5	233	3.5	233
1000_011	66	3.5	233	4	266
1000_100	66	3.5	233	4.5	300

Notes:
1. Because of speed dependencies, not all of the possible configurations in Table 15 are applicable.
2. The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than150 MHz and the CPM ranges between 66 – 233 MHz.
3. Input clock frequency is given only for the purpose of reference. MODCK_H–MODCK_L should be set so that the resulting configuration does not exceed the frequency rating of the user's part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 66 MHz input clock and MODCK_H–MODCK_L[0111–101] (with a core multiplication factor of 4 and a CPM multiplication factor of 3). The resulting configuration equals the part's maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, and 66 MHz bus.
2. 50 MHz input clock and MODCK_H–MODCK_L[0111–101] to achieve a configuration of 200 MHz CPU, 150 MHz CPM, and 50 MHz bus.
3. 40 MHz input clock and MODCK_H–MODCK_L[0010–011] to achieve a configuration of 200 MHz CPU, 160 MHz CPM, and 40 MHz bus.

Note that with each example, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part's rating.

PCI Mode

This section pertains to the PC8265A and the PC8266A only.

In PCI mode only, MODCK_HI[0:3] and PCI_MODCK come from the following external pins:

- PCI_MODCK = LGPL5
- MODCK_HI[0:3] = {LGPL0,LGPL1,LGPL2,LGPL3}

Note: The minimum Tval = 2 when PCI_MODCK = 1 and minimum Tval = 1 when PCI_MODCK = 0; therefore, board designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

Table 16. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3](1)	Input Clock Frequency	CPM Multiplication	CPM Frequency	Core Multiplication	Core Frequency	PCI Division Factor(2)	PCI Frequency(2)
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

Notes: 1. Assumes MODCK_HI = 0000.
2. The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.)

Table 17 describes all possible clock configurations when using the PC8265A or the PC8266A’s internal PCI bridge in host mode.

Table 17. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency(1) (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor(2)	PCI Frequency(2)
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	33 MHz	4	133 MHz	5	166 MHz	4/8	33/16 MHz
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000(3)	33 MHz	5	166 MHz	5	166 MHz	5	33 MHz
0011_001(3)	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (Continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0011_010[3]	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
0101_001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	66 MHz	2.5	166 MHz	2.5	166 MHz	3/6	55/28 MHz
0110_001	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (Continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency(1) (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor(2)	PCI Frequency(2)
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

Notes: 1. Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 66 MHz input clock, MODCK_H–MODCK_L[0111–011] (with a core multiplication factor of 4 and a CPM multiplication factor of 3), and PCI_MODCK = 0 (see note 2 below). The resulting configuration equals the part's maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, 66 MHz 60x bus, and a PCI frequency of 66 MHz.
2. 50 MHz input clock, MODCK_H–MODCK_L[0111–011], and PCI_MODCK = 0 (see note 2below) to achieve a configuration of 200 MHz CPU, 150 MHz CPM, 50 MHz 60x bus, and a PCI frequency of 50 MHz.
3. 40 MHz input clock, MODCK_H–MODCK_L[0010–000], and PCI_MODCK = 0 (see note 2 below) to achieve a configuration of 200 MHz CPU, 160 MHz CPM, 40 MHz 60x bus, and a PCI frequency of 40 MHz.

Note that with each of the examples, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part's rating.

2. The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic "1"), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.).
3. In this mode, PCI_MODCK must be "0"

.

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)(1)

MODCK[1–3](2)	Input Clock Frequency (PCI)(3)	CPM Multiplication Factor(3)	CPM Frequency	Core Multiplication Factor	Core(4) Frequency	Bus Division Factor	60x Bus(5) Frequency
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

Notes:
1. The user should verify that all buses and functions run frequencies that are within the supported ranges
2. Assumes MODCK_HI = 0000
3. The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2
4. Core frequency = (60x bus frequency)(core multiplication factor)
5. Bus frequency = CPM frequency/bus division factor

Table 19 describes all possible clock configurations when using the PC8265A or the PC8266A’s internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode(1)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)(2)(3)	CPM Multiplication Factor(2)	CPM Frequency	Core Multiplication Factor	Core(4) Frequency	Bus Division Factor	60x Bus(5) Frequency
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	150 MHz	3	180 MHz	2.5	60 MHz
0010_010	50/25 MHz	3/6	150 MHz	3.5	210 MHz	2.5	60 MHz
0010_011	50/25 MHz	3/6	150 MHz	4	240 MHz	2.5	60 MHz
0010_100	50/25 MHz	3/6	150 MHz	4.5	270 MHz	2.5	60 MHz
0011_000	66/33 MHz	2/4	133 MHz	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	133 MHz	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	133 MHz	3.5	154 MHz	3	44 MHz
0011_011	66/33 MHz	2/4	133 MHz	4	176 MHz	3	44 MHz
0011_100	66/33 MHz	2/4	133 MHz	4.5	198 MHz	3	44 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode[1] (Continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[2][3]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[4]	Bus Division Factor	60x Bus Frequency[5]
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	3	66 MHz
0100_001	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
0100_010	66/33 MHz	3/6	200 MHz	3.5	233 MHz	3	66 MHz
0100_011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz
0100_100	66/33 MHz	3/6	200 MHz	4.5	300 MHz	3	66 MHz
0101_000[6]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	66 MHz
0101_001[6]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[6]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[6]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[6]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode(1) (Continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)(2)(3)	CPM Multiplication Factor(2)	CPM Frequency	Core Multiplication Factor	Core Frequency(4)	Bus Division Factor	60x Bus Frequency(5)
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

Notes:
1. The user should verify that all buses and functions run frequencies that are within the supported ranges.
2. The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2.
3. Input clock frequency is given only for the purpose of reference. MODCK_H–MODCK_L should be set so that the resulting configuration does not exceed the frequency rating of the user’s part.

Example. If a part is rated at 266 MHz CPU, 200 MHz CPM, and 66 MHz bus, any of the following are possible (note that the three input clock frequencies are only three of many possible input clock frequencies):

1. 50 MHz input clock, MODCK_H–MODCK_L[0110–011] (with a core multiplication factor of 4, a CPM multiplication factor of 4, and a bus division factor of 3), and PCI_MODCK = 0 (see note 2 above). The PCI frequency is 50 MHz and the resulting configuration equals the part’s maximum possible frequencies of 266 MHz CPU, 200 MHz CPM, and 66 MHz 60x bus.
2. 66 MHz input clock, MODCK_H–MODCK_L[0100–001], and PCI_MODCK = 1 (see note 2 above) to achieve a PCI frequency of 33 MHz and a configuration of 200MHz CPU, 200 MHz CPM, and 66 MHz 60x bus.
3. 40 MHz input clock, MODCK_H–MODCK_L[1001–011], and PCI_MODCK = 0 (see note 2 above) to achieve a PCI frequency of 40 MHz and a configuration of 160 MHz CPU, 160 MHz CPM, and 40 MHz 60x bus.

Note that with each of the examples, any one of several values for MODCK_H–MODCK_L could possibly be used as long as the resulting configuration does not exceed the part’s rating.

4. Core frequency = (60x bus frequency) (core multiplication factor)
5. Bus frequency = CPM frequency/bus division factor
6. In this mode, PCI_MODCK must be “1”.

Package Description

The following sections provide the package parameters and mechanical dimensions for the PC8265A.

Package Parameters

Package parameters are provided in Table 20. The package type is a 37.5 x 37.5 mm, 480-lead TBGA.

Table 20. Package Parameters

Parameter	Value
Package Outline	37.5 x 37.5 mm
Interconnects	480 (29 x 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

Status

Table 21. Datasheet Status

Datasheet Status		Validity
Objective Specification	This datasheet contains target and goal specification for discussion with customer and application validation.	Valid before design phase
Target Specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary Specification ∝ Site	This datasheet contains preliminary data. Additional data may be published later. This could include simulation results.	Valid before the characterization phase
Preliminary Specification β Site	This datasheet also contains characterization results.	Valid before the industrialization phase.
Product Specification	This datasheet contains final product specifications.	Valid for production purposes

Limiting Values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application Information

Where application information is given, it is advisory and does not form part of the specification.

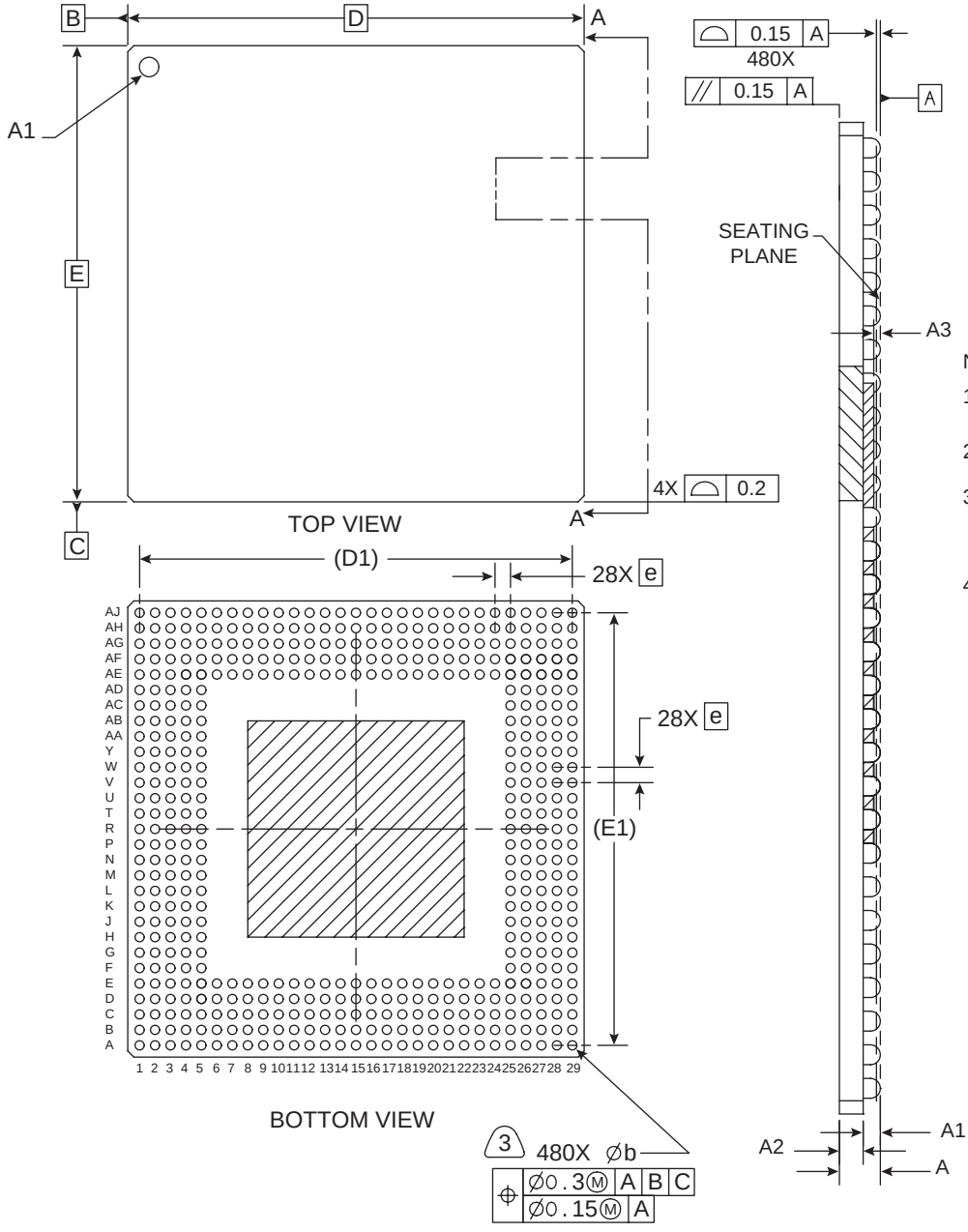
Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

Mechanical Dimensions

Figure 14 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.

Figure 14. Mechanical Dimensions and Bottom Surface Nomenclature

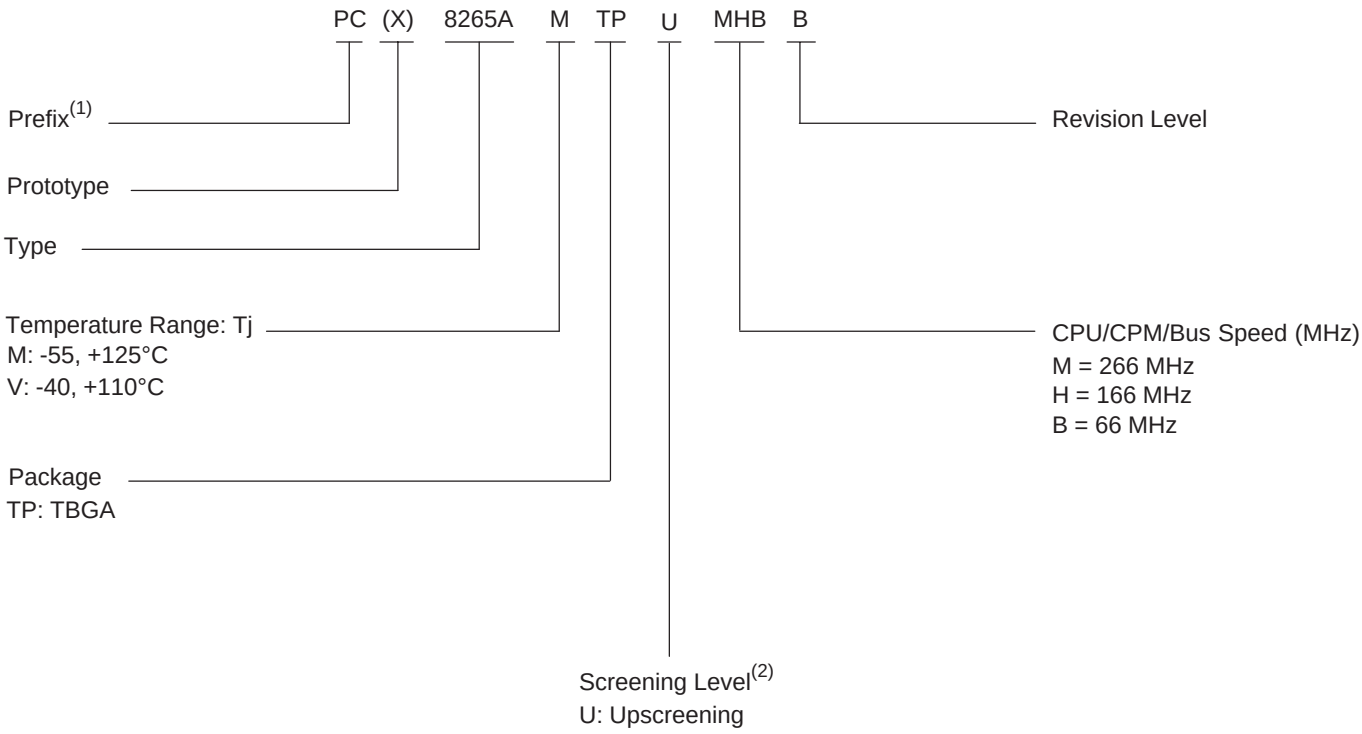


Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994
2. Dimensions in millimeters
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A
4. Primary data A and the seating plane are defined by the spherical crowns of the solder balls

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	_
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Ordering Information



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