Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

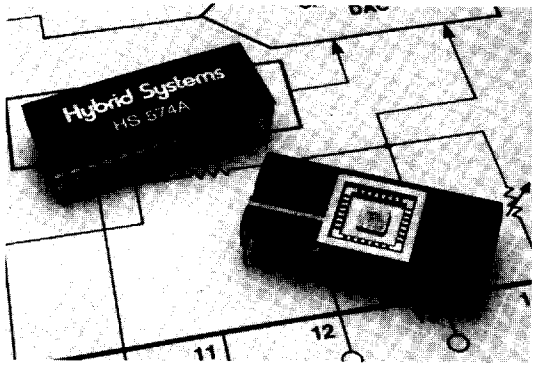
HS574A

COMPLETE 12-BIT, 25μSEC A/D CONVERTER WITH μP INTERFACE

T-51-10-12

FEATURES

- Complete 12-bit A/D converter with sample-hold, reference, clock, and three state outputs
- Low power dissipation: 150mW max
- 12-bit linearity over temperature
- Fast conversion time: 25μSec max
- Monolithic construction



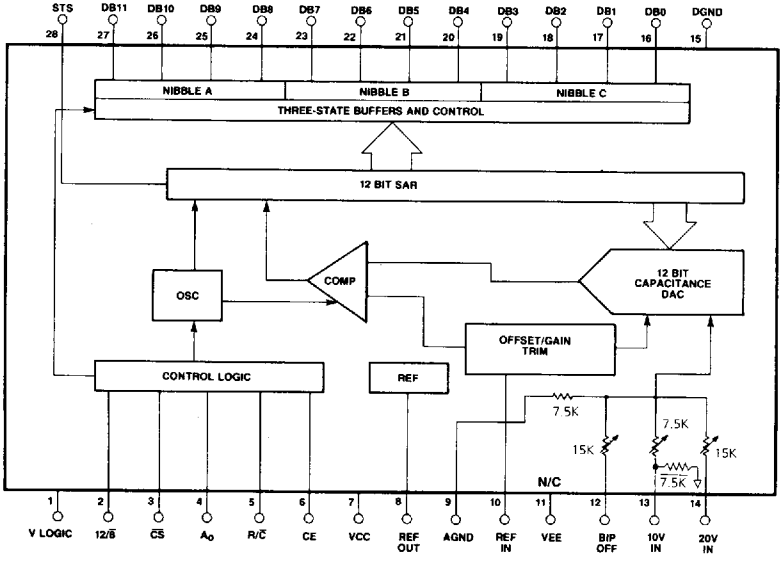
DESCRIPTION

The HS574A is a complete 12-bit successive-approximation A/D converter with three-state output buffers for direct interface to 8-, 12- or 16-bit microprocessor buses. The device is integrated on a single die and includes an internal reference, clock and a sample-hold.

The HS574A has standard bipolar and unipolar input ranges of 10V and 20V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy. Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative supply is not required. Conversion time of 25μSec (max) is also featured.

The HS574A is available in 9 product grades. The HS574AJ, AK and AL are specified over a 0°C to +70°C temperature range; the HS574AA, AB and AC: −40°C to +85°C; and the HS574AS, AT and AU: −55°C to +125°C. Processing in accordance with MIL-STD-883C is also available.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

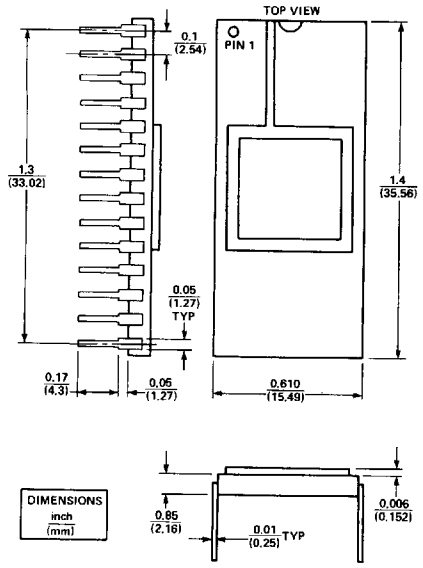
(Typical @ +25°C with V_{CC} = +15V, V_{EE} = 0V, V_{LOGIC} = +5V unless otherwise specified)

MODEL	HS 574AJ	HS 574AK	HS 574AL	HS 574AS	HS 574AT	HS 574AU
RESOLUTION (max)	12 Bits	*	*	*	*	*
TYPE	Successive Approximation	*	*	*	*	*
ANALOG INPUTS						
Input Ranges						
Bipolar	±5V, ±10V	*	*	*	*	*
Unipolar	0 to +10V, 0 to +20V	*	*	*	*	*
Input Impedance						
10 Volt Span	3.75kΩ min, 6.25kΩ max	*	*	*	*	*
20 Volt Span	15kΩ min, 25kΩ max	*	*	*	*	*
DIGITAL INPUTS						
Logic Inputs						
CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$						
Logic 1	+2.4V min, +5.5V max	*	*	*	*	*
Logic 0	−0.3V min, +0.8V max	*	*	*	*	*
Current						
−0.3V to 5.5V Input	±0.1μA typ, ±50μA max	*	*	*	*	*
0 to 5.5V Input	±5μA max	*	*	*	*	*
Capacitance	5pF	*	*	*	*	*
Control Input, 12/$\overline{8}$	Hardwire to V_{LOGIC} or DIG COM	*	*	*	*	*
DIGITAL OUTPUTS						
Logic Outputs						
DB_{11}-DB_0, STS						
Logic 0	+0.4V max, I_{SINK} ≤1.6mA	*	*	*	*	*
Logic 1	+2.4V min, I_{SOURCE} ≤ 500μA	*	*	*	*	*
Leakage (High Z State)	±40μA max (Data Bits Only)	*	*	*	*	*
Capacitance	5pF	*	*	*	*	*
Parallel Data						
Output Codes						
Unipolar	Positive True Binary	*	*	*	*	*
Bipolar	Positive True Offset Binary	*	*	*	*	*
REFERENCE						
Internal	10.00 ±0.1 Volts max	*	*	*	*	*
Output Current[1]	2mA	*	*	*	*	*
CONVERSION TIME						
12-bit	13μSec min, 25μSec max	*	*	*	*	*
8-bit	10μSec min, 19μSec max	*	*	*	*	*
ACCURACY						
Linearity Error @25°C	±1 LSB	±½ LSB	±½ LSB	±1 LSB	±½ LSB	±½ LSB
(t_{min} to t_{max})	±1 LSB	±½ LSB	±½ LSB	±1 LSB	±½ LSB	±½ LSB
Differential Linearity Error[2] @25°C	11 Bits	12 Bits	12 Bits	11 Bits	12 Bits	12 Bits
(t_{min} to t_{max})	11 Bits	12 Bits	12 Bits	11 Bits	12 Bits	12 Bits
Offset[3]						
Unipolar	±2 LSB	*	*	*	*	*
Bipolar	±10 LSB	±4 LSB	±4 LSB	±10 LSB	±4 LSB	±4 LSB
Full Scale Calibration Error (% of FSR)						
Fixed 50Ω resistor from REF OUT to REF IN	0.3%	*	*	*	*	*
No Adjustment at +25°C t_{min} to t_{max}	0.5%	0.4%	0.35%	0.8%	0.6%	0.4%
With Adjustment at +25°C t_{min} to t_{max}	0.22%	0.12%	0.05%	0.5%	0.25%	0.12%
STABILITY						
Unipolar Offset (ppm/°C max)						
0°C to +70°C	±10	±5	±5	±5	±2.5	±2.5
−55°C to +125°C						
Bipolar Offset (ppm/°C max)						
0°C to +70°C	±10	±5	±5	±10	±5	±2.5
−55°C to +125°C						
Gain (Scale Factor)(ppm/°C max)						
0°C to +70°C	±50	±27	±10	±50	±25	±12.5
−55°C to +125°C						
POWER SUPPLY						
V_{LOGIC}	+4.5 to +5.5 Volts @ 3mA	*	*	*	*	*
V_{CC}	+11.4 to +16.5 Volts @ 9mA	*	*	*	*	*
Power Dissipation	110mW typ, 150mW max	*	*	*	*	*
POWER SUPPLY REJECTION						
Max. change in full scale calibration						
+13.5V ≤ V_{CC} ≤ +16.5V or +11.4V ≤ V_{CC} ≤ 12.6V	±2 LSB	±1 LSB	±1 LSB	±2 LSB	±1 LSB	±1 LSB
+4.5V ≤ V_{LOGIC} ≤ +5.5V	±½ LSB	*	*	*	*	*
TEMPERATURE RANGE						
Operating	0°C to +70°C	*	*	−55°C to +125°C	**	**
Storage	−40°C to +85°C	*	*	−65°C to +150°C	**	**

NOTES: 1. Available for external loads. External load should not change during conversion. When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output. 2. Minimum resolution for which no missing codes are guaranteed. 3. Externally adjustable to zero. See applications information.

*Specifications same as HS 574AJ. **Specifications same as HS 574AS.

PACKAGE OUTLINE



NOTE: See ordering information for Leadless Chip Carrier & CERDIP package outline. Sipex reserves the right to ship CERDIP in lieu of ceramic package.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	V_{LOGIC}	28	STS
2	12/8	27	DB_{11} (MSB)
3	$\overline{CS}$	26	DB_{10}
4	A_0	25	DB_9
5	R/$\overline{C}$	24	DB_8
6	CE	23	DB_7
7	V_{CC}	22	DB_6
8	REF OUT	21	DB_5
9	ANA GND(AC)	20	DB_4
10	REF IN	19	DB_3
11	N/C*	18	DB_2
12	BIP OFF	17	DB_1
13	$10V_{IN}$	16	DB_0 (LSB)
14	$20V_{IN}$	15	DIGITAL GND

*This pin is not connected inside the device so it can be tied to −15V, ground, or left floating.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, CS, A_0, 12/8, R/C) to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering ..... 300°C, 10Sec
J/C ..... 45°C/W
MTBF-25°C Ground Base ..... 2.915 million hours
MTBF-125°C Missile Launch ..... 10.16 thousand hours

CONVERT MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = +15V or +10V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	TEST CONDITIONS[1]	MIN	MAX	UNITS
t_{DSC} STS Delay from CE			200	ns
t_{HEC} CE Pulse Width		50		ns
t_{SSC} $\overline{CS}$ to CE Setup		50		ns
t_{HSC} $\overline{CS}$ Low during CE high		50		ns
t_{SRC} R/$\overline{C}$ to CE Setup		50		ns
t_{HRC} R/$\overline{C}$ Low during CE High		50		ns
t_{SAC} A_0 to CE Setup		0		ns
t_{HAC} A_0 Valid During CE High		50		ns
t_C Conversion Time				
12-Bit Cycle[3]	T_{min} to T_{max}	13	25	µs
8-Bit Cycle[3]	T_{min} to T_{max}	10	19	µs

NOTES:
1. Parameters guaranteed by design and sample tested.
2. Parameters 100% tested @25°C on special orders.
3. 100% tested

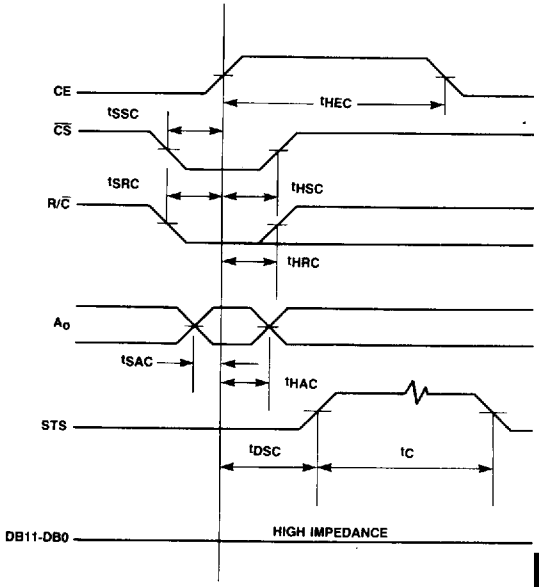


Figure 1. Convert Mode Timing Diagram

READ MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	MIN	TYP	MAX	UNITS
t_{DD} Access Time From CE[2]			150	ns
t_{HD} Data Valid After CE Low[2]	25			ns
t_{HL} Output Float Delay[2]			150	ns
t_{SSR} $\overline{CS}$ to CE Setup	50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup	0	0		ns
t_{SAR} A_0 to CE Setup	50			ns
t_{HSR} CS Valid After CE Low	0	0		ns
t_{HRR} R/$\overline{C}$ High After CE low	0	50		ns
t_{HAR} A_0 Valid After CE low	50			ns
t_{HS} STS Delay After Data Valid	300		1000	ns

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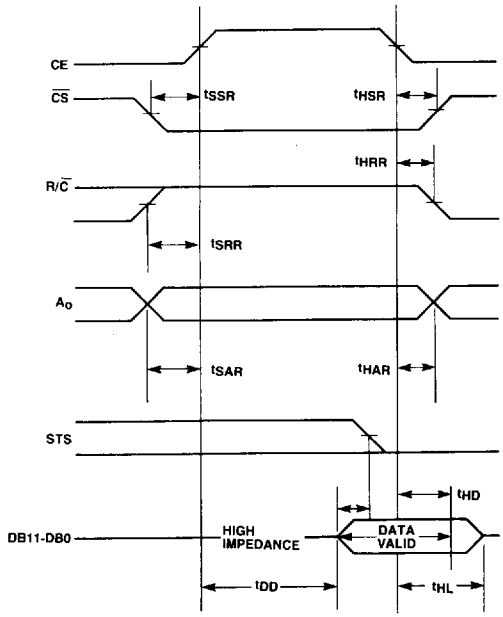

Figure 2. Read Mode Timing Diagram

STAND-ALONE MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL} Low R/C Pulse Width[2]	50			ns
t_{DS} STS Delay from R/C[2]			200	ns
t_{HDR} Data Valid After R/C Low[2]		25		ns
t_{HS} STS Delay After Data Valid[2]	300		1000	ns
t_{HRH} High R/C Pulse Width	150			ns
t_{DDR} Data Access Time			150	ns

NOTES:
1. Parameters guaranteed by design and sample tested.
2. Parameters 100% tested @25°C on special orders.

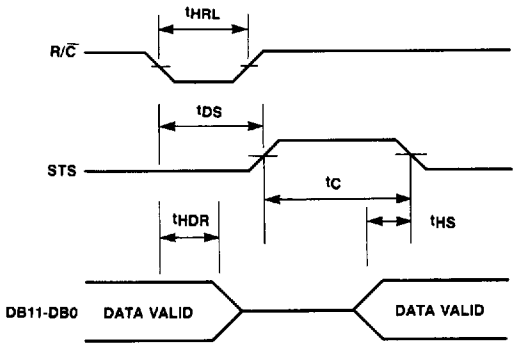

Figure 3. Low Pulse For R/C — Outputs Enabled After Conversion

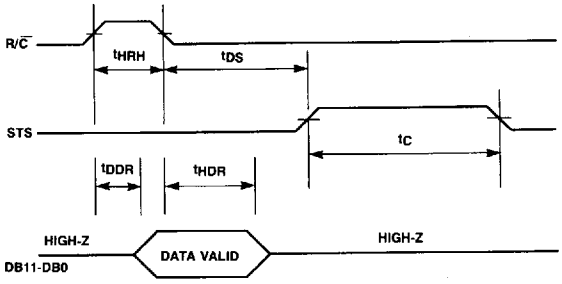

Figure 4. High Pulse For R/C — Outputs Enabled While R/C is High, Otherwise High Impedance

CIRCUIT OPERATION

The HS 574A is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 574. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive-approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make it possible to use the HS 574A with few external components.

When the control section of the HS 574A initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HS 574A 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±½ LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with ±15V supplies. If the HS 574A is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the HS 574A reference must remain constant during conversion.

The sample and hold is a default function by virtue of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although there is no sample–and–hold circuit in the classical sense, the sampling nature of the capacitive DAC makes the HS574A appear to have a built in sample and hold. This sample and hold action substantially increases the usefulness of the HS574A over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HS 574A is disconnected from the input. This prevents transients occurring during conversion from being inflicted upon the attached buffer. All other 574/674 circuits will cause a transient load current on the input which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the HS 574A allows the user an opportunity to release the hold on an external sample–and–hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HS 574A acts as any other 574 device because the internal S/H is transparent. The sample/hold function in the HS 574A is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for MUX operation, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HS 574A and is controlled through the normal R/C control line (refer to Figure 5.) When the R/C line makes a negative transition, the HS 574A starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acqusition of the input by the CDAC (this time is defined as t_{ACQ}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Note that because the sample is taken relative to the R/C transition, t_{ACQ} is also the traditional "aperture delay" of this internal sample and hold.

Since t_{ACQ} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in t_{ACQ} = 2.9µsec ±1.1µsecs between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HS 574A.

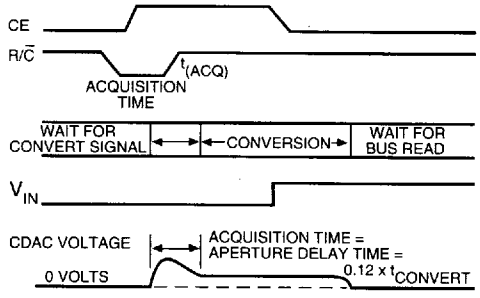

Figure 5. Sample and Hold Function

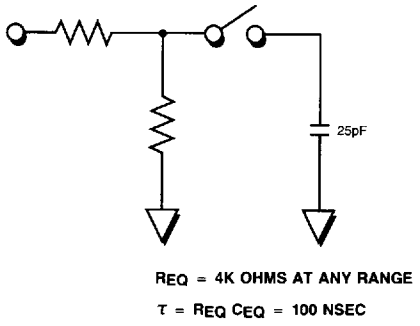

Figure 6. Equivalent HS 574A Input Circuit

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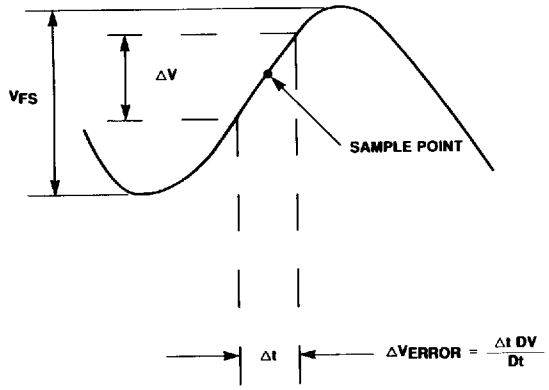

Figure 7. Aperture Uncertainty

TYPICAL INTERFACE CIRCUIT

The HS 574A is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figures 8 and 9. The two typical interface circuits are for operating the HS 574A in either a unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HS 574A must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 μF tantalum and a 0.1 μF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HS 574A is being used to upgrade an already existing design.

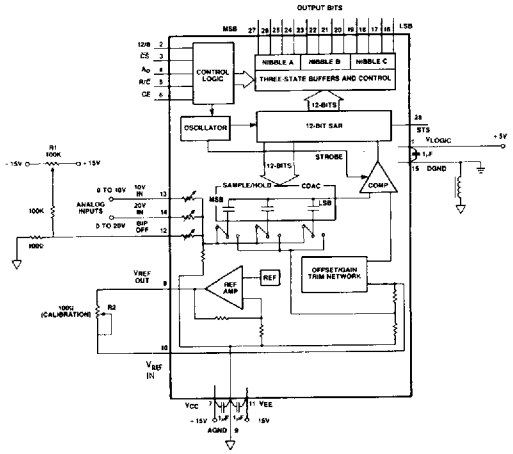

Figure 8. Unipolar Input Connections

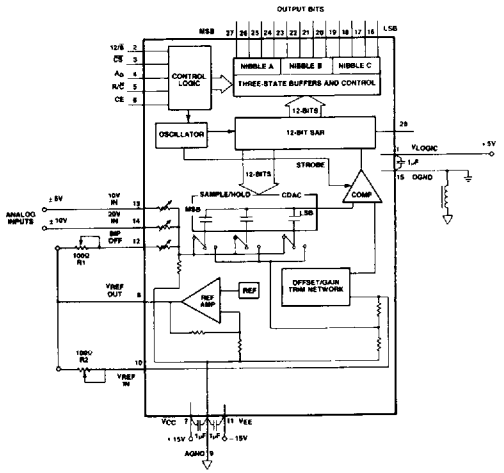

Figure 9. Bipolar Input Connections

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accomodate the ground currents present with this device.

The analog ground current is approximately 6mADC while the digital ground is 3mADC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HS 574A may be operated by a μP or in the stand-alone mode. The part has four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 8, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +½ LSB or +1.22mV for the 10V range and +2.44mV for the 20V range should be applied to the HS 574A. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1½ LSB below the nominal full scale which is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

BIPOLAR

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R1 and R2 (See Figure 9). If adjustment is not needed, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5V range or to pin 14 for a ±10V range. First apply a DC input voltage ½ LSB above negative full scale which is −4.9988V for the ±5V range or −9.9976V for the ±10V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½ LSB below positive full scale which is +4.9963V for the ±5V range or +9.9927V for the ±10V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

The 100Ω potentiometer R2 provides gain adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (for and LSB of 2.5mV) or 20.48 (for an LSB of 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then to provide gain adjust for the 10.24 range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 1000Ω potentiometer in series with pin 14.

CONTROLLING THE HS 574A

The HS 574A can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/C input pin. Full μP control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/8, CS, A_0, R/C and CE. The use of these inputs in controlling the converter's operations is shown in Table 1, and the internal control logic is shown in a simplified schematic in Figure 10.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/C. The other controls must be tied to known states as follows: CE and 12/8 are wired high, A_0 and CS are wired low. The output data arrives in words of 12-bits each. The limits on R/C duty cycle are shown in Figures 3 and 4. It may have duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress.

CONVERSION LENGTH

A conversion start transition latches the state of A_0 as shown in Figure 10 and Table 1. The latched state determines if the conversion stops with 8-bits (A_0 high) or continues for 12-bits (A_0 low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". A_0 is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

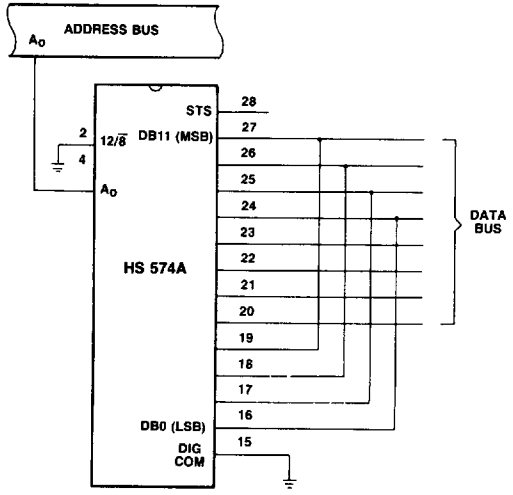

Figure 10. Interfacing the HS 574A to an 8-Bit Data Bus

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CONVERSION START

A conversion may be initated by a logic transition on any of the three inputs: CE, CS, R/C, as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if A_0 changes state after a conversion begins, an additional Start Convert command will latch the new state of A_0 and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

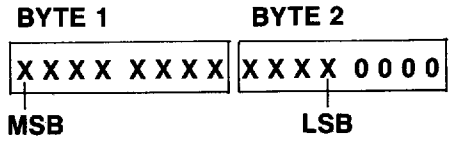
READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/C is high, STS is low, CE is high and CS is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/8 and A_0. The timing diagram for this process is shown in Figure 2. When 12/8 is high, all 12 data outputs become active simultaneously and the A_0 input is ignored. This is for easy interface to a 12 or 16 bit data bus. The 12/8 input is usually tied high or low, although it is TTL/CMOS compatible.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 Bit Conversion
↑	0	0	X	1	Initiate 8 Bit Conversion
1	↓	0	X	0	Initiate 12 Bit Conversion
1	↓	0	X	1	Initiate 8 Bit Conversion
1	0	↓	X	0	Initiate 12 Bit Conversion
1	0	↓	X	1	Initiate 8 Bit Conversion
1	0	1	1	X	Enable 12 Bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Table 1. Truth Table for the HS 574 Control Inputs

When 12/8 is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 10. The A_0 control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When A_0 is pulled low, the 8 MSB's are enabled only. When A_0 is high, the 4 MSB's are disabled, bits 4 through 7 are forced to a zero and the four LSB's are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

A_0 may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 10 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.

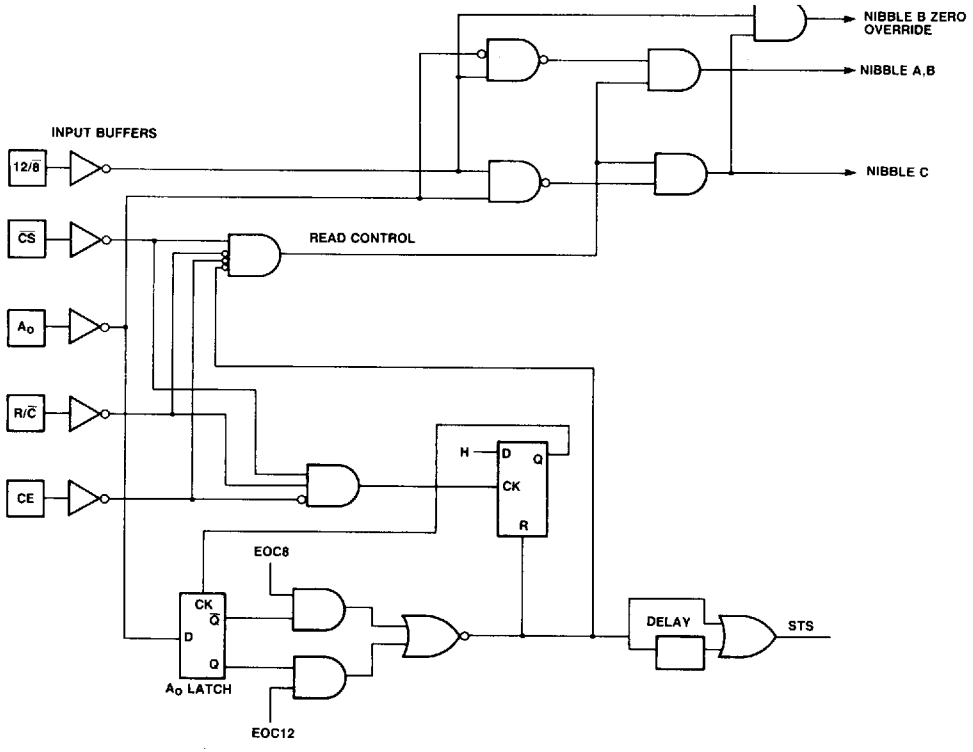


Figure 11. HS 574A Control Logic

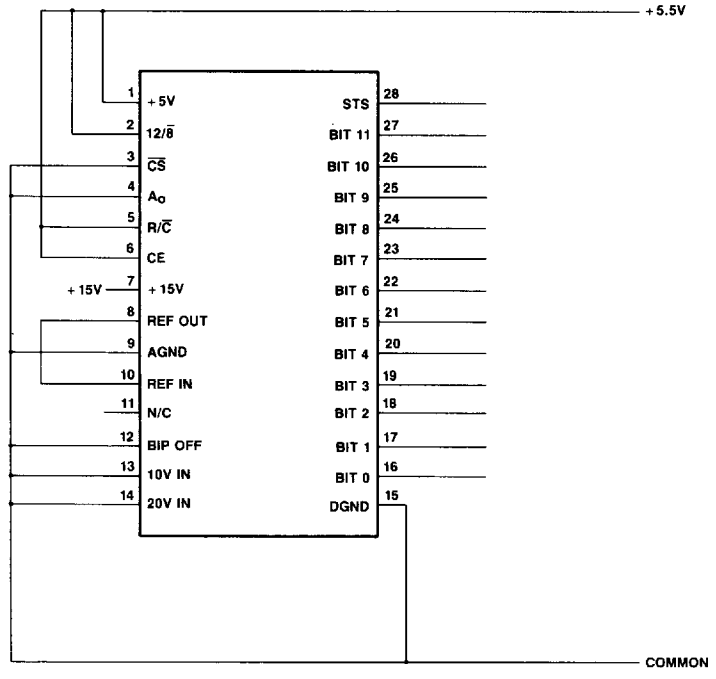


Figure 12. Burn-In Schematic

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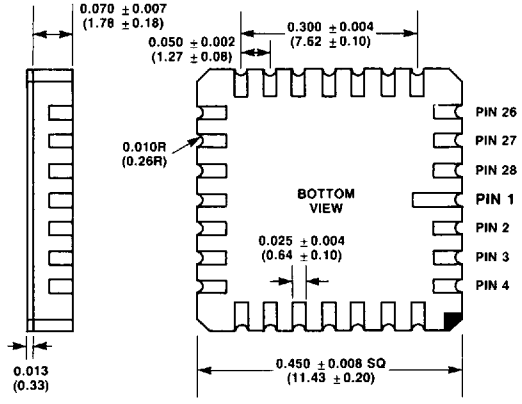
ORDERING INFORMATION

MODEL NUMBER	RESOLUTION NO MISSING CODES (T_{min} to T_{max})	LINEARITY ERROR	MAX FULL SCALE T.C. (ppm/°C)	TEMP. RANGE	MIL SCREENING
HS 574AJ	11 Bits	±1 LSB	50.0	0°C to +70°C	—
HS 574AK	12 Bits	±½ LSB	27.0	0°C to +70°C	—
HS 574AL	12 Bits	±½ LSB	10.0	0°C to +70°C	—
HS 574AA[1]	11 Bits	±½ LSB	50.0	−40°C to +85°C	—
HS 574AB[1]	12 Bits	±½ LSB	27.0	−40°C to +85°C	—
HS 574AC[1]	12 Bits	±½ LSB	10.0	−40°C to +85°C	—
HS 574AS	11 Bits	±1 LSB	50.0	−55°C to +125°C	—
HS 574AT	12 Bits	±½ LSB	25.0	−55°C to +125°C	—
HS 574AU	12 Bits	±½ LSB	12.5	−55°C to +125°C	—
HS 574AS/B	11 Bits	±1 LSB	50.0	−55°C to +125°C	MIL-STD-883C
HS 574AT/B	12 Bits	±½ LSB	25.0	−55°C to +125°C	MIL-STD-883C
HS 574AU/B	12 Bits	±½ LSB	12.5	−55°C to +125°C	MIL-STD-883C

NOTE: 1.Electrical specifications for AA, AB, and AC grades are the same as AJ, AK, and AL models, respectively with the exception of extended operating temperature range performance from −40°C to +85°C.

PACKAGE OUTLINE

28 Pin Leadless Chip Carrier



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.018	0.20	0.46	7
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015		0.38		3
S		0.100		2.54	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTE: To order Leadless Chip Carrier version add /LCC suffix to model number.