REVISIONS			
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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
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DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE
FOR USE BY ALL DEPARTMENTS
AND AGENCIES OF THE
DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
RAJESH PITHADIA

APPROVED BY
RAYMOND MONNIN

DRAWING APPROVAL DATE
97-11-21

REVISION LEVEL

MICROCIRCUIT, LINEAR, HIGH POWER FACTOR PREREGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-97630**

SHEET 1 OF 12

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	97630	01	Q	P	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
Drawing number						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UC1852	High power factor preregulator

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage (V_{CC}) (low impedance source)	30.0 V
Supply current (I_{CC}) (high impedance source)	30.0 mA
Peak output current (I_{OUT})	±1.0 A
Output energy, capacitive load	5.0 µJ
Input voltage, ISNS	±5.0 V
Feedback input voltage (V_{FB})	-0.3 V to +10.0 V
COMPARATOR current (I_{COMP})	±10.0 mA
I_{SET} current	-10.0 mA
Power dissipation (P_D) at $T_A = +25°C$	1.0 W
Storage temperature	-65° C to +150° C
Lead temperature (soldering, 10 seconds)	+300° C
Junction temperature (T_J)	+185° C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA})	160° C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	24.0 V
Ambient operating temperature range (T_A)	-55° C to +125° C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages with respect to ground.
3/ All currents are positive into the specified terminal.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -	List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 -	Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Timer section							
ISET voltage	V_{ISET}		1,2,3	01	4.5	5.5	V
RAMP charge current	I_{CH}	RAMP pin = 2.5 V	1,2,3	01	88	108	µA
RAMP discharge current	I_{DIS}	ISNS pin = -1.0 V, RAMP pin = 1.0 V	1,2,3	01	12	50	mA
RAMP saturation voltage	V_{SAT}	ISNS pin = -1.0 V, IRAMP = 100 µA	1,2,3	01		0.200	V
RAMP threshold voltage (maximum frequency)	V_{TH}	V_{FB} = 10 V, COMP = open	1,2,3	01	0.92	1.12	V
RAMP threshold voltage (PWM comparator)	V_{TH}		1,2,3	01	3.9	4.8	V
Current sense comparator							
ISNS restart threshold voltage	V_{TH}		1,2,3	01	-18	-4	mV
ISNS fault threshold voltage	V_{TH}		1,2,3	01	-550	-350	mV
ISNS input current	I_{IN}		1,2,3	01	-100	100	µA
Error amplifier section							
V_{FB} input voltage	V_{IN}		1,2,3	01	4.6	5.3	V
V_{FB} input bias current	I_{IB}		1,2,3	01	-5.0	5.0	µA
COMP sink current	I_{SI}	COMP pin = 7.5 V	1,2,3	01	10		mA
COMP source current	I_{SO}	COMP pin = 2.5 V	1,2,3	01	-300	-100	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Error amplifier section - continued.							
COMP clamp voltage	V_{CL}	V_{FB} = 0.0 V, COMP = open	1,2,3	01	9.2	10.6	V
OUTPUT section							
OUTPUT saturation voltage high	V_{HSAT}	V_{CC} = 13 V, RAMP = 2 V, I_{OUT} = -200 mA	1,2,3	01	0.5	2.5	V
OUTPUT saturation voltage low	V_{LSAT}	I_{OUT} = 200 mA, ISNS = -1.0 V	1,2,3	01	0.5	2.2	V
OUTPUT saturation voltage low at 10 mA	V_{LSAT}	I_{OUT} = 10 mA, ISNS = -1.0 V	1,2,3	01		0.40	V
OUTPUT clamp voltage	V_{CL}	I_{OUT} = -200 mA, RAMP = 2 V	1,2,3	01	10.0	14.5	V
OUTPUT voltage during under voltage lock out	V_{UVLO}	I_{OUT} = 100 mA, V_{CC} = 0 V	1,2,3	01	0.5	2.2	V
Overall section							
Inactive supply current	I_{INA}	V_{CC} = 10 V	1,2,3	01	0.2	1.0	mA
Active supply current	I_{ACT}		1,2,3	01	3.0	10	mA
V_{CC} clamp voltage		I_{CC} = 25 mA	1,2,3	01	30	36	V
V_{CC} turn-on threshold voltage	V_{ON}		1,2,3	01	14.5	17.5	V
V_{CC} turn-off threshold voltage	V_{OFF}		1,2,3	01	10.5	13.0	V
V_{CC} threshold hysteresis voltage	V_{HYS}		1,2,3	01	3	7	V

1/ Unless otherwise specified, V_{CC} = 24 V, I_{SET} = 50 kΩ to GND, RAMP = 1 nF to GND, ISNS = -0.1 V, VFB pin connected to COMP pin, and no load on the OUTPUT pin.

Device type	01
Case outline	P
Terminal number	Terminal symbol
1	VFB
2	ISNS
3	ISET
4	RAMP
5	GND
6	OUTPUT
7	V_{CC}
8	COMP

FIGURE 1. Terminal connections.

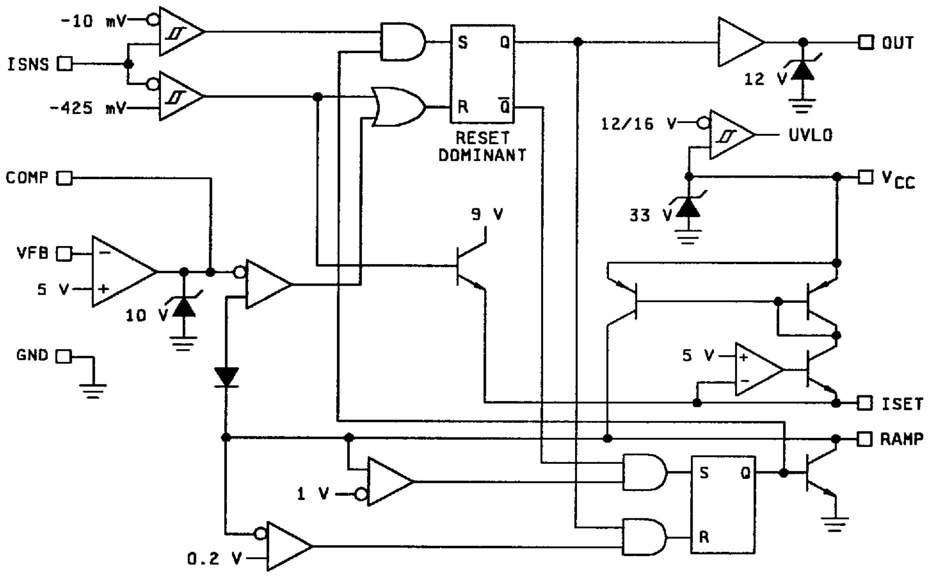

FIGURE 2. Logic diagram.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 52 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

   (1) Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

   (2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3 1/	1,2,3 1/	1,2,3 1/
Group A test requirements (see 4.4)	1,2,3	1,2,3	1,2,3
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, 8, 9,10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25°C \pm 5°C$, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

COMP	COMP is the output of the error amplifier and the input of the pulse width modulator (PWM) comparator. To limit PWM on-time, this pin is clamped to approximately 10 V. To implement soft start, the COMP pin can be pulled low and ramped up with a PNP transistor, a capacitor, and a resistor.
GND	GROUND for all functions is through this pin.
ISET	The first function of this pin is to program RAMP charging current. RAMP charging current is approximately 5 V divided by the external resistor placed from ISET to ground. Resistors in the external in the range of 10 kΩ to 50 kΩ are recommended, producing currents in the range of 100 µA to 500 µA. The second function of ISET is as reference output. The ISET pin is normally regulated to 5 V ±10%. It is critical that this pin only see the loading of the RAMP programming resistor, but a high input-impedance comparator or amplifier may be connected to this pin or tap on the RAMP programming resistor if required. The third function of the ISET pin is as a FAULT output. In the event of an over-current fault, the ISET pin is forced to approximately 9 V by the fault comparator. This can be used to trip an external protection circuit which can disable the load or start a fault restart cycle.
ISNS	This input to the zero and over current comparators is specially built to allow operation over ±5 V dynamic range. In noisy systems or systems with very high Q inductors, it is desirable to filter the signal entering the ISNS input to prevent premature restart or fault cycles.
OUTPUT	The output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±500 mA.
RAMP	A controlled on-time PWM requires a timer whose time can be modulated by an external voltage. The timer current is programmed by a resistor from ISET to GND. A capacitor from RAMP to GND sets the on time in conjunction with the voltage on COMP. Recommended values for the timer capacitors are between 100 pF and 1 nF.
VCC	VCC is the logic and control power connection for this device. VCC current is the sum of active device supply current and the average OUTPUT current.
VFB	VFB is the error amplifier inverting input. This input serves as both the voltage sense input to the error amplifier.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-11-21

Approved sources of supply for SMD 5962-97630 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9763001QPA	48726	UC1852J/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
48726	Unitrode Integrated Circuits Corporation 7 Continental Boulevard Merrimack, NH 03054

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.