REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 03. Editorial changes throughout.	93-09-27	M.A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV	A																			
SHEET	35																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS															
	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

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DRAWING APPROVAL DATE
91-02-06

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, ANALOG INTERFACE CIRCUIT,MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90863

SHEET 1 OF 35

DESC FORM 193
JUL 91

5962-E208-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

74E ■ 9004708 0000227 516 ■

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device class Q and M) and space application (device class V) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

```
    5962            -         90863      01          M           X          X
 ____|_____     ____|____              __|__      ___|___      __|__      __|__
  Federal          RHA                 Device      Device       Case       Lead
stock class    designator               type        class      outline    finish
designator     (see 1.2.1)          (see 1.2.2)   designator (see 1.2.4) (see 1.2.5)
                                                 (see 1.2.3)
\____________________/\_____________________/
                     \/
               Drawing number
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1.2.1 Radiation hardness assurance (RHA) designator. Device class M RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q or V devices shall meet or exceed the electrical performance characteristics specified in table I herein after exposure to the specified irradiation levels specified in the absolute maximum ratings herein and the RHA marked device shall be marked in accordance with MIL-I-38535. A dash (-) indicates a non RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLC32040M	Analog interface circuit
02	TLC32044M	Voice-band analog interface circuit
03	TLC32046M	Wide-band analog interface circuit

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line
3	CQCC1-N28	28	square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Positive analog supply voltage (V_{CC+}) 2/	-0.3 V to 15 V
Digital supply voltage (V_{DD})	-0.3 V to 15 V
Output voltage (V_{OUT})	-0.3 V to 15 V
Input voltage (V_{IN})	-0.3 V to 15 V
Digital ground voltage	-0.3 V to 15 V
Storage temperature range	-65°C to 150°C
Power dissipation (P_D)	4 W
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C
Lead temperature soldering 1.6 mm (1/16 inch) from case for 60 seconds:	+300°C

1.4 Recommended operating conditions.

Positive analog supply voltage (V_{CC+}) 3/	4.75 V minimum to 5.25 V maximum
Negative analog Supply voltage (V_{CC-}) 3/	-4.75 V minimum to -5.25 V maximum
Digital supply voltage (V_{DD}) 3/	4.75 V minimum to 5.25 V maximum
Digital ground voltage with respect to ANLG GND, DGTL GND	0 V nominal
High-level input voltage (V_{IH})	+2.0 V minimum
Low-level input voltage (V_{IL})	+0.8 V maximum
Load resistance at OUT+ and/or OUT- (R_L)	300 Ω minimum
Master clock (MCLK) frequency 4/	10.368 MHz maximum
Load capacitance at OUT+ and/or OUT- (C_L)	100 pF maximum
A/D or D/A conversion rate	16 kHz maximum
Conversion rate	20 kHz
Ambient operating temperature range, (T_A)	-55°C to 125°C
Analog input amplifier common mode input voltage 5/	±1.5 V maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Voltage values for maximum ratings are with respect to V_{CC-}.

3/ Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-}, are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.

4/ For device types 01 and 02, the band-pass and low-pass switched-capacitor filter response specifications apply only when the switched-capacitor clock frequency is 288 kHz. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of the switched-capacitor filter clock frequency to 288 kHz. For device type 03, the band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 16 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 16 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 16 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 288 kHz.

5/ This range applies when (IN+ - IN-) or (AUX IN+ - AUX IN-) equals ± 6 V.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 2.

3.2.4 Internal timing configuration(s). Internal timing configuration(s) shall be as specified on figure 3.

3.2.5 Data word format. Data word format shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 77 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V sampling and inspection procedures shall be in accordance with MIL-I-38535.

4.2 Screening. For device class M screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. For device class M the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le 125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{DD} = 4.75 V, I_{OH} = -300 µA	ALL	1,2,3	2.4		V
Low level output voltage	V_{OL}	V_{DD} = 4.75 V, I_{OL} = 2 mA	ALL	1,2,3		0.4	V
Supply current from V_{CC+}	I_{CC+}		01,02	1,2,3		40	mA
			03			45	
Supply current from V_{CC-}	I_{CC-}		01,02	1,2,3		-40	mA
			03			-45	
Supply current from V_{DD}	I_{DD}		01, 03	1,2,3		7	mA
			02			8	
Internal reference output voltage	V_{REF}		ALL	1,2,3	2.9	3.3	V
Input current	I_I		01,02	1,2,3		±10	µA
A/D converter offset error (filters bypassed), receive amplifier input	OE_B		01	1,2,3		65	mV
A/D converter offset error (filters in), receive amplifier input	OE_I		01	1,2,3		65	mV
			02			85	
			03			70	
Common mode rejection ratio at IN+, IN-, or AUX IN+, AUX IN-, receive amplifier input	CMRR	0-dBm, 1-kHz input signal with an 8-kHz conversion rate	01,02	1,2,3	35		dB
Output offset voltage at OUT+ or OUT- (single ended relative to ANLG GND), transmit filter output	V_{OO}		01	1,2,3		75	mV
			02, 03			85	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq 125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Maximum peak output voltage swing between OUT+ and OUT- (differential output), transmit filter output	V_{OM}	$R_L \geq 300\Omega$	All	1,2,3	±6		V
Absolute transmit gain tracking error while transmitting into 300Ω 2/	TE_T	-48 dB to 0 dB signal range (0 dB relative to V_{REF})	All	4,5,6	- 0.15	+0.15	dB
Absolute receive gain tracking error 2/	TE_R	-48 dB to 0 dB signal range (0 dB relative to V_{REF})	All	4,5,6	- 0.15	+0.15	dB
Transmit noise (differential)	TN_1	DX INPUT = 00000000000000, Constant input code	01	4,5,6		500	µV RMS
Transmit noise with (sin x)/x	TN_2	DX INPUT = 00000000000000, Constant input code	02	4,5,6		575	µV RMS
			03			500	
Transmit noise without (sin x)/x	TN_3	DX INPUT = 00000000000000, Constant input code	02, 03	4,5,6		450	µV RMS
Transmit noise with (sin x)/x	TN_4	DX INPUT = 00000000000000, Constant input code f = 0 to 30 kHz	03	4,5,6		400	µV RMS
Transmit noise without (sin x)/x	TN_5						
Transmit noise with (sin x)/x	TN_6	DX INPUT = 00000000000000, Constant input code f = 0 to 3.4 kHz	03	4,5,6		300	µV RMS
Transmit noise without (sin x)/x	TN_7						
Transmit noise with (sin x)/x	TN_8	DX INPUT = 00000000000000, Constant input code f = 0 to 6.8 kHz (wideband operation with 7.2 kHz roll-off)	03	4,5,6		350	µV RMS
Transmit noise without (sin x)/x	TN_9						

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le 125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Receive noise 3/	RN	Inputs grounded, gain = 1	01	4,5,6		475	µV RMS
			02, 03			500	
Crosstalk attenuation, transmit-to-receive (full differential)	CA_{T-R}	DX INPUT = 00000000000000	01	4,5,6	70		dB
			02		65		
			03		60		
Crosstalk attenuation, receive-to-transmit	CA_{R-T}	Inputs grounded, gain = 1, 2, and 4	01, 03	4,5,6	70		dB
			02		65		
Attenuation of second harmonic of A/D input signal, single ended	HA_1	SCF clock frequency = 288 kHz V_{IN} = -0.5 dB to -24 dB referred to V_{REF} 2/, T_A = +25°C	01, 02	4	62		dB
Attenuation of second harmonic of A/D input signal, differential	HA_2	SCF clock frequency = 288 kHz V_{IN} = -0.5 dB to -24 dB referred to V_{REF} 2/	ALL	4,5,6	62		dB
Attenuation of third and higher harmonics of A/D input signal, single ended	HA_3	SCF clock frequency = 288 kHz V_{IN} = -0.5 dB to -24 dB referred to V_{REF} 2/ T_A = +25°C	01,02	4	57		dB
Attenuation of third and higher harmonics of A/D input signal, differential	HA_4	SCF clock frequency = 288 kHz V_{IN} = -0.5 dB to -24 dB referred to V_{REF} 2/	ALL	4,5,6	57		dB
Attenuation of second harmonic of D/A input signal (full differential)	HA_5	SCF clock frequency = 288 kHz V_{IN} = 0 dB to -24 dB referred to V_{REF} 2/	ALL	4,5,6	62		dB
Attenuation of third and higher harmonics of D/A input signal (full differential)	HA_6	SCF clock frequency = 288 kHz V_{IN} = 0 dB to -24 dB referred to V_{REF} 2/	ALL	4,5,6	57		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq 125°C$ unless otherwise specified	A_V=	Device type	Group A subgroups	Limits Min	Limits Max	Unit
A/D channel signal-to-distortion ratio	DR_{A-D}	$-6\ dB \leq V_{IN} < -.5\ dB$	1,2,4	ALL	4,5,6	58		dB
		$-12\ dB \leq V_{IN} < -6\ dB$	1,2,4	ALL		58		
		$-18\ dB \leq V_{IN} < -12\ dB$	1	ALL		56		
			2,4	ALL		58		
		$-24\ dB \leq V_{IN} < -18\ dB$	1	ALL		50		
			2	ALL		56		
			4	ALL		58		
		$30\ dB \leq V_{IN} < -24\ dB$	1	ALL		44		
			2	ALL		50		
			4	ALL		56		
		$-36\ dB \leq V_{IN} < -30\ dB$	1	ALL		38		
			2	ALL		44		
			4	ALL		50		
		$-42\ dB \leq V_{IN} < -36\ dB$	1	ALL		32		
			2	ALL		38		
			4	ALL		44		
		$-48\ dB \leq V_{IN} < -42\ dB$	1	ALL		26		
			2	ALL		32		
			4	ALL		38		
		$-54\ dB \leq V_{IN} < -48\ dB$	1	ALL		20		
			2	ALL		26		
			4	ALL		32		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq 125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
			A_V=					
D/A channel signal-to-distortion ratio 4/ 5/	DR_{D-A}	-6 dB $\leq V_{IN} <$ 0.0 dB	1	ALL	4,5,6	58		dB
		-12 dB $\leq V_{IN} < -6$ dB	1	ALL		58		
		-18 dB $\leq V_{IN} < -12$ dB	1	ALL		56		
		-24 dB $\leq V_{IN} < -18$ dB	1	ALL		50		
		-30 dB $\leq V_{IN} < -24$ dB	1	ALL		44		
		-36 dB $\leq V_{IN} < -30$ dB	1	ALL		38		
		-42 dB $\leq V_{IN} < -36$ dB	1	ALL		32		
		-48 dB $\leq V_{IN} < -42$ dB	1	ALL		26		
		-54 dB $\leq V_{IN} < -48$ dB	1	ALL		20		
Filter gain, bandpass filter transfer function 5/ 6/	FG_{BP}	f = 100 Hz		01	4,5,6		-42	dB
		f = 170 Hz		01			-25	
		300 Hz $\leq$ f < 3.4 kHz		01		-0.5	0.5	
		f = 4 kHz		01			-16	
		f $\geq$ 4.6 kHz		01			-58	
		f $\leq$ 50 Hz		02		-25	-33	
		f = 109 Hz		02		-4	-1	
		172 Hz $\leq$ f < 3.1 kHz		02		-0.25	0.25	
		3.1 kHz $\leq$ f < 3.3 kHz		02		-0.3	0.3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le 125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Filter gain, bandpass filter transfer function 5/ 6/	FG_{BP}	3.3 kHz < f < 3.6 kHz	02	4,5,6	-0.5	0.5	dB
		f = 3.8 kHz	02		-3	-0.5	
		f = 4 kHz	02		-20	-16	
		f = 4.4 kHz	02			-40	
		f = 5 kHz	02			-65	
		f ≤ 100 Hz	03		-33	-25	
		f = 200 Hz	03		-4	-1	
		f = 300 Hz to 6200 Hz	03		-0.25	0.25	
		f = 6200 Hz to 6600 Hz	03		-0.3	0.3	
		f = 6600 Hz to 7300 Hz	03		-0.5	0.5	
		f = 7600 Hz	03		-5.0	-0.5	
		f = 8000 Hz	03		-18	-14	
		f ≥ 8800 Hz	03			-40	
		f ≥ 10000 Hz	03			-65	
Filter gain, low pass transfer function 5/ 6/	FG_{LP}	f ≤ 3.4 kHz	01	4,5,6	-0.5	0.5	dB
		f = 3.6 kHz	01			-4	
		f = 4 kHz	01			-30	
		f ≥ 4.4 kHz	01			-58	
		0 Hz ≤ f < 3.1 kHz	02		-0.25	0.25	
		3.1 kHz ≤ f < 3.3 kHz	02		-0.3	0.3	
		3.3 kHz ≤ f < 3.6 kHz	02		-0.5	0.5	
		f = 3.8 kHz	02		-3	-0.5	
		f = 4 kHz	02		-20	-16	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq 125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Filter gain, low pass transfer function-continued	FG_{LP}	f ≥ 5 kHz	02	4,5,6		-65	dB
		f ≥ 4.4 kHz	02			-40	
		f = 0 Hz to 6200 Hz	03		-0.25	0.25	
		f = 6200 Hz to 6600 Hz	03		-0.3	0.3	
		f = 6600 Hz to 7300 Hz	03		-0.5	0.5	
		f = 7600 Hz	03		-5.0	-0.5	
		f = 8000 Hz	03		-18	-14	
		f ≥ 8800 Hz	03			-40	
		f ≥ 10000 Hz	03			-65	
Master clock (MCLK) cycle time, serial port	$t_{c(MCLK)}$	$T_A = +25°C$ 7/	01,02	9	100	192	ns
			03		95		
RESET pulse duration, serial port 8/	$t_{w(RESET)}$		ALL	9	800		
DX setup time before SCLK falling edge, serial port	$t_{su(DX)}$		ALL	9	28		
DX hold time after SCLK falling edge, serial port	$t_{h(DX)}$		ALL	9	$\frac{t_{c(SCLK)}}{4}$		
Shift clock (SCLK) cycle time, serial port	$t_{c(SCLK)}$		ALL	9	400		
Delay from SCLK rising edge to FSR/FSX falling edge, serial port	$t_{d(CH-FL)}$		01,02			260	
			03			250	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq 125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Delay from SCLK rising edge to FSR/FSX rising edge, serial port	$t_{d(CH-FH)}$	$T_A = +25°C$ 7/	01,02	9		260	ns
			03			250	
DR valid after SCLK rising edge, serial port	$t_{d(CH-DR)}$		01,02			316	
			03			250	
Delay from SCLK rising edge to EODX/EODR falling edge in word mode, serial port	$t_{dw(CH-EL)}$		01,02			280	
			03			250	
Delay from SCLK rising edge to EODX/EODR rising edge in word mode, serial port	$t_{dw(CH-EH)}$		01,02			280	
			03			250	
Delay from SCLK rising edge to EODX/EODR falling edge in byte mode, serial port	$t_{db(CH-EL)}$		03			250	
Delay from SCLK rising edge to EODX/EODR rising edge in byte mode, serial port	$t_{db(CH-EH)}$		03			250	
Delay from MCLK rising edge to SCLK falling edge, serial port	$t_{d(MCH-CL)}$		01,02			105	
			03			170	
Delay from RESET rising edge to SCLK falling edge, serial port	$t_{d(RH-CL)}$		01,02			150	
			03			170	
Delay from RESET rising edge to FSX/FSR falling edge, serial port	$t_{d(RH-FL)}$		01,02			936	

TABLE I. Electrical performance characteristics - Continued.

1/ V_{CC+} = +5 V, V_{CC-} = -5 V, and V_{DD} = 5 V. MCLK frequency = 5.184 MHz and all outputs are not loaded unless otherwise specified.

2/ Gain tracking is relative to the absolute gain at 1 kHz and 0 dB.

3/ This noise is referred to the input with a buffer gain of one. If the buffer gain is two or four, the noise figure will be correspondingly reduced. The noise is computed by statistically evaluating the digital output of the A/D converter.

4/ The test condition is a 1 kHz signal with 8-kHz conversion rate. The load impedance for DAC is 300Ω.

5/ The above filter specifications are for a switched-capacitor filter clock frequency range of 288 kHz ±2 percent. For switched-capacitor filter clocks at frequencies other than 288 kHz ±2 percent, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

6/ The filter gain outside the passband is measured with respect to the gain at 1 kHz for device types 01 and 02 and at 2 kHz for device type 03. The filter gain within the passband is measured with respect to average gain within the passband. The passbands are 300 to 34,000 Hz for device types 01 and 02 and 300 to 7,200 Hz for device type 03 for bandpass filters. The passbands are 0 to 3,400 Hz for device types 01 and 02 and 0 to 7,200 Hz for device type 03 for the low-pass filters. The input signal in bandpass filter gain test condition and the output signal in low-pass filter gain test condition are referenced to 0 dB.

7/ All times are tested in word mode only. However, byte mode timing can be guaranteed by word mode timing. See figure 5.

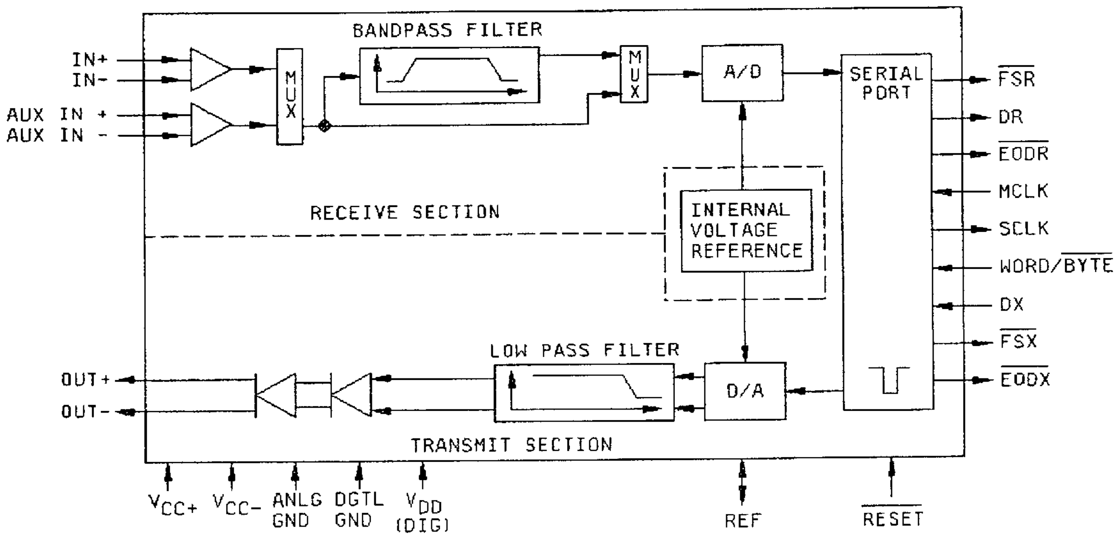
8/ $\overline{RESET}$ pulse duration is the amount of time that the $\overline{RESET}$ pin is held below 0.8 V after the power supplies have reached their recommended values.

Device types	01 and 02	03
Case outlines	X and 3	X and 3
Terminal number	Terminal symbol	Terminal symbol
1	NC	FSD/WORD-BYTE
2	RESET	RESET
3	EODR	EODR
4	FSR	FSR
5	DR	DR
6	MCLK	MCLK
7	V_{DD}	V_{DD}
8	REF	REF
9	DGTL GND	DGTL GND
10	SCLK	SCLK
11	EODX	EODX
12	DX	DX
13	WORD/BYTE	DATA-DR/CONTROL
14	FSX	FSX
15	NC	NC
16	NC	NC
17	ANLG GND	ANLG GND
18	ANLG GND	ANLG GND
19	V_{CC-}	V_{CC-}
20	V_{CC+}	V_{CC+}
21	OUT-	OUT-
22	OUT+	OUT+
23	AUX IN-	AUX IN-
24	AUX IN+	AUX IN+
25	IN-	IN-
26	IN+	IN+
27	NC	NC
28	NC	NC

NC = No connection; no external connection should be made to these pins.

FIGURE 1. Terminal connections.

Device type 01



Device type 02

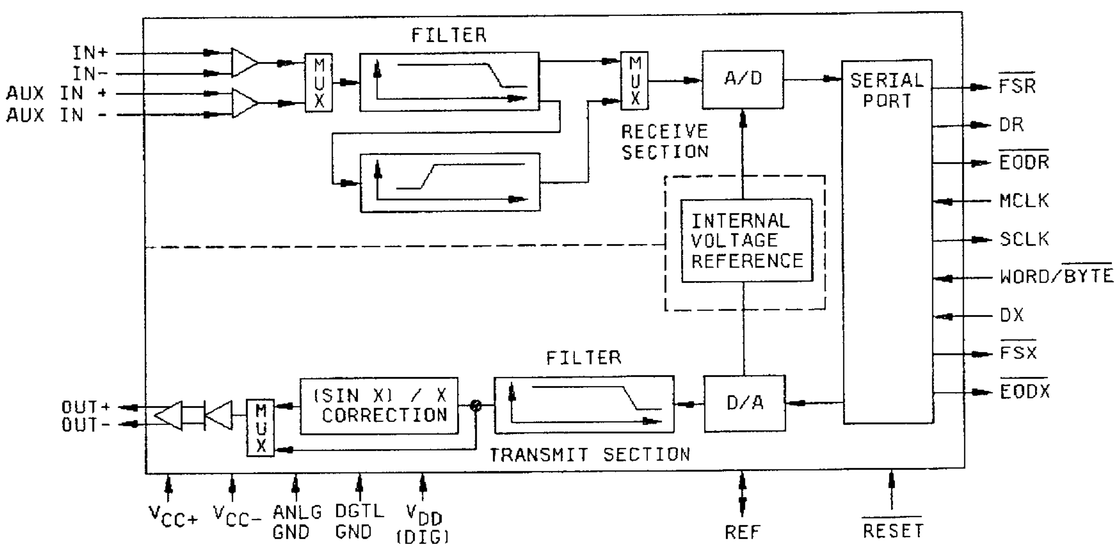
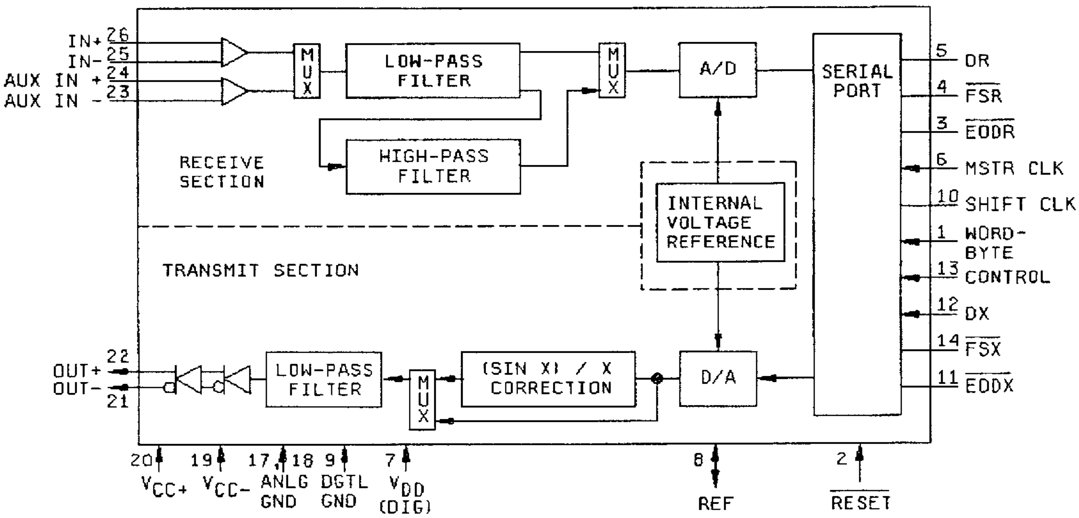


FIGURE 2. Block diagrams.

Device type 03

WORD OR BYTE MODE



DUAL-WORD (TELEPHONE INTERFACE) MODE

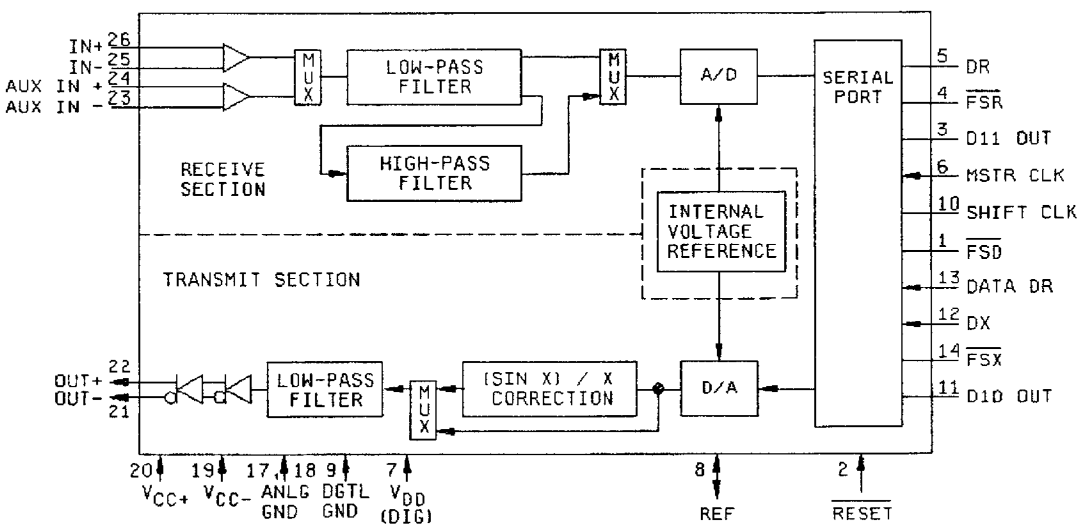
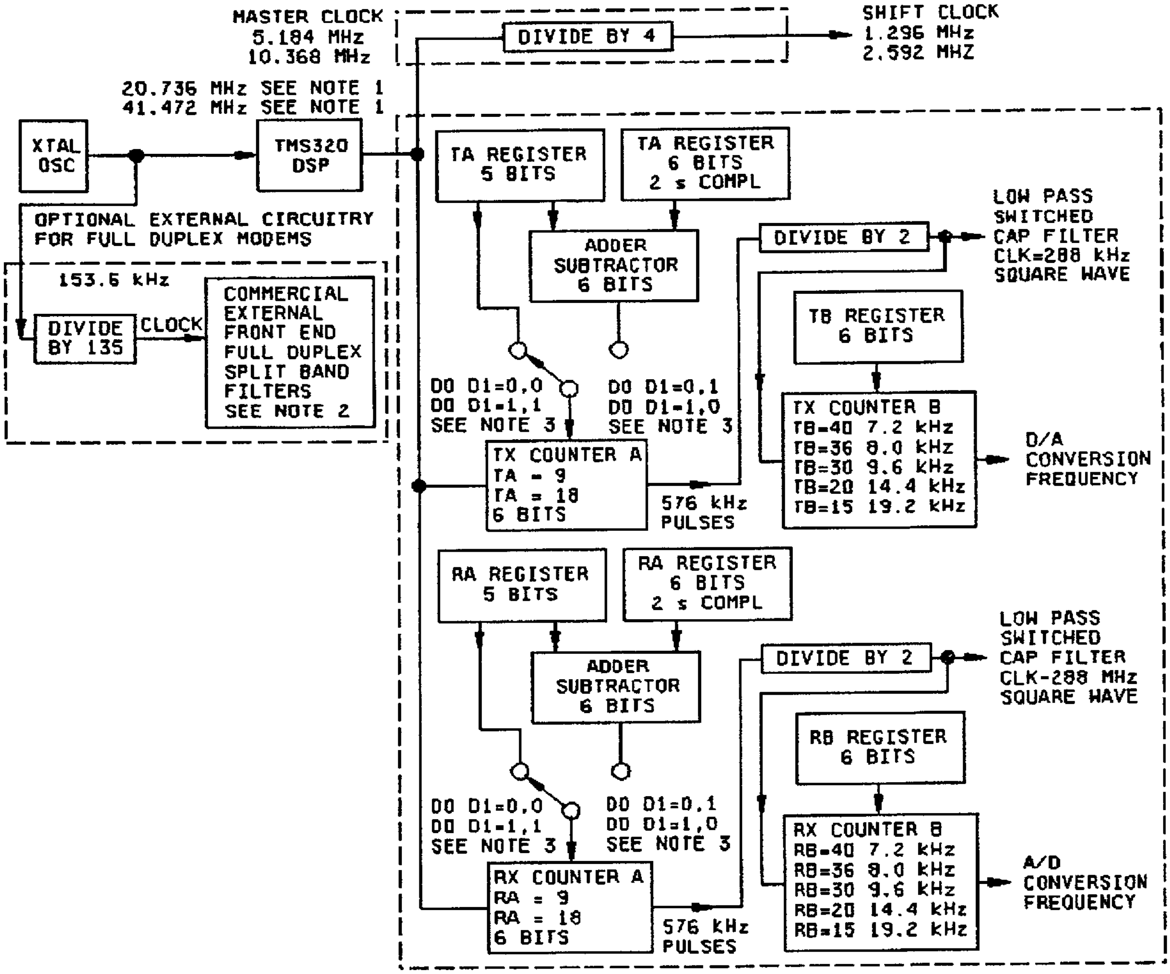


FIGURE 2. Block diagrams - continued.

Device type 01



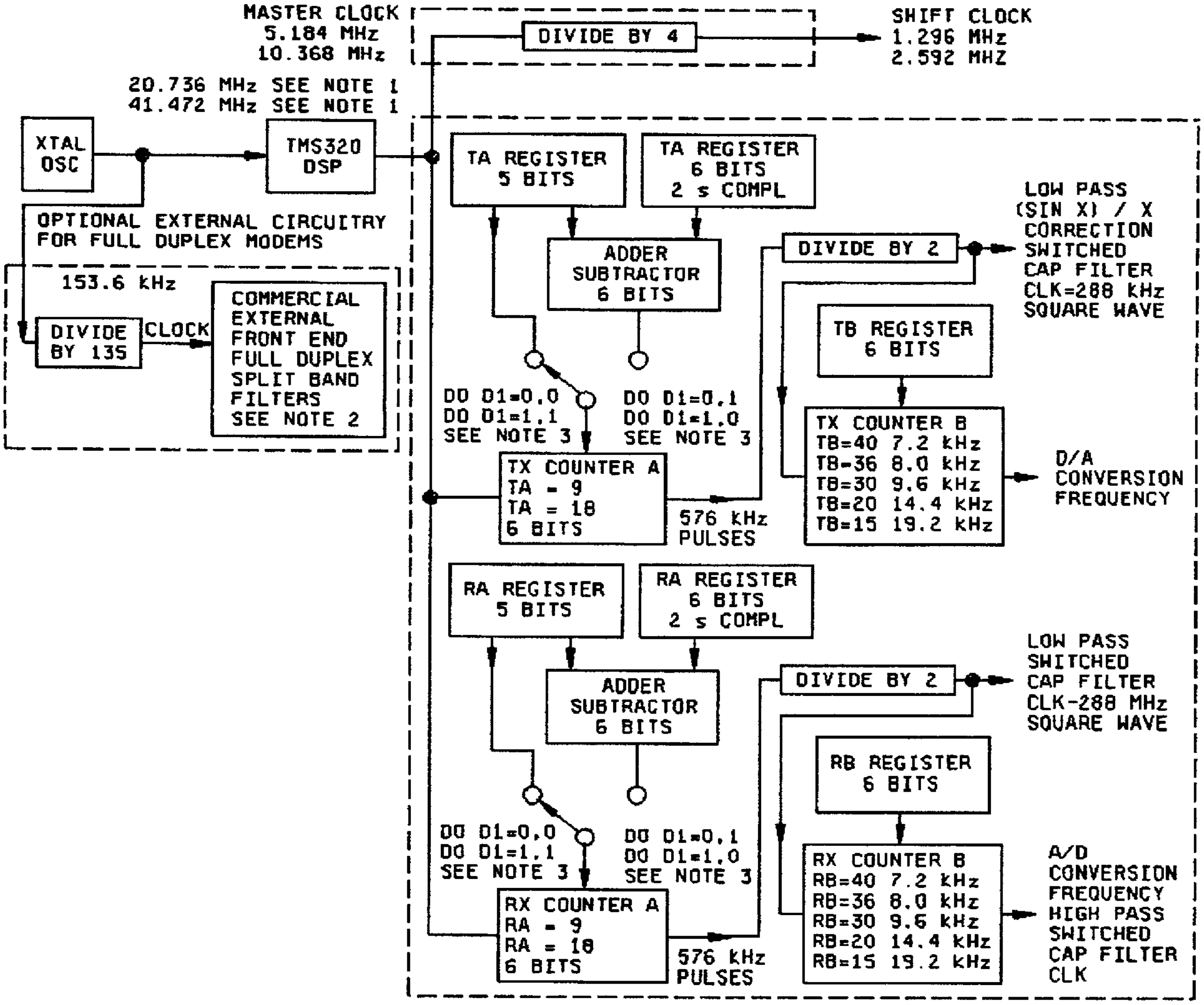
$$\text{SCF CLOCK FREQUENCY} = \frac{\text{MASTER CLOCK FREQUENCY}}{2 \times \text{CONTENTS OF COUNTER A}}$$

NOTES:

1. Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split band filter clock), popular speech and modem sampling signal frequencies, and an internal 288 kHz switched capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high frequency signals, which are used by high-speed digital signal processors.
2. Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.
3. These control bits are described in the AIC DX Data Word Format section.

FIGURE 3. Internal timing configuration.

Device type 02

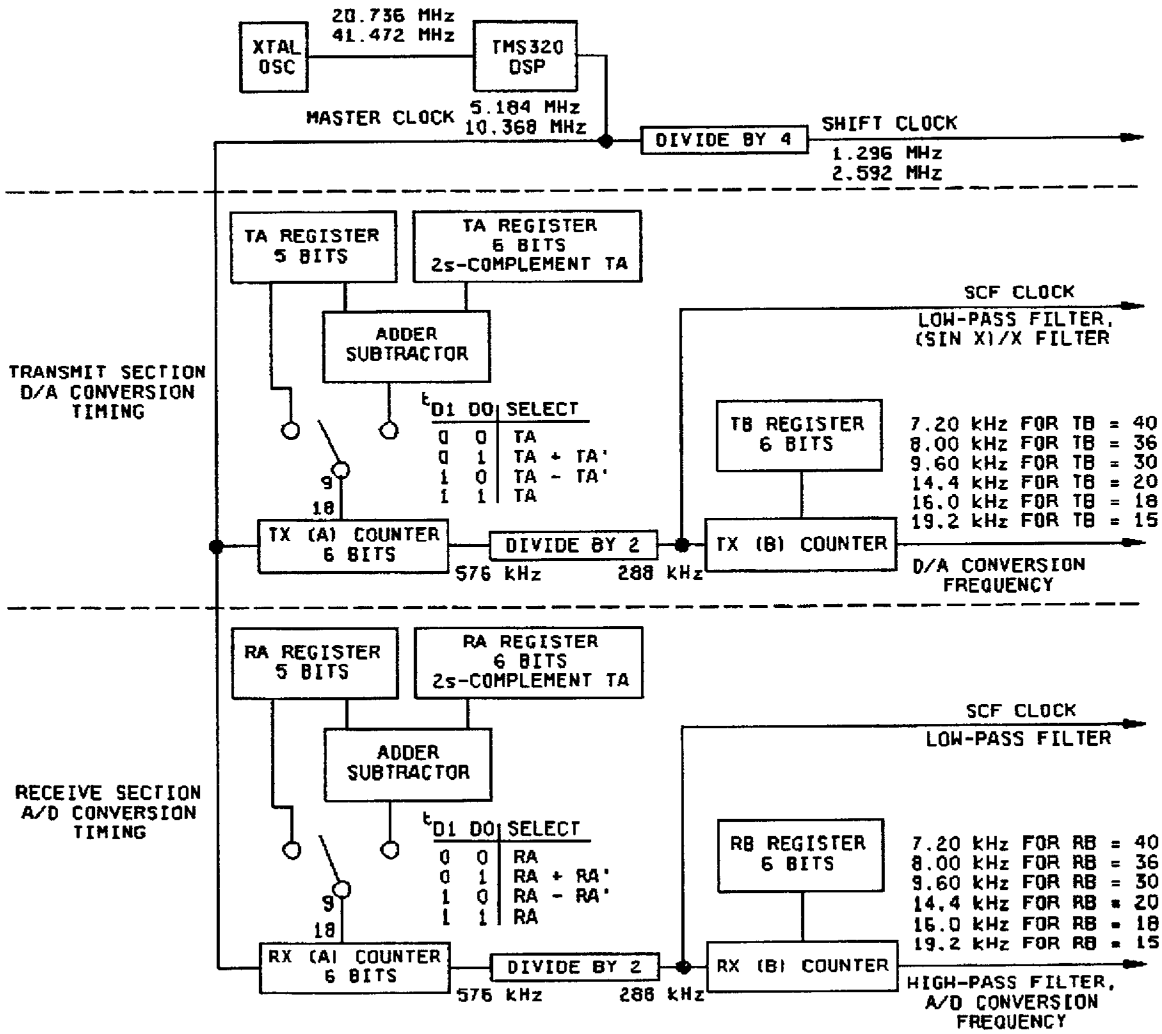


NOTES:

1. Frequency 1, 20.736 MHz, is used to show how 153.6 kHz (for a commercially available modem split band filter clock), popular speech and modem sampling signal frequencies, and an internal 288 kHz switched capacitor filter clock can be derived synchronously and as submultiples of the crystal oscillator frequency. Since these derived frequencies are synchronous submultiples of the crystal frequency, aliasing does not occur as the sampled analog signal passes between the analog converter and switched capacitor filter stages. Frequency 2, 41.472 MHz, is used to show that the AIC can work with high frequency signals, which are used by high-speed digital signal processors.
2. Split-band filtering can alternatively be performed after the analog input function via software in the TMS320.
3. These control bits are described in the AIC DX Data Word Format section.

FIGURE 3. Internal timing configuration. - Continued.

Device type 03



NOTES:

1. In synchronous operation, RA, RA',RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.
2. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP will provide a master clock frequency of 5.184 MHz the TLC32046 will produce a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 9, the SCF clock frequency will then be 288 kHz, and the D/A conversion frequency will be 288 kHz + TB.

FIGURE 3. Internal timing configuration. - Continued.

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Device type 01

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent → D15

1st bit sent of 2nd byte → D7

A/D or D/A LSB → D2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

AIC DX data word format section

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Comments
primary DX serial communication protocol																
D15 (MSB) through D2 go to the D/A converter register														0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
D15 (MSB) through D2 go to the D/A converter register														0	1	The TX and RX Counter A's are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: D1 = 0, D0-1 will cause the next D/A and A/D conversion periods to be changed by addition of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to AIC Responses to Improper Conditions.
D15 (MSB) through D2 go to the D/A converter register														1	0	The TX and RX Counter A's are loaded with the TA - TA' and RA - RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: D1 = 1, D0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to AIC Responses to Improper Conditions.
D15 (MSB) through D2 go to the D/A converter register														1	1	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

FIGURE 4. Data word format.

Device type 01

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Second Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{FSX}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, The Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, $\overline{FSR}$ will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x	to TA register	x x	to RA register	0	0	D13 and D6 are MSBs (unsigned binary)
x	to TA' register	x	to RA' register	0	1	D14 and D7 are 2's complement sign bits
x	to TB register	x	to RB register	1	0	D14 and D7 are MSB's (unsigned binary)
x x x x x x x x		D7 D6 D5 D4 D3 D2 ←---- CONTROL REGISTER ----→		1	1	D2 = 0/1 deletes/inserts the bandpass filter D3 = 0/1 disables/enables the loopback function D4 = 0/1 disables/enables the AUX IN+ and AUX IN - pins D5 = 0/1 asynchronous/synchronous transmit and receive sections D6 = 0/1 gain control bits D7 = 0/1 gain control bits

FIGURE 4. Data word format - Continued.

Device type 02

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent ↓								1st bit sent of 2nd byte ↓					A/D or D/A LSB ↓		
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

AIC DX data word format section

D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2	D1	D0	Comments
primary DX serial communication protocol			
D15 (MSB) through D2 go to the D/A converter register	0	0	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with TB and RB register values.
D15 (MSB) through D2 go to the D/A converter register	0	1	The TX and RX Counter A's are loaded with the TA + TA' and RA + RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: D1 = 0, D0 = 1 will cause the next D/A and A/D conversion periods to be changed by addition of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to AIC Responses to Improper Conditions.
D15 (MSB) through D2 go to the D/A converter register	1	0	The TX and RX Counter A's are loaded with the TA - TA' and RA - RA' register values. The TX and RX Counter B's are loaded with the TB and RB register values. NOTE: D1 = 1, D0 = 0 will cause the next D/A and A/D conversion periods to be changed by the subtraction of TA' and RA' Master Clock cycles, in which TA' and RA' can be positive or negative or zero. Please refer to AIC Responses to Improper Conditions.
D15 (MSB) through D2 go to the D/A converter register	1	1	The TX and RX Counter A's are loaded with the TA and RA register values. The TX and RX Counter B's are loaded with the TB and RB register values. After a delay of four Shift Clock cycles, a secondary transmission will immediately follow to program the AIC to operate in the desired configuration.

FIGURE 4. Data word format - Continued.

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (Primary Communications) to the AIC will initiate Second Communications upon completion of the Primary Communications.

Upon completion of the Primary Communication, $\overline{FSX}$ will remain high for four SHIFT CLOCK cycles and will then go low and initiate the Secondary Communication. The timing specifications for the Primary and Secondary Communications are identical. In this manner, The Secondary Communication, if initiated, is interleaved between successive Primary Communications. This interleaving prevents the Secondary Communication from interfering with the Primary Communications and DAC timing, thus preventing the AIC from skipping a DAC output. It is important to note that in the synchronous mode, FSR will not be asserted during Secondary Communications.

secondary DX serial communication protocol

x x	to TA register	x x	to RA register	0	0	D13 and D6 are MSBs (unsigned binary)
x	to TA' register	x	to RA' register	0	1	D14 and D7 are 2's complement sign bits
x	to TB register	x	to RB register	1	0	D14 and D7 are MSB's (unsigned binary)
x x x x x x D9 x D7 D6 D5 D4 D3 D2 (D9 to D2: CONTROL REGISTER)				1	1	D2 = 0/1 deletes/inserts the A/D high pass filter D3 = 0/1 disables/enables the loopback function D4 = 0/1 disables/enables the AUX IN+ and AUX IN- pins D5 = 0/1 asynchronous/synchronous transmit and receive sections D6 = 0/1 gain control bits D7 = 0/1 gain control bits D9 = 0/1 delete/insert on board second order (sin x)/x correction filter

FIGURE 4. Data word format - Continued.

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent ↓								1st bit sent of 2nd byte ↓					A/D or D/A LSB ↓		
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Primary DX serial communication protocol

FUNCTIONS	D1	D0
D15 (MSB) - D2 → D/A Converter Register TA → TX(A), RA → RX(A). TB → TX(B), RB → RX(B).	0	0
D15 (MSB) - D2 → D/A Converter Register TA + TA' → TX(A), RA + RA' → RX(A). TB → TX(B), RB → RX(B). The next D/A and A/D conversion period will be changed by the addition of TA' and RA' master clock cycles, in which TA' and RA' can be positive, negative, or zero.	0	1
D15 (MSB) - D2 → D/A Converter Register TA - TA' → TX(A), RA - RA' → RX(A). TB → TX(B), RB → RX(B). The next D/A and A/D conversion period will be changed by the subtraction of TA' and RA' master clock cycles, in which TA' and RA' can be positive, negative, or zero.	1	0
D15 (MSB) - D2 → D/A Converter Register TA → TX(A), RA → RX(A). TB → TX(B), RB → RX(B). After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on the DATA DR (pin 13) is routed to DR (Serial Data Output) during secondary transmission.	1	1

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, FSX remains high for four SHIFT CLOCK cycles and goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. It is important to note that FSR is not asserted due to secondary communications activity. However, in the telephone interface mode, FSD is asserted during secondary communications, but not during primary communications.

FIGURE 4. Data word format - Continued.

Device type 03

AIC DR or DX word bit pattern

A/D or D/A MSB, 1st bit sent → D15; 1st bit sent of 2nd byte → D7; A/D or D/A LSB → D2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Secondary DX serial communication protocol

FUNCTIONS	D1	D0
D13 (MSB) - D9 → TA, 5 bits unsigned binary. D6 (MSB) - D2 → RA, 5 bits unsigned binary. D15, D14, D8, and D7 are unassigned.	0	0
D14 (sign bit) - D9 → TA', 6 bits 2s complement. D7 (sign bit) - D2 → RA', 6 bits 2s complement. D15 and D8 are unassigned.	1	1
D14 (MSB) - D9 → TB, 6 bits unsigned binary. D7 (MSB) - D2 → RB, 6 bits unsigned binary. D15 and D8 are unassigned.	0	0
D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables the AUX IN+ and AUX IN- pins. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Gain Control section). D7 = 0/1 gain control bits (see Gain Control section). D9 = 0/1 delete/insert on-board second-order (sinx)/x correction filter D10 = 0/1 output to D10OUT (telephone-interface mode) D11 = 0/1 output to D11OUT (telephone-interface mode) D8, D12 - D15 are unassigned.	1	1

Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the RESET pin initializes the AIC registers to provide an 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz, and 0 Hz to 7200 Hz, respectively. Therefore, the filter bandwidths are half those shown in the filter transfer function specification section. The AIC, excepting the CONTROL register, is initialized as follows (see AIC DX Data word format section):

REGISTER	TA	TA'	TB	RA	RA'	RB
INITIALIZED VALUE (HEX)	12	01	12	12	01	12

The CONTROL register bits are reset as follows (see AIC DX Data word format section):

D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1

FIGURE 4. Data word format - Continued.

Device types 01 and 02

AIC Responses to improper conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register - TA' register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA' register + 40 HEX is loaded into TX(A) counter.
RA register + RA' register = 0 or 1 RA register - RA' register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA' register + 40 HEX is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down.
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

Gain Control Table
(Analog input signal required for full-scale A/D conversion)

INPUT CONFIGURATIONS	CONTROL REGISTER BITS D6	CONTROL REGISTER BITS D7	ANALOG 1/ INPUT	A/D CONVERSION RESULT
Differential configuration Analog input = IN+ - IN- = AUX IN+ - AUX IN-	1 0	1 0	± 6 V	± full scale
	1	0	± 3 V	± full scale
	0	1	± 1.5 V	± full scale
Single-ended configuration Analog input = IN+ - ANLG GND = AUX IN+ - ANLG GND	1 0	1 0	± 3 V	± half scale
	1	0	± 3 V	± full scale
	0	1	± 1.5 V	± full scale

1/ In this example, V_{REF} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

FIGURE 4. Data word format - Continued.

Device type 03

AIC Responses to improper conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA' register = 0 or 1 TA register - TA' register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA' register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA' register + 40 HEX is loaded into TX(A) counter.
RA register + RA' register = 0 or 1 RA register - RA' register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA' register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA' register + 40 HEX is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates.
TB register = 0 or 1	Reprogram TB register with 24 HEX
RB register = 0 or 1	Reprogram RB register with 24 HEX
AIC and DSP cannot communicate	Hold last DAC output

Gain Control Table
(Analog input signal required for full-scale Bipolar A/D conversion 2s complement) 1/

INPUT CONFIGURATIONS	CONTROL REGISTER BITS D6	D7	ANALOG 2/ 3/ INPUT	A/D CONVERSION RESULT
Differential configuration Analog input = IN+ - IN- = AUX IN+ - AUX IN-	1 0	1 0	$V_{ID} = \pm 6$ V	± full scale
	1	0	$V_{ID} = \pm 3$ V	± full scale
	0	1	$V_{ID} = \pm 1.5$ V	± full scale
Single-ended configuration Analog input = IN+ - ANLG GND = AUX IN+ - ANLG GND	1 0	1 0	$V_I = \pm 3$ V	± half scale
	1	0	$V_I = \pm 3$ V	± full scale
	0	1	$V_I = \pm 1.5$ V	± full scale

1/ $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $V_{DD} = 5$ V
2/ V_{ID} = Differential Input Voltage, V_I = Input Voltage referenced to ground with IN- or AUX IN- connected to ground.
3/ In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

FIGURE 4. Data word format - Continued.

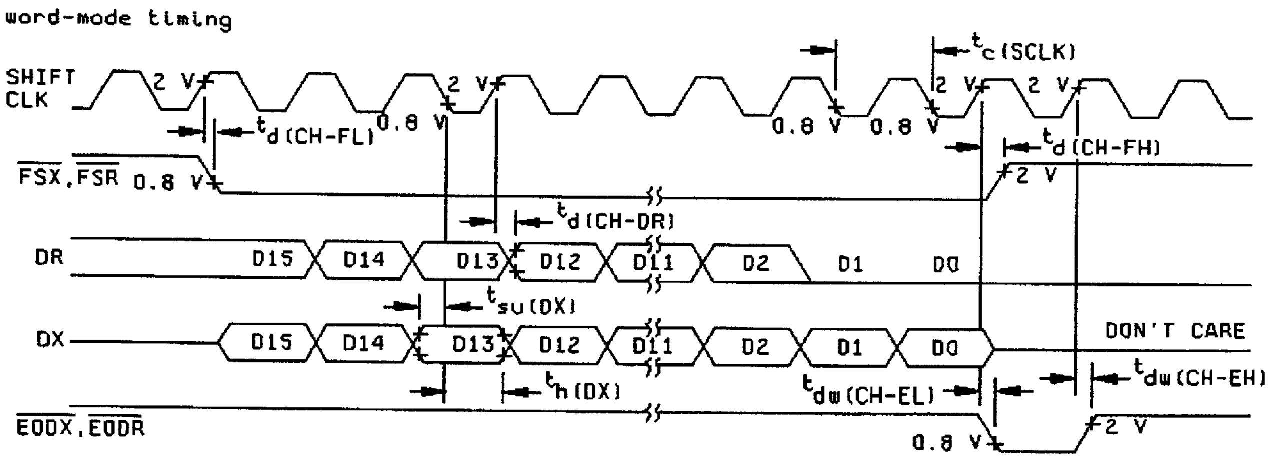


FIGURE 5. Serial port timing waveforms.

Device types 01 and 02

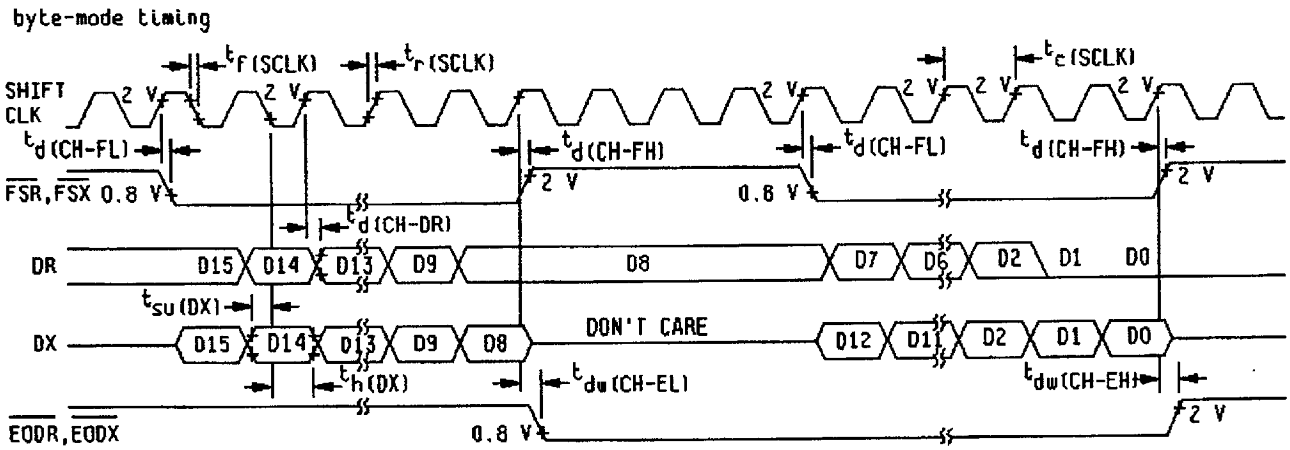
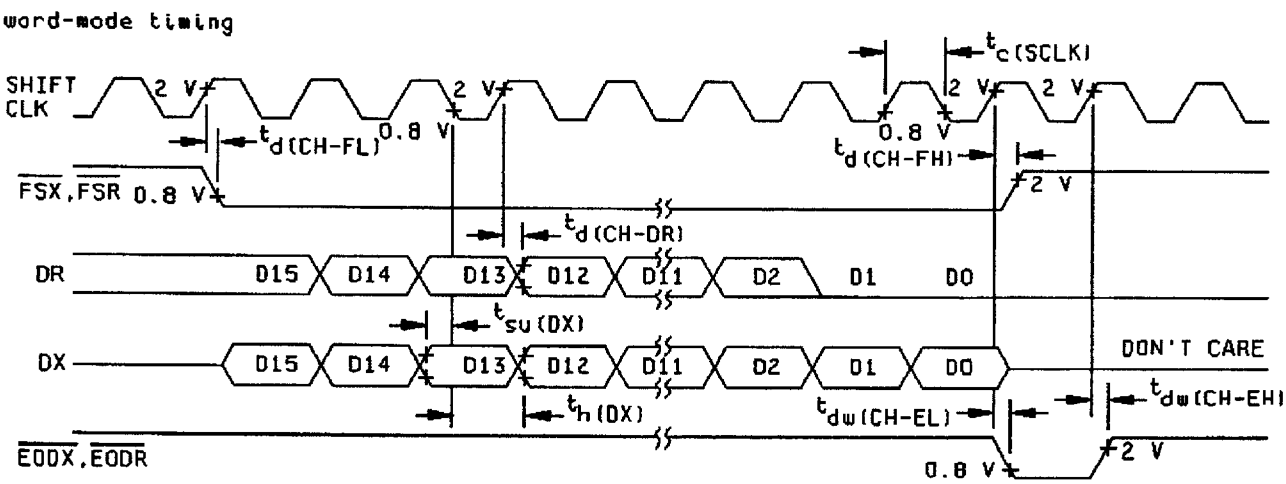


FIGURE 5. Serial port timing waveforms - Continued.

Device type 03



NOTES:

1. The time between falling edges of $\overline{FSR}$ is the A/D conversion period, and the time between falling edges of $\overline{FSX}$ is the D/A conversion period.
2. In the byte mode, when $\overline{EODX}$ or $\overline{EODR}$ is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clocks long, allowing for a four-shift-clock setup time between byte transmissions.

FIGURE 5. Serial port timing waveforms - Continued.

Device type 03

dual word-mode timing

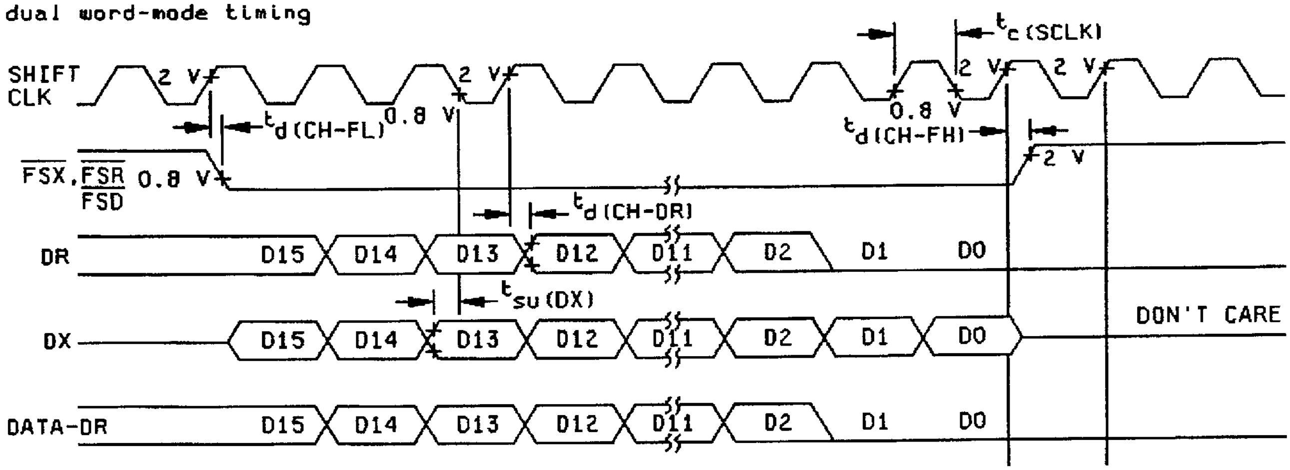


FIGURE 5. Serial port timing waveforms - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 10 and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B or D. For device class M the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883 TM 5005, table I	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1/ 1,2,3, 4,5,6,9	1/ 1,2,3, 4,5,6,9	1/ 1,2,3, 4,5,6,9
Group A test requirements (see 4.4)	1,2,3, 4,5,6, 7,8,9	1,2,3, 4,5,6, 7,8,9	1,2,3, 4,5,6, 7,8,9
Group C end-point electrical parameters (see 4.4)	1	1	1,2,3,4,5, 6,7,8,9
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	1,4,7	1,4,7	1,4,7

1/ PDA applies to subgroup 1.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A for RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA environment and level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = 25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique part numbers. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique part number. By establishing a one part number system covering all three documents, the OEM can procure to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.