REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 03 for vendor CAGE number 65786. Add a reprogrammability test to 4.3.2. Change to margin test method A. Editorial changes throughout.	93-01-12	M. A. Frye

REV																			
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REV STATUS OF SHEETS		A	A	A	A	A	A	A	A	A	A	A	A		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
89-01-26

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 16K X 8 UV EPROM, POWER DOWN, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89538
A	67268	

SHEET 1 OF 12

1

DESC FORM 193
JUL 91

5962-L381

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89538	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	CY7C254	16K x 8 UV EPROM	65 ns
02	CY7C254	16K x 8 UV EPROM	55 ns
03	CY7C254	16K x 8 UV EPROM	45 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	CQCC1-N32	32	Rectangular leadless chip carrier 1/
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line 1/
Z	GDFP2-F28	28	Flat pack 1/

1.2.3 Lead finish. The lead finish shall be as specified in MIL-M-38510. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to Outputs in high Z	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines U, X, and Z	See MIL-STD-1835
Maximum power dissipation (P_D) 2/	1.0 W
Maximum junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds maximum)	+260°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C inspection (see 4.3), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern or equivalent (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPROMs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure or programmed EPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA $V_{IN} = V_{IH}$ or V_{IL}	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16.0 mA $V_{IN} = V_{IH}$ or V_{IL}	1, 2, 3	All		0.5	V
Input high voltage 1/	V_{IH}		1, 2, 3	All	2.0		V
Input low voltage 1/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{OUT} = 5.5 V and GND	1, 2, 3	All	-40	40	µA
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.0 V	1, 2, 3	All	-20	-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA Inputs cycling from 0 V to 3 V, f = 16.7 MHz	1, 2, 3	All		120	mA
Input capacitance 3/	C_{IN}	V_{IN} = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		10	pF
Output capacitance 3/	C_{OUT}	V_O = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		10	pF
Address to output valid 4/	t_{AA}	V_{CC} = 4.5 V See figures 3 and 4	9, 10, 11	01		65	ns
				02		55	
				03		45	
Chip select active to output valid 4/ 5/	t_{ACS}		9, 10, 11	01		35	ns
				02		30	
				03		25	

See footnotes at end of table.

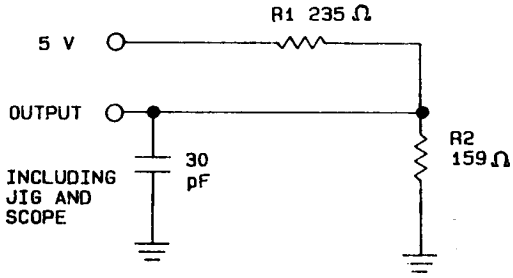
Device types	01 - 03	
Case outlines	X, Z	U
Terminal number	Terminal symbol	
1	A_9	A_9
2	A_8	A_8
3	A_7	A_7
4	A_6	A_6
5	A_5	A_5
6	A_4	A_4
7	A_3	A_3
8	A_2	A_2
9	A_1	A_1
10	A_0	A_0
11	O_0	NC
12	O_1	O_0
13	O_2	O_1
14	GND	O_2
15	O_3	NC
16	O_4	GND
17	O_5	O_3
18	O_6	NC
19	O_7	O_4
20	$\overline{CS}_4$	O_5
21	CS_3	O_6
22	$\overline{CS}_2$	O_7
23	$\overline{CS}_1$	NC
24	A_{13}	$\overline{CS}_4$
25	A_{12}	CS_3
26	A_{11}	$\overline{CS}_2$
27	A_{10}	$\overline{CS}_1$
28	V_{CC}	A_{13}
29	---	A_{12}
30	---	A_{11}
31	---	A_{10}
32	---	V_{CC}

FIGURE 1. Terminal connections.

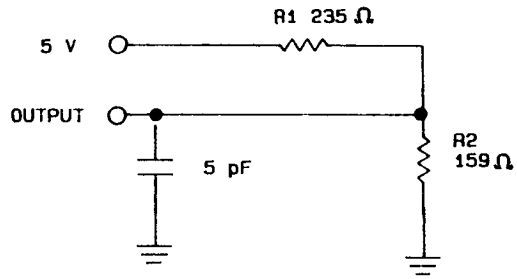
Mode	$\overline{CS}_4$	CS_3	$\overline{CS}_2$	$\overline{CS}_1$	A_{13}-A_0	Power	Outputs
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	X	I_{CC}	Data out
Output disable	X	X	X	V_{IH}	X	I_{CC}	High-Z
Output disable	X	X	V_{IH}	X	X	I_{CC}	High-Z
Output disable	X	V_{IL}	X	X	X	I_{CC}	High-Z
Output disable	V_{IH}	X	X	X	X	I_{CC}	High-Z
Program	XP	V_{IHP}	V_{PP}	V_{ILP}	XP	I_{CC}	Data in
Program verify	XP	V_{ILP}	V_{PP}	V_{IHP}	XP	I_{CC}	Data out
Program inhibit	XP	V_{IHP}	V_{PP}	V_{IHP}	XP	I_{CC}	High-Z
Blank check	XP	V_{ILP}	V_{PP}	V_{IHP}	XP	I_{CC}	Data out

NOTE:
1. X = Don't care.
2. High-Z = High impedance state.
3. V_{PP} = 12.5 V ±0.5 V; V_{ILP} = 0.4 V maximum; V_{IHP} = 3.0 V minimum.
4. XP = 0.4 V maximum or 3.0 V minimum to 5.25 V maximum.

FIGURE 2. Truth table.



CIRCUIT A



CIRCUIT B

FIGURE 3. Output load circuits.

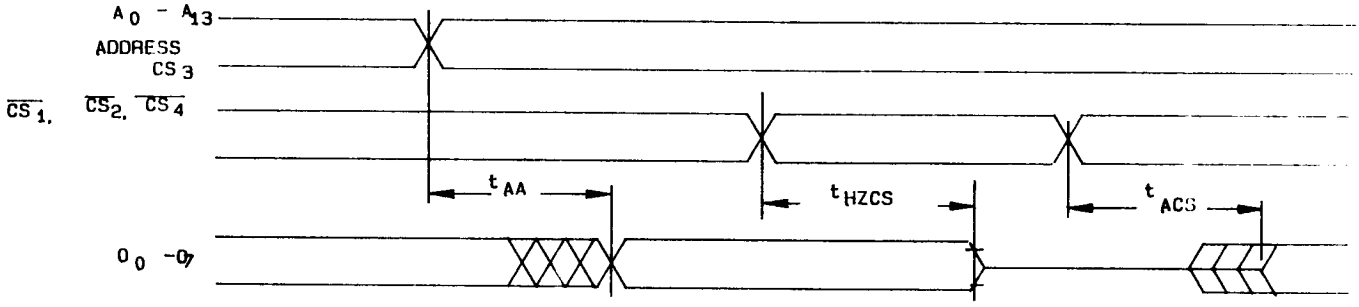


FIGURE 4. Switching waveform.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A. 1/

(1) Program at +25°C greater than 95 percent of the bit locations.

(2) Bake, unbiased, for 72 hours at +140°C or 32 hours at +150°C or 8 hours at +200°C or 4 hours at +300°C for unassembled devices only.

(3) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Erase (see 3.10.1).

(5) Program at +25°C with a 50 percent pattern (example: checkerboard or equivalent).

(6) Perform margin test using V_m = +5.75 V and V_m = +4.40 V at +25°C with loose timing.

(7) Perform dynamic burn-in in accordance with 4.2a herein.

(8) Perform margin test using V_m = +5.55 V and V_m = +4.40 V at +25°C using loose timing.

(9) Perform electrical tests (see 4.2b).

(10) Erase (see 3.10.1), except devices submitted for groups A, B, C, and D testing.

(11) Verify erasure (see 3.10.3). The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table and the EPROM pattern specified in 4.3.1e.

e. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.

1/ Steps 1 through 4 may be performed at the wafer level.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices submitted for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for group D testing).

c. A reprogammability test shall be completed as part of the vendors reliability monitors, this reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. This test shall consist of 25 program/erase cycles on 25 devices with the following conditions:

(1) All devices selected for testing shall be programmed per 3.2.3.1 herein.

(2) Verify pattern (see 3.10.3).

(3) Erase (see 3.10.1).

(4) Verify pattern erasure (see 3.10.3).

TABLE II. Electrical test requirements. 1/ 2/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8,9
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

1/ Any or all subgroups may be combined when using high-speed testers.
2/ Subgroups 7 and 8A, and 8B functional tests shall also verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
* Indicates PDA applies to subgroups 1 and 7.
** See 4.3.1c.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating.
The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Electrostatic discharge sensitivity (ESDS). Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.