REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add F-6 package. Editorial changes throughout.	91-04-23	M. A. Frye

REV																									
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A						A	A	A								
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15									

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 27 JULY 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS 256 x 4 SRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88594

SHEET 1 OF 15

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911
5962-E1462

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-88594	01	W	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(See 6.6)	256 X 4 CMOS static RAM	15 ns
02	(See 6.6)	256 X 4 CMOS static RAM	35 ns
03	(See 6.6)	256 X 4 CMOS static RAM	25 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package
W	D-7 (22-lead, 1.111" x .410" x .225"), dual-in-line package
X	C-3 (24-terminal, .410" x .410" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage to ground potential	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs	-0.5 V dc to V_{CC} +0.5 V dc
DC input voltage	-0.5 V dc to V_{CC} +0.5 V dc
Output current into outputs (low)	20 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	495 mW 1/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases W, X, and K	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C
Latchup current	>200 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Minimum high level input voltage (V_{IH})	2.1 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -5.2 mA, V_{IL} = 0.8 V, V_{IH} = 2.1 V	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.1 V	1,2,3	All		0.4	V
Input load current	I_I	$0\ V \le V_{IN} \le 5.5\ V$	1,2,3	All	-10	10	µA
Output current, high impedance	I_{OZ}	$V_{OL} \le V_{OUT} \le V_{OH}$, output disabled	1,2,3	All	-10	10	µA
Output short circuit current 1/ 2/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0 V	1,2,3	All		-90	mA
Power supply current	I_{CC}	Addresses cycling between V_{SS} and 3.0 V, f = $1/t_{AVAV}$(minimum), V_{CC} = 5.5 V, $\overline{CE}_1$ = 0.8 V, CE_2 = 2.1 V, outputs open, $\overline{WE}$ = 2.1 V, $\overline{OE}$ = 0.8 V	1,2,3	All		90	mA
Input capacitance	C_{IN}	V_{CC} = 5.0 V, f = 1.0 MHz, T_A = +25°C, see 4.3.1c	4	All		4.0	pF
Output capacitance	C_{OUT}		4	All		7.0	pF
Read cycle time	t_{AVAV}	See figures 3 and 4 3/	9,10,11	01	15		ns
				02	35		ns
				03	25		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip select time	t_{ELQV}	See figures 3 and 4 3/	9,10,11	01		8.0	ns
				02		25	ns
				03		15	ns
Chip select to high impedance	t_{E1HQZ}	See figures 3 and 4 2/ 4/	9,10,11	01		12	ns
				02		30	ns
				03		20	ns
Output enable time	t_{OLQV}	See figures 3 and 4 3/	9,10,11	01		8.0	ns
				02		25	ns
				03		15	ns
Output enable to high impedance	t_{OHQZ}	See figures 3 and 4 2/ 4/	9,10,11	01		12	ns
				02		30	ns
				03		20	ns
Address access time	t_{AVQV}	See figures 3 and 4 3/	9,10,11	01		15	ns
				02		35	ns
				03		25	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle time	t_{AVAV}	See figures 3 and 5 3/	9,10,11	01	15		ns
				02	35		ns
				03	25		ns
Write enable to high impedance	t_{WLQZ}	See figures 3 and 5 2/ 4/	9,10,11	01		12	ns
				02		30	ns
				03		20	ns
Write recovery time	t_{WHQV}	See figures 3 and 5 3/	9,10,11	01		12	ns
				02		25	ns
				03		20	ns
Write pulse width	t_{WLWH}	See figures 3 and 5 3/ 5/	9,10,11	01	11		ns
				02	25		ns
				03	15		ns
Data setup time prior to write	t_{DXWL}	See figures 3 and 5 3/	9,10,11	01	0		ns
				02, 03	5.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data hold time after write	t_{WHDX}	See figures 3 and 5 3/	9,10,11	01	2.0		ns
				02, 03	5.0		ns
Address setup time	t_{AVWL}	See figures 3 and 5 3/ 5/	9,10,11	01	0		ns
				02	10		ns
				03	5.0		ns
Address hold time	t_{WHAX}	See figures 3 and 5 3/	9,10,11	01	4.0		ns
				02, 03	5.0		ns
Chip select setup time	t_{E1LWL} t_{E2HWL}	See figures 3 and 5 3/	9,10,11	01	0		ns
				02, 03	5.0		ns
Chip select hold time	t_{WHE2L}	See figures 3 and 5 3/	9,10,11	01	2.0		ns
				02, 03	5.0		ns

1/ Not more than one output should be shorted at a time, and duration of short circuit shall not exceed 30 seconds.

2/ May not be tested, but shall be guranteed to the limits specified in table I.

3/ Test conditions assume signal transition times of 3.0 ns or less for device type 01 and 5.0 ns or less for device types 02 and 03. Timing is referenced at input and output levels of 1.5 V. Output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 30 pF.

4/ Test conditions assume signal transition times of 3.0 ns or less for device type 01 and 5.0 ns or less for device types 02 and 03. Transition is measured at steady-state high level of -500 mV or steady-state low level of +500 mV on the output from 1.5 V level on the input with a load capacitance of 5.0 pF.

5/ t_{WLWH} is measured at t_{AVWL} = minimum. t_{AVWL} is measured at t_{WLWH} = minimum.

Pin name			
Device	All	All	02, 03
Package	W	X	K
Pin number			
1	A_2	A_3	A_3
2	A_1	A_2	A_2
3		A_1	A_1
4		A_0	A_0
5	A_5	A_5	A_5
6	A_6	NC	A_6
7	A_7	A_6	A_7
8	GND	A_7	Y_{SS}
9	D_0	GND	D_0
10	O_0	D_0	O_0
11	D_1	O_0	D_1
12	O_1	D_1	NC
13	D_2	O_1	NC
14	O_2	D_2	O_1
15	D_3	O_2	D_2
16	O_3	D_3	O_2
17	CE_2	O_3	D_3
18	$\overline{OE}$	NC	O_3
19	$\overline{CE_1}$	CE_2	CS_2
20	$\overline{WE}$	$\overline{OE}$	$\overline{OE}$
21	A_4	$\overline{CE_1}$	$\overline{CS_1}$
22	V_{CC}	$\overline{WE}$	$\overline{WE}$
23	---	A_4	A_4
24	---	V_{CC}	V_{CC}

FIGURE 1. Terminal connections.

Device types 01 through 03

Input					Output	Mode
CE_2	$\overline{CE}_1$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	
L	X	X	X	X	High Z	Not selected
X	H	X	X	X	High Z	Not selected
H	L	X	H	X	High Z	Output disabled
H	L	H	L	X	Selected data	Read data
H	L	L	X	L	High Z	Write "0"
H	L	L	X	H	High Z	Write "1"

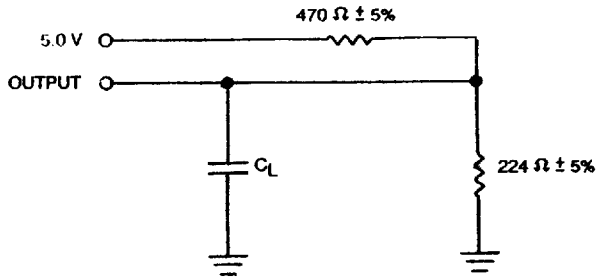
H = Logic 1 state

L = Logic 0 state

X = Don't care

HIGH Z - High impedance state

FIGURE 2. Truth table.



Measurement	C_L (including scope and jig capacitance, minimum
t_{E1HQZ}, t_{OHQZ}, and t_{WLQZ}	C_L = 5.0 pF
All others	C_L = 30 pF

FIGURE 3. Output load circuit.

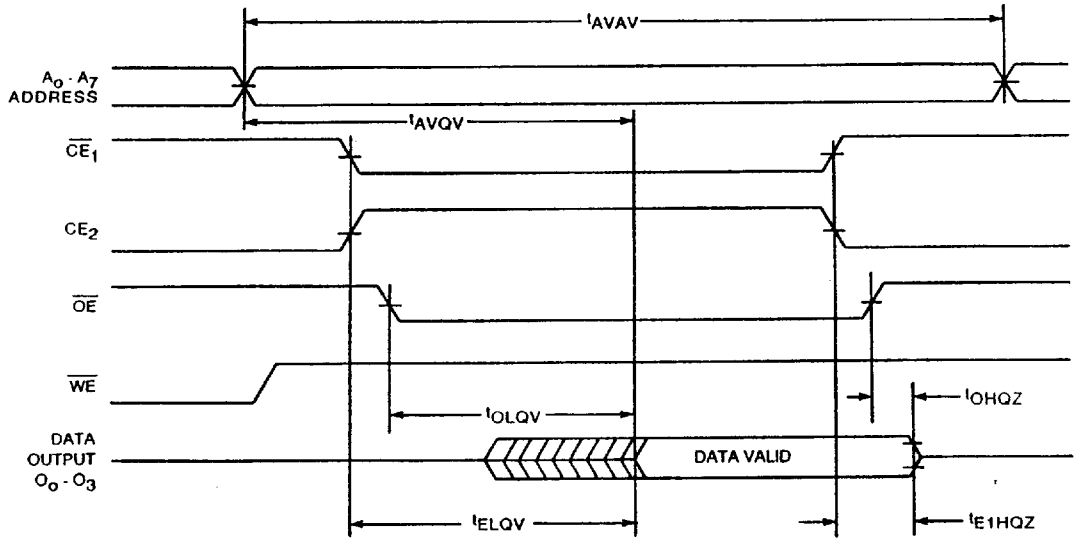


FIGURE 4. Read cycle timing diagram.

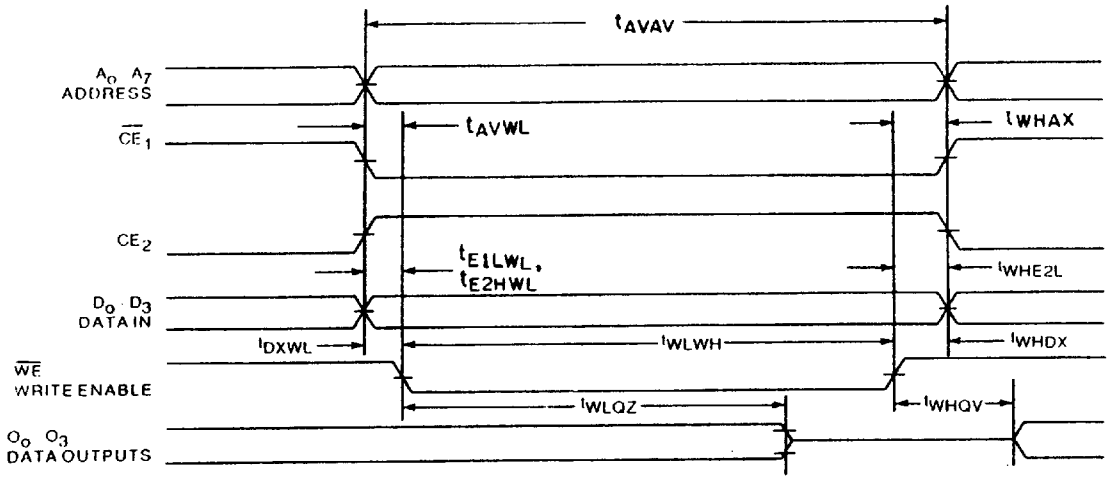


FIGURE 5. Write cycle timing diagram.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*,2,3,7*, 8,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8

* PDA applies to subgroup 1 and 7.
** See 4.3.1c

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.