

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

## TC74HC564AP, TC74HC564AF TC74HC574AP, TC74HC574AF, TC74HC574AFW

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT  
 TC74HC564AP/AF INVERTING  
 TC74HC574AP/AF/AFW NON-INVERTING

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74HC564A and HC574A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ).

The TC74HC564A has inverting outputs, and the TC74HC574A has non-inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

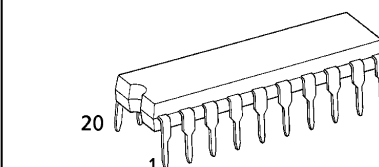
### FEATURES:

- High Speed.....  $f_{MAX} = 62\text{MHz}(\text{typ.})$   
at  $V_{CC} = 5\text{V}$
- Low Power Dissipation.....  $I_{CC} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity.....  $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability..... 15 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 6\text{mA}(\text{Min.})$
- Balanced Propagation Delays.....  $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range...  $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS564/574

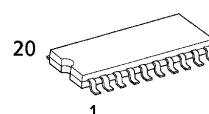
### TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(574A)	$\overline{Q}$ (564A)
H	X	X	Z	Z
L		X	$Q_n$	$\overline{Q}_n$
L		L	L	H
L		H	H	L

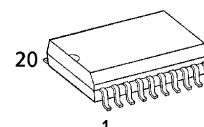
X : Don't Care  
 Z : High Impedance  
 $Q_n$  ( $\overline{Q}_n$ ) : No Change



P (DIP20-P-300-2.54A)  
 Weight : 1.30g (Typ.)

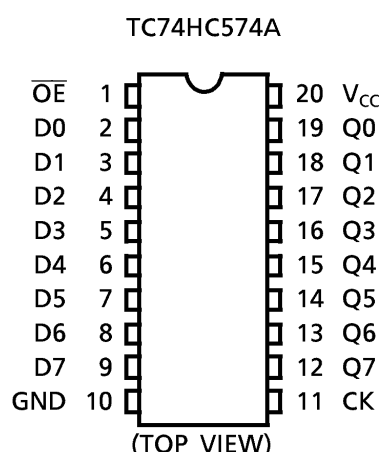
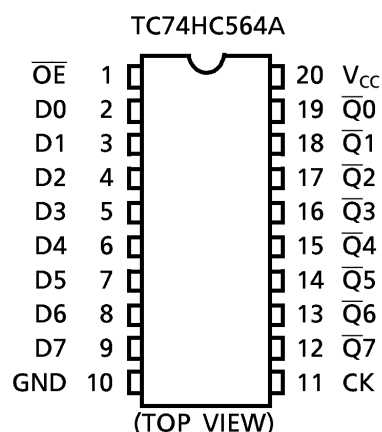


F (SOP20-P-300-1.27)  
 Weight : 0.22g (Typ.)



FW (SOL20-P-300-1.27)  
 Weight : 0.46g (Typ.)

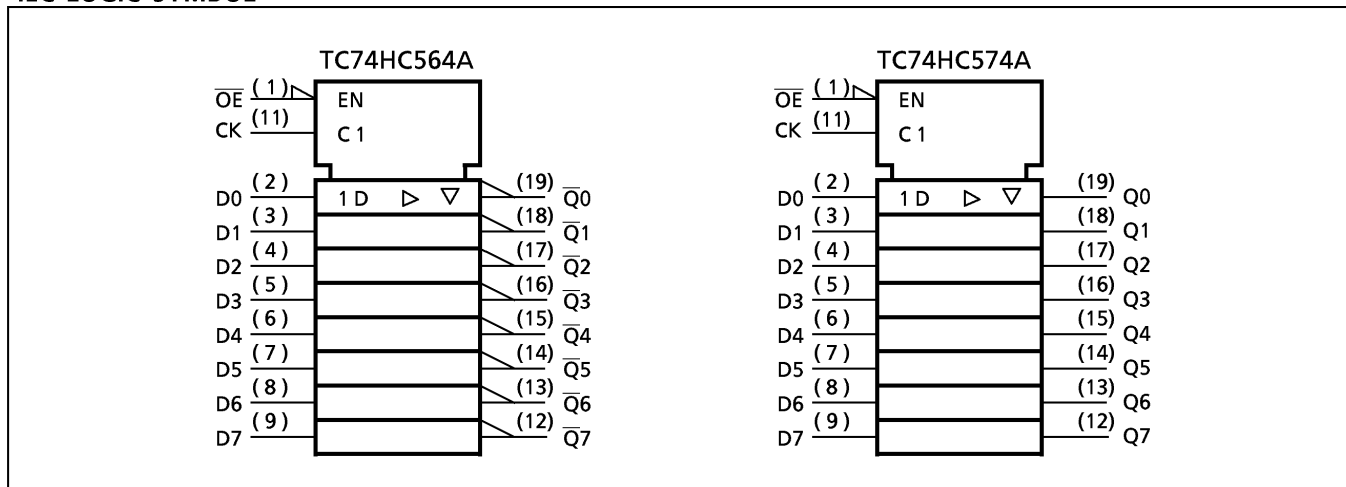
### PIN ASSIGNMENT



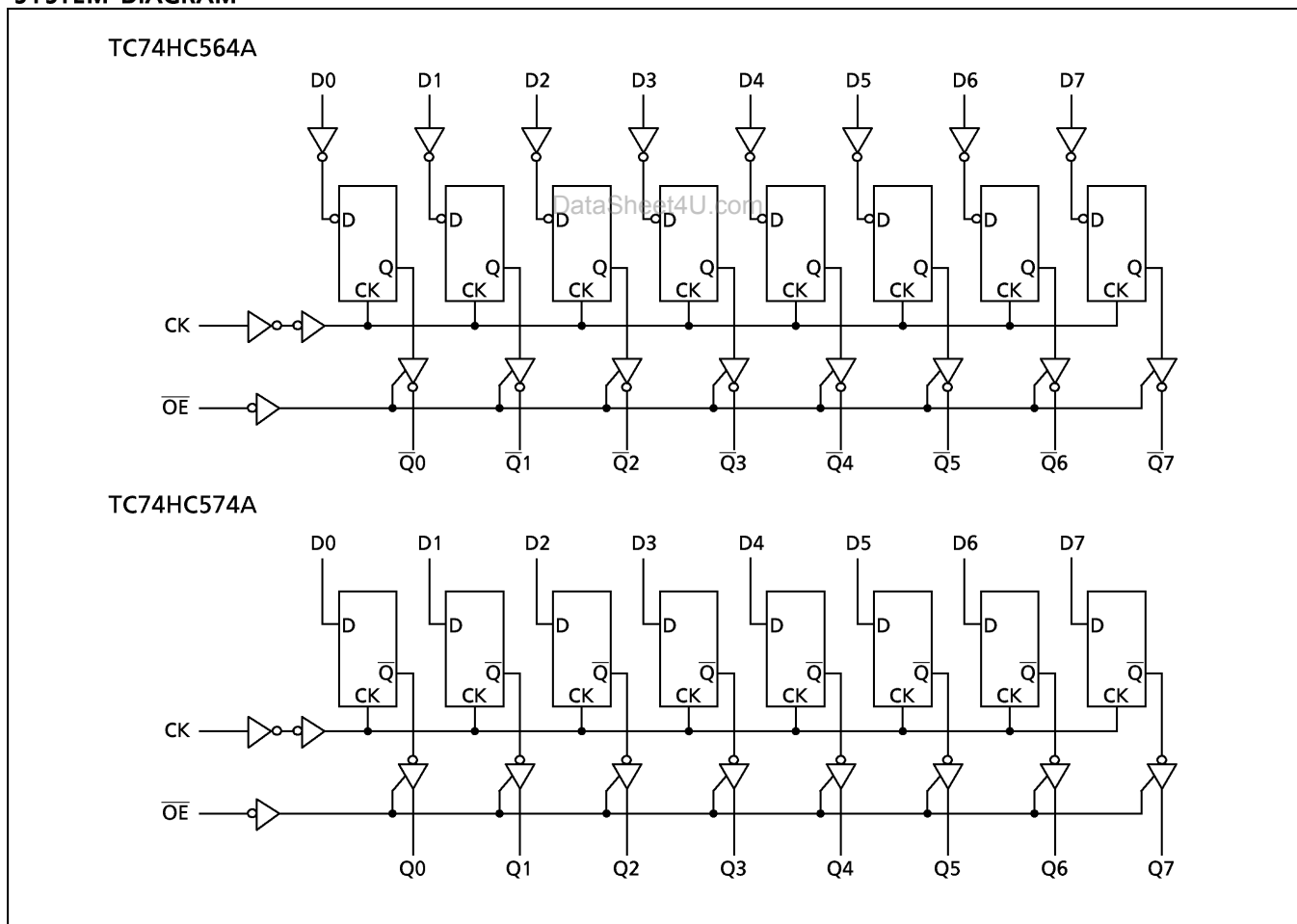
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## IEC LOGIC SYMBOL



## SYSTEM DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 35$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 75$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V	
Low - Level Input Voltage	$V_{IL}$		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	— — —	V
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
				$I_{OH} = -6\text{ mA}$ $I_{OH} = -7.8\text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
				$I_{OL} = 6\text{ mA}$ $I_{OL} = 7.8\text{ mA}$	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	
3 - State Output Off - State Current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	6.0	—	—	$\pm 0.5$	—	$\pm 5.0$	$\mu\text{A}$	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$		
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0		

TIMING REQUIREMENTS (Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (Dn)	$t_s$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time (Dn)	$t_h$		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	31	24	
			6.0	—	36	28	

AC ELECTRICAL CHARACTERISTICS (Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	$V_{CC}$ (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$ $t_{THL}$		50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Propagation Delay Time (CK-Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$		50	2.0	—	70	150	—	190	
				4.5	—	20	30	—	38	
				6.0	—	15	26	—	33	
				150	2.0	—	88	190	—	240
					4.5	—	25	38	—	48
					6.0	—	19	33	—	41
Output Enable time	$t_{pZL}$ $t_{pZH}$	$R_L = 1\text{k}\Omega$	50	2.0	—	48	125	—	155	
				4.5	—	15	25	—	31	
				6.0	—	12	21	—	26	
				150	2.0	—	60	165	—	205
					4.5	—	20	33	—	41
					6.0	—	16	28	—	35
Output Disable time	$t_{pLZ}$ $t_{pHZ}$	$R_L = 1\text{k}\Omega$	50	2.0	—	34	125	—	155	
				4.5	—	17	25	—	31	
				6.0	—	15	21	—	26	
Maximum Clock Frequency	$f_{MAX}$		50	2.0	6	17	—	5	—	MHz
				4.5	31	50	—	24	—	
				6.0	36	59	—	28	—	
Input Capacitance	$C_{IN}$				—	5	10	—	pF	
Output Capacitance	$C_{OUT}$				—	10	—	—		
Power Dissipation Capacitance	$C_{PD}$ (1)				—	54	—	—		

Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

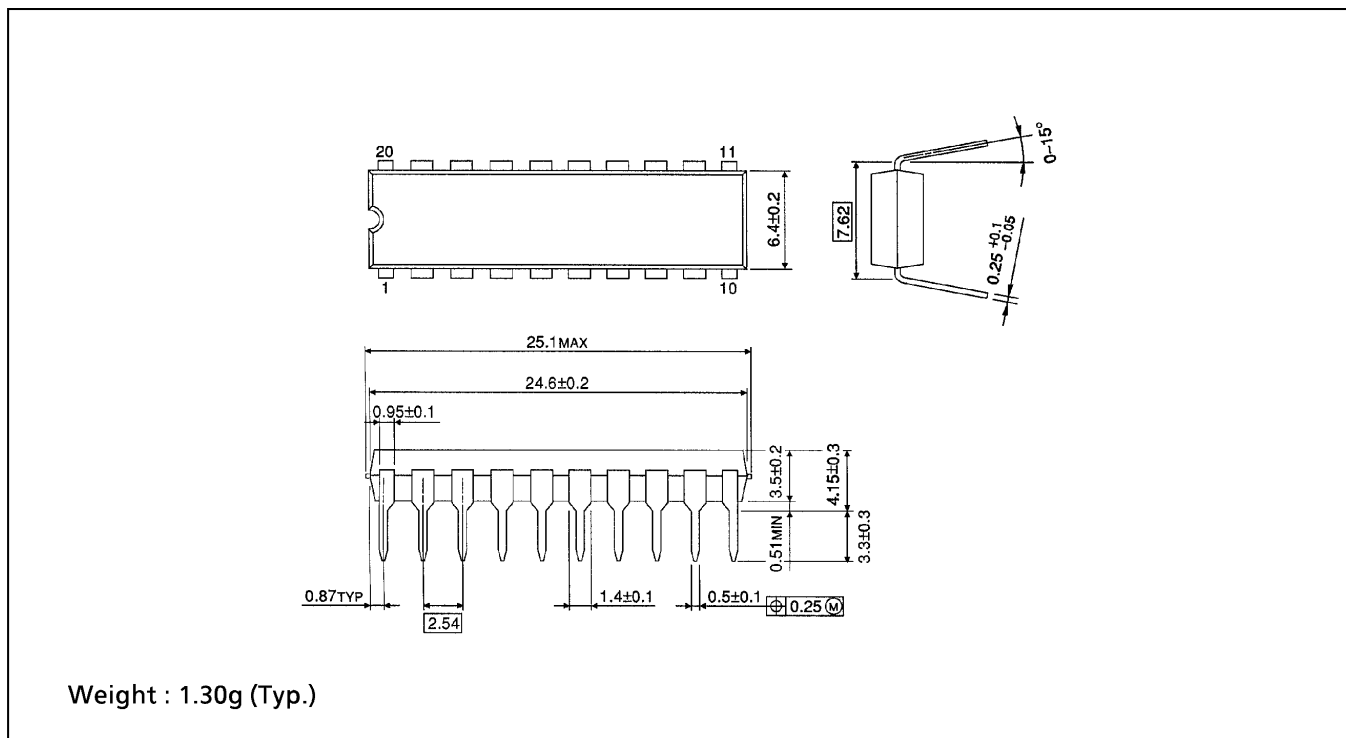
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

And the total  $C_{PD}$  when n pcs. of Flip Flop operate can be gained by the following equation:

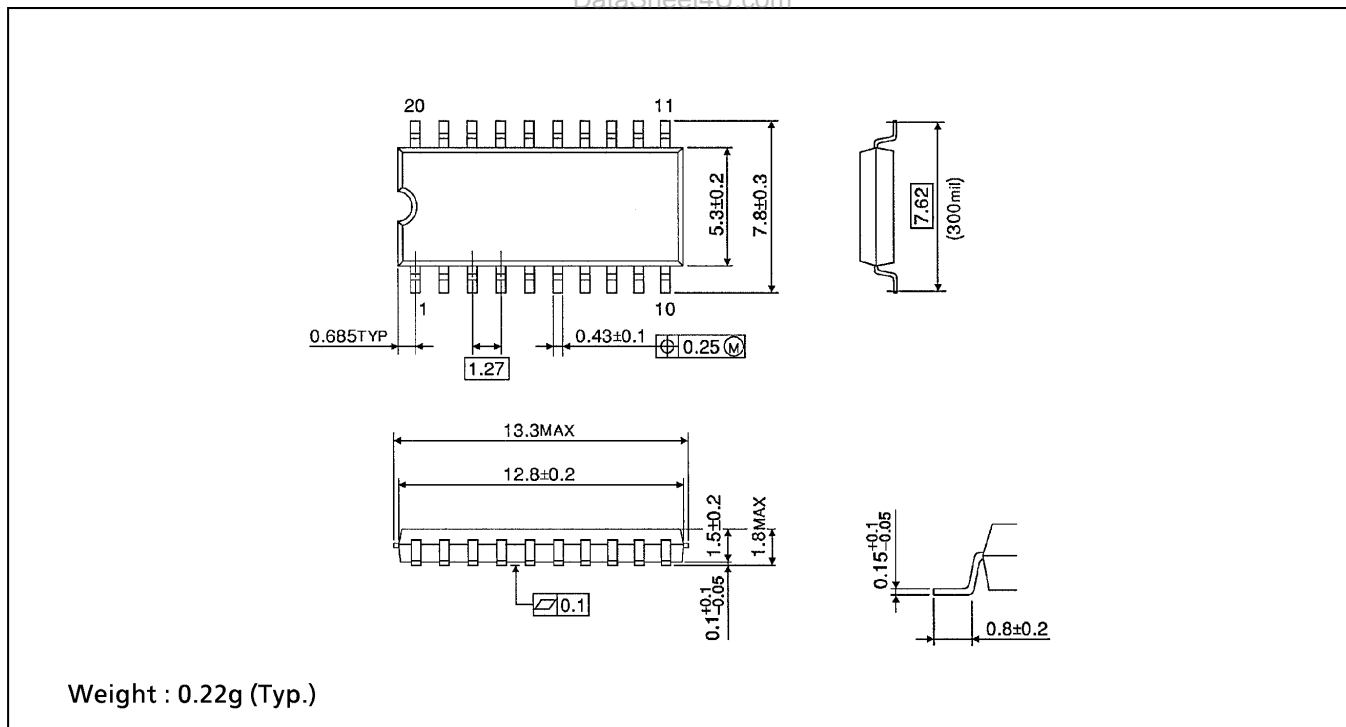
$$C_{PD}(\text{total}) = 39 + 15 \cdot n$$

**DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)**

Unit in mm

**SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)**

Unit in mm



**SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)**

Unit in mm

(Note) This package is not available in Japan.

