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## DESCRIPTION

The (Spindle) Motor Commutator in conjunction with a companion microcontroller, provides starting, accelerating, precise rotational speed regulation functions, coasting (for retract), and dynamic brake. The circuit can be used with 4-, 8-, or 12-pole, 3 phase, brushless DC motors without the need for Hall sensors.

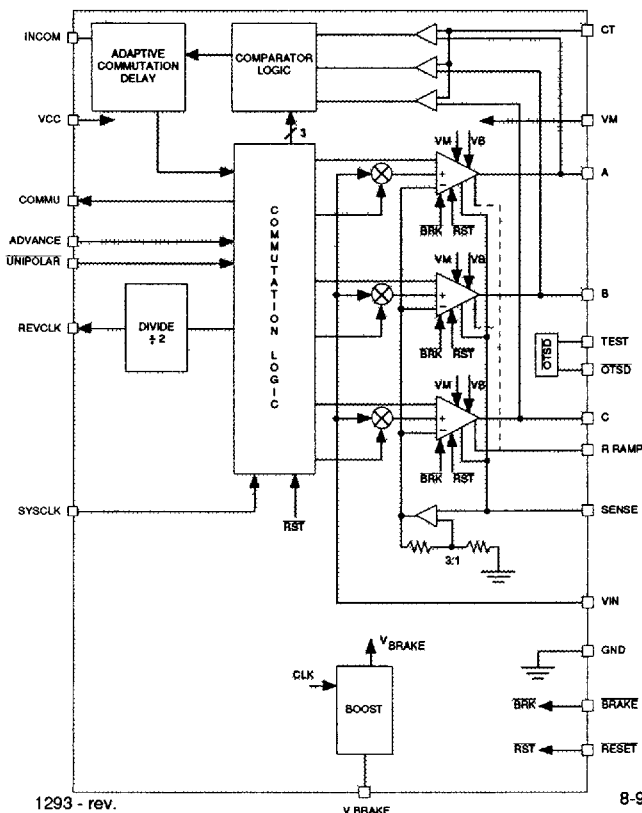
The commutator determines motor armature position by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (CT) and initiates commutation when the appropriate comparison is made.

Because the back-emf comparison event occurs prior

(continued)

## FEATURES

- Optimum commutation without external components
- Retract coast and brake modes supported
- 1 $\Omega$  FET drivers
- Commutation without Hall sensors
- Reduced DV/DT on commutation - no snubber networks required
- No blocking diode required
- Immune to brown outs and load transients



## BLOCK DIAGRAM

INCOM	1	36	ADVANCE
UNIPOLAR	2	35	REVCLK
N/C	3	34	N/C
RESET	4	33	N/C
BRAKE	5	32	N/C
VIN	6	31	SYSCLK
GND	7	30	R RAMP
VM1	8	29	VCC
SENSE1	9	28	SENSE4
VM2	10	27	VM10
VM3	11	26	VM9
C	12	25	A
VM4	13	24	VM8
VM5	14	23	VM7
SENSE2	15	22	CT
V BRAKE	16	21	TEST
OTSD	17	20	SENSE3
VM6	18	19	B

36-Pin SOM

## PIN DIAGRAM

CAUTION: Use handling procedures necessary for a static sensitive component.

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## Hall-Sensorless

### Motor Speed Commutator

#### DESCRIPTION (Continued)

to the time when optimum commutation should occur, commutation is delayed by a predetermined time after the comparison. The commutation delay is provided by a circuit which measures the interval between prior comparison events and delays commutation by a time equal to 0.43 of the prior interval. (The delay is set at 0.43 not 0.50 in order to compensate for commutation delays and motor current build-up time.) The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds. Since the commutation of motor current typically causes transients, the circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 0.71 of the interval (between events) after the comparison event. The commutation delay can be externally modified by  $\pm 15\%$  with the INCOM pin. The commutation states are shown in Table 1.

Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a

gain stage ( $A_v=4$ ) and fed to the inverting input of the transconductance output stage. Input voltage VIN must be generated from external means that use either REVCLK or other external rotational index indicators to measure rotational speed.

Four operating conditions are selected via  $\overline{\text{BRAKE}}$  and  $\overline{\text{RESET}}$ . With  $\overline{\text{BRAKE}}$  and  $\overline{\text{RESET}}$  asserted (low), outputs A, B, and C are low impedance to ground, (without current limiting function) and analog circuits are de-biased. This is the "sleep" condition. It also provides dynamic braking to the motor. With  $\overline{\text{BRAKE}}$  asserted, and  $\overline{\text{RESET}}$  de-asserted, drivers are low impedance to ground (without current limit function) and the analog circuitry is biased. For  $\overline{\text{RESET}}$  asserted,  $\overline{\text{BRAKE}}$  de-asserted, the output drivers are in a high impedance state. This will allow the user to take energy from the back-emf of a spinning motor for retracting heads. Normal operation is given for  $\overline{\text{BRAKE}}$  and  $\overline{\text{RESET}}$  de-asserted.

Note that circuit utilizes NMOS driver transistors and does not require a Schottky blocking diode to prevent current flow from the spinning motor to the power supply. During RETRACT conditions, the motor is isolated from VM.

TABLE 1: Output Driver States

STATE	COMMU	PULL DOWNS			PULL UP		
		A	B	C	UPA	UPB	UPC
0, (Reset State)	1	off	on, (off)	off	on	off	off
1	0	off	off	on	on	off	off
2	1	off	off	on	off	on	off
3	0	on	off	off	off	on	off
4	1	on	off	off	off	off	on
5	0	off	on	off	off	off	on

TABLE 2: Rout Low to SENSE

$\overline{\text{BRAKE}}$	$\overline{\text{RESET}}$	CONDITION	ANALOG	COUNTERS	A, B, C
0	0	SLEEP/BRAKE	OFF	RESET	Rout low to SENSE
0	1	BRAKE	ON	ACTIVE	Rout low to SENSE
1	0	RETRACT	ON	ACTIVE	FLOAT
1	1	RUN	ON	ACTIVE	ACTIVE

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE,  $\overline{\text{RESET}}$  and COMMU. The microprocessor can assert  $\overline{\text{RESET}}$  to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

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#### PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
RESET	I	Refer to Table 2.
BRAKE	I	BRAKE is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to RESET are selected such that $1.2 \cdot R \cdot C$ is equal to the maximum time required for retract.
SYSCLK	I	2.0 MHz clock input signal.
COMMU	O	COMMU is the LSB of the commutation counter.
REVCLK	O	Indicates 1 revolution of 4-pole motor, 1/2 revolution of 8-pole, and 1/3 revolution of 12-pole motor.
ADVANCE	I	ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal commutation due to back-emf events.
VM 1 - 10	Power	Motor Power Supply.
INCOM	I	Adaptive commutator delay trim. Generally a no-connect.
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the sense amplifier, transconductance ( $G_m$ ) will be $G_m = I_m/VIN = 1/(R_s \cdot 4)$ . The voltage at VIN must be controlled by external circuitry to accomplish speed control.
SENSE1 SENSE2 SENSE3 SENSE4	Power	Current monitoring sense amplifier (high side) input pin. The lower driver transistor current (hence motor current) is sent through a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 4 in the sense amplifier) to match VIN.
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.
CT	I	Back-EMF input from motor coil center tap. Input connected to the center tap for sensing generated back-emf voltages. The circuit uses the back-emf voltages to determine rotor position and effect commutation. 3 equal value resistors from A, B, and C attached to CT will suffice to synthesize a center-tap potential on three terminal motors. 4 terminal motors should use this terminal.
VCC	Power	5-volt power pin.

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### Motor Speed Commutator

#### PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
V BRAKE	O	External capacitor to store charge for driver circuitry. The stored charge is used by the lower drivers in fault conditions to achieve dynamic braking.
GND	-	Ground connection. GND is the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential.
OTSD	O	Indicates over temperature condition and forces drivers off. Operation after cool down is restored by asserting ADVANCE.
R RAMP	I	External resistor. Sets DV/DT for lower driver turn-off. DV/DT is approximately $25 \cdot \frac{10^9}{RRAMP}$ (Volts / Second)
UNIPOLAR	I	Select line for Unipolar or Bipolar mode. UNIPOLAR = low will de-activate upper drivers. Note: for BRAKE and SLEEP modes user must guarantee that external Unipolar driver transistor(s) do not conflict with lower driver transistors on circuit.
TEST	I/O	No connect, leave open circuited.

#### ELECTRICAL SPECIFICATIONS

##### ABSOLUTE MAXIMUM RATINGS

(Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability.)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VCC	-0.3	7	V
	VM	-0.3	7	V
Digital Inputs/Outputs	SYSCLK, ADVANCE COMMU, REVCLK	-0.3	VCC +0.3	V
Analog I/O	VIN, RRAMP, INCOM, TEST	-0.3	VCC +0.3	V
Motor Interface Voltage	CT, A, B, C, BRAKE, SENSE, RESET	-0.3	20	V
Motor Interface Current	A, B, C, VM, SENSE	-1.0	+1.0	A
Storage Temperature, Tstg		-65	150	°C
Lead Temperature, Tlead		-	300	°C

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#### ELECTRICAL SPECIFICATIONS

##### RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VCC		4.75		5.25	V
	VM		4.75		5.25	V
Supply Current	ICC		1.0		10.0	mA
	ICC, Sleep Mode		0.05		1.0	mA
	IVM		0		0.75	A
	IVM, Sleep Mode		0		1.5	mA
Ambient Temperature	Ta		0		70	°C
Capacitive Load Digital I/O	CI		0		100	pF

##### DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Fmax, SYSCLK		1.0	2.0	4.5	MHz
Twh, Twl, SYSCLK width high or low		40			ns
Advance Pulse Width		200			ns
Input Leakage, others				1	μA
Vil (SYSCLK, ADVANCE)				0.8	V
Vih (inputs above)		2.0			V
Vil (RESET, BRAKE)	VBRAKE ≥ 4.5V			0.8	V
Vih (RESET, BRAKE)	VBRAKE ≥ 4.5V	2.0			V

##### DIGITAL OUTPUTS, COMMU, REVCLK

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voh	Iout = -100 μA	2.4			V
Vol	Iout = 2.0 mA			0.4	V

##### VIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage		0		2.25	V
Input Current	0 ≤ Vin < 2.5V	-1		+1	μA

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#### ELECTRICAL SPECIFICATIONS (Continued)

##### OUTPUTS A, B, C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Routup	Output in high state VM = 4.75V	0.05		1.0	$\Omega$
Routlow	Output driving low, VM = 4.75V	0.05		1.0	$\Omega$

##### SENSE

Vin, SENSE	Normal operation	0.0		0.5	V
Iin, SENSE	$0.0 \leq V_{in} < 1.0V$	-10		+10	$\mu A$
Cin				20	pF
Transconductance gain from VIN to motor current (steady-state) will be given by: $G = I_{motor}/V_{IN} = 1/R_{sense} \cdot 4.$					

##### CT

Rin	$-0.3V \leq V_{in} < 15V$	30K			$\Omega$
Cin				10	pF

##### V BRAKE

Ibst (run)	VCC = 4.75V			100	$\mu A$
Ibst (float)	VCC $\leq$ 0.5V		25	100	$\mu A$
Ibst (brake)	VCC $\leq$ 0.5V		3	10	$\mu A$

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#### PACKAGE PIN DESIGNATIONS

(Top View)

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36-Pin SOM

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