Single-chip 8-bit EPROM microcontroller with 10-bit A/D, capture compare timer, high-speed outputs, PWM

87C552

CFEATURES

- 80C51 central processing unit
- 8k × 8 EPROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 × 8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Extended temperature ranges
- OTP package available

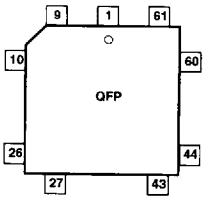
DESCRIPTION

The 87C552 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C552 has the same instruction set as the 80C51. The 87C552 is an EPROM version of the 83C552.

The 87C552 contains an 8k × 8 EPROM program memory, a volatile 256 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C552 can be expanded using standard TTL compatible memories and logic.

In addition, the 87C552 has two software selectable modes of power reduction — idle mode and power-down mode The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative

PIN CONFIGURATION



Pin	Function	Pin	Function
1	P5 0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2 0/A08
6	$\overline{EW}$	40	P2 1/A09
7	P4 0/CMSR0	41	P2 2/A10
8	P4 1/CMRS1	42	P2 3/A11
9	P4 2CMSR2	43	P2 4/A12
10	P4 3/CMSR3	44	P2 5/A13
11	P4 4/CMSR4	45	P2 6/A14
12	P4 5/CMSR5	45	P2 7/A15
13	P4 6/CMT0	47	$\overline{PSEN}$
14	P4 7/CMT1	48	ALE/$\overline{PROG}$
15	RST	49	$\overline{EA}$/V_{PP}
16	P1 0/CT0I	50	P0 7/AD7
17	P1 1/CT1I	51	P0 6/AD6
18	P1 2/CT2I	52	P0 5/AD5
19	P1 3/CT3I	53	P0 4/AD4
20	P1 4/T2	54	P0 3/AD3
21	P1 5/RT2	55	P0 2/AD2
22	P1 6/SCL	56	P0 1/AD1
23	P1 7/SDA	57	P0 0/AD0
24	P3 0/RxD	58	AVref-
25	P3 1TxD	59	AVref+
26	P3 2/$\overline{INT0}$	60	AV_{SS}
27	P3 3/$\overline{INT1}$	61	AV_{DD}
28	P3 4/T0	62	P5 7/ADC7
29	P3 5/T1	63	P5 6/ADC6
30	P3 6/$\overline{WR}$	64	P5 5/ADC5
31	P3 7/$\overline{RD}$	65	P5 4/ADC4
32	NC	66	P5 3/ADC3
33	NC	67	P5 2/ADC2
34	XTAL2	68	P5 1/ADC1

ORDERING INFORMATION

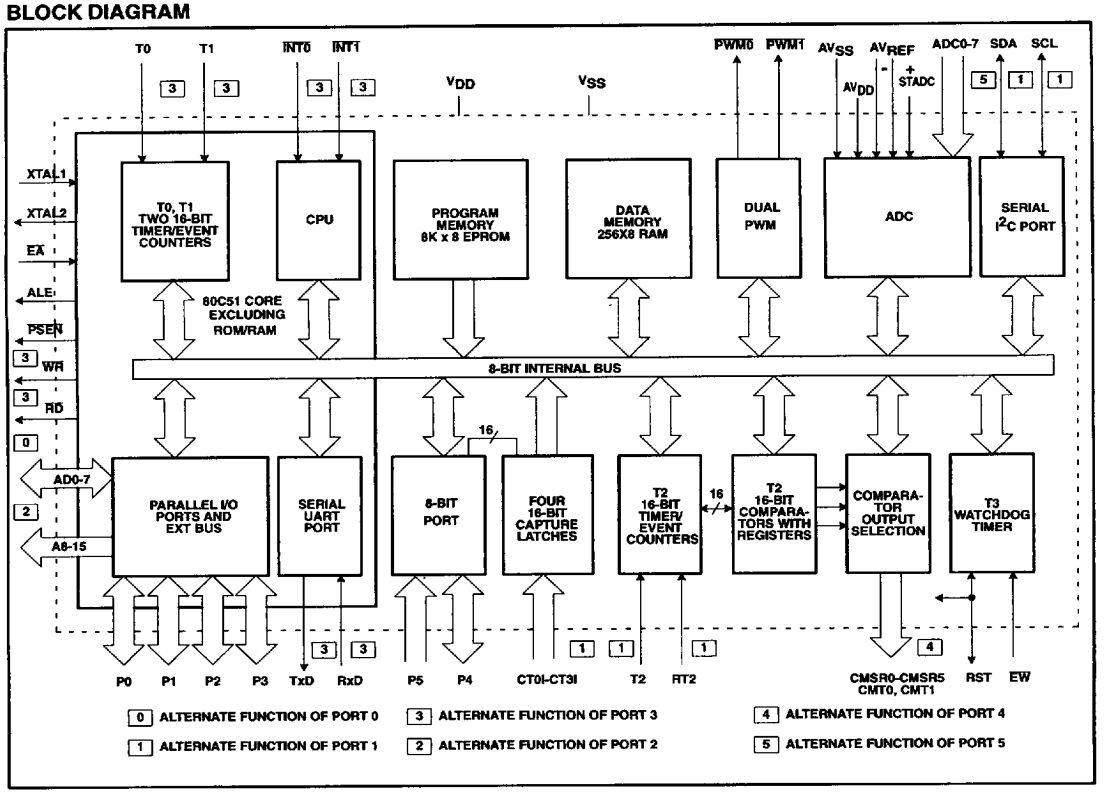
DESCRIPTION	ORDER CODE	FREQUENCY	PKG DESIGNATOR*
Ceramic Quad Flat Pack with J Bend Leads	87C552/BMA	3 5 - 12MHz	GQCC1-J68

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

Single-chip 8-bit EPROM microcontroller with 10-bit A/D, capture compare timer, high-speed outputs, PWM

87C552

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{DD}	2	I	**Digital Power Supply:** +5V power supply pin during normal operation, idle and power-down mode.
STADC	3	I	**Start ADC Operation:** Input starting analog to digital conversion (ADC operation can also be started by software).
$\overline{PWM0}$	4	O	**Pulse Width Modulation:** Output 0.
$\overline{PWM1}$	5	O	**Pulse Width Modulation:** Output 1.
$\overline{EW}$	6	I	**Enable Watchdog Timer:** Enable for T3 watchdog timer and disable power-down mode.
P0.0-P0.7	57-50	I/O	**Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 is also used to input the code byte during programming and to output the code byte during verification.
P1.0-P1.7	16-23	I/O	**Port 1:** 8-bit I/O port. Alternate functions include:
	16-21	I/O	**(P1.0-P1.5):** Quasi-bidirectional port pins.
	22-23	I/O	**(P1.6, P1.7):** Open drain port pins.
	16-19	I	**CT0I-CT3I (P1.0-P1.3):** Capture timer input signals for timer T2.
	20	I	**T2 (P1.4):** T2 event input
	21	I	**RT2 (P1.5):** T2 timer reset signal. Rising edge triggered.
	22	I/O	**SCL (P1.6):** Serial port clock line I^2C-bus.
	23	I/O	**SDA (P1.7):** Serial port data line I^2C-bus. Port 1 is also used to input the lower order address byte during EPROM programming and verification. A0 is on P1.0, etc.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
P2.0-P2.7	39-46	I/O	**Port 2:** 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08-A15) Port 2 is also used to input the upper order address during EPROM programming and verification A8 is on P2 0, A9 on P2 1, through A12 on P2 4
P3 0-P3.7	24-31 24 25 26 27 28 29 30 31	I/O	**Port 3:** 8-bit quasi-bidirectional I/O port Alternate functions include: **RxD(P3.0):** Serial input port **TxD (P3.1):** Serial output port. **$\overline{INT0}$ (P3.2):** External interrupt **$\overline{INT1}$ (P3.3):** External interrupt **T0 (P3.4):** Timer 0 external input **T1 (P3.5):** Timer 1 external input **$\overline{WR}$ (P3.6):** External data memory write strobe. **$\overline{RD}$ (P3.7):** External data memory read strobe.
P4.0-P4.7	7-14 7-12 13, 14	I/O O O	**Port 4:** 8-bit quasi-bidirectional I/O port. Alternate functions include **CMSR0-CMSR5 (P4.0-P4.5):** Timer T2 compare and set/reset outputs on a match with timer T2 **CMT0, CMT1 (P4.6, P4.7):** Timer T2 compare and toggle outputs on a match with timer T2
P5 0-P5 7	68-62, 1	I	**Port 5:** 8-bit input port **ADC0-ADC7 (P5.0-P5.7):** Alternate function Eight input channels to ADC
RST	15	I/O	**Reset:** Input to reset the 87C552 It also provides a reset pulse as output when timer T3 overflows.
XTAL1	35	I	**Crystal Input 1:** Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator Receives the external clock signal when an external oscillator is used
XTAL2	34	O	**Crystal Input 2:** Output of the inverting amplifier that forms the oscillator Left open-circuit when an external clock is used
V_{SS}	36, 37	I	**Digital ground.**
$\overline{PSEN}$	47	O	**Program Store Enable:** Active-low read strobe to external program memory
ALE/$\overline{PROG}$	48	O	**Address Latch Enable:** Latches the low byte of the address during accesses to external memory It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming
$\overline{EA}$/V_{PP}	49	I	**External Access:** When $\overline{EA}$ is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL low level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float This pin also receives the 12 75V programming supply voltage (V_{PP}) during EPROM programming
AV_{REF-}	58	I	**Analog to Digital Conversion Reference Resistor:** Low-end
AV_{REF+}	59	I	**Analog to Digital Conversion Reference Resistor:** High-end.
AV_{SS}	60	I	**Analog Ground**
AV_{DD}	61	I	**Analog Power Supply**

NOTE: To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0 5V or V_{SS} –0 5V, respectively.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier The pins can be configured for use as an on-chip os- cillator, as shown in the logic symbol, page 1 To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles At power-on, the voltage on V_{DD} and RST must come up at the same time for a proper start-up

IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PWM0/ PWM1
Idle	Internal	1	1	Data	Data	Data	Data	Data	High
Idle	External	1	1	Float	Data	Address	Data	Data	High
Power-down	Internal	0	0	Data	Data	Data	Data	Data	High
Power-down	External	0	0	Float	Data	Data	Data	Data	High

Serial Control Register (S1CON) - See Table 2

S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 2. Serial Clock Rates

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{OSC}	f_{OSC} DIVIDED BY
			12MHz	
0	0	0	47	256
0	0	1	54	224
0	1	0	62.5	192
0	1	1	75	160
1	0	0	12.5	960
1	0	1	100	120
1	1	0	200[1]	60
1	1	1	0.5 < 62.5	96 x (256 - (reload value Timer 1)) (Reload value range: 0 - 254 in mode 2)

ABSOLUTE MAXIMUM RATINGS[2, 3, 4]

PARAMETER	RATING	UNIT
Storage temperature range	-65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ to V_{SS}	-0.5 to +13	V
Voltage on any other pin to V_{SS}	-0.5 to +6.5	V
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W

DC ELECTRICAL CHARACTERISTICS

T_{amb} = -55°C to +125°C, V_{DD}, AV_{DD} = 5V ±10%, V_{SS}, AV_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[5]	MAX	
V_{DD}	Supply voltage		4 5		5 5	V
I_{DD}	Power supply current Active mode @ 12MHz Idle mode @ 12MHz Power down mode	See note 9		 11 5 1 3 3	 30 7 200	 mA mA µA
Inputs						
V_{IL}	Input low voltage, except $\overline{EA}$,P1 6/SCL, P1 7/SDA		-0.5		0 2V_{DD}-0 25	V
V_{IL1}	Input low voltage to $\overline{EA}$		-0.5		0 2V_{DD}-0 45	V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA[9]		-0 5		0 3V_{DD}	V
V_{IH}	Input high voltage, except XTAL1, RST, P1 6/SCL, P1 7/SDA		0 2V_{DD}+0.10		V_{DD}+0.45	V
V_{IH1}	Input high voltage, XTAL1, RST		0.7V_{DD}+0 2		V_{DD}+0 5	V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA[9]		0 7V_{DD}		6 0	V
I_{IL}	Logical 0 input current, ports 1, 2, 3, 4, except P1.6/SCL, P1.7/SDA	V_{IN} = 0.45V			-75	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3, 4, except P1.6/SCL, P1.7/SDA	See note 8			-750	µA
I_{IL1}	Input leakage current, port 0, $\overline{EA}$, STADC, $\overline{EW}$	0 45V<V_I<V_{DD}			±10	µA
I_{IL2}	Input leakage current, P1 6/SCL, P1 7/SDA	0V<V_I<6V 0V<V_{DD}<5 5V			±10	µA
Outputs						
V_{OL}	Output low voltage, ports 1, 2, 3, 4 except P1 6/SCL, P1.7/SDA	I_{OL} = 1 6mA[6]			0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$	I_{OL} = 3 2mA[6]			0.45	V
V_{OL2}	Output low voltage, P1 6/SCL, P1 7/SDA	I_{OL} = 3.0mA[6]			0 4	V
V_{OH}	Output high voltage, ports 1, 2, 3, 4, except P1 6/SCL, P1.7/SDA	I_{OH} = -60µA I_{OH} = -25µA I_{OH} = -10µA	2 4 0 75V_{DD} 0.9V_{DD}			V V V
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)[7]	I_{OH} = -400µA I_{OH} = -150µA I_{OH} = -40µA	2.4 0 75V_{DD} 0.9V_{DD}			V V V
V_{OH2}	High level output voltage (RST)	I_{OH} = -400µA I_{OH} = -120µA	2.4 0 8V_{DD}			V V
R_{RST}	Internal reset pull-down resistor		50		150	kΩ
C_{IO}	I/O buffer pin capacitance[13]	Test freq = 1MHz, T_A = 25°C			10	pF
	Except I/O buffer and analog input pins[15]				20	pF
Analog Inputs						
AV_{DD}	Analog supply voltage[10]	AV_{DD} = V_{DD}±0.2V	4 5		5 5	V
AI_{DD}	Analog supply current. Operating Idle mode Power-down	Port 5 = 1 4V AV_{DD} = 2-5.5V			 1.1 50 50	 mA µA µA
AV_{IN}	Analog input voltage		AV_{SS}-0.2		AV_{DD}+0 2	V
AV_{REF}	Reference voltage: AV_{REF-} Reference voltage: AV_{REF+}		AV_{SS}-0 2		 AV_{DD}+0 2	V V
R_{REF}	Resistance between AV_{REF+} and AV_{REF-}		10		50	kΩ

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[4]	MAX	
Analog Inputs (Continued)						
C_{IA}	Analog input capacitance[14]	Test freq = 1MHz, $T_A = 25^{\circ}C$			15	pF
t_{ADS}	Sampling time				$8t_{CY}$	µs
t_{ADC}	Conversion time (including sampling time)				$50t_{CY}$	µs
DL_e	Differential non-linearity[12]		-1		+2	LSB
IL_e	Integral non-linearity[12]				±2	LSB
OS_e	Offset error[12]				±2	LSB
G_e	Gain error[12]				0.4	%
M_{CTC}	Channel to channel matching				±1	LSB
C_t	Crosstalk[13]	0-100kHz			-60	dB

AC ELECTRICAL CHARACTERISTICS[14]

T_{amb} = -55°C to +125°C, V_{DD}, AV_{DD} = 5V ±10%, V_{SS}, AV_{SS} = 0V

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	1	Oscillator frequency			3.5	12	MHz
t_{LHLL}	1	ALE pulse width	112		$2t_{CLCL}$-55		ns
t_{AVLL}	1	Address valid to ALE low	13		t_{CLCL}-70		ns
t_{LLAX}	1	Address hold after ALE low	33		t_{CLCL}-50		ns
t_{LLIV}	1	ALE low to valid instruction in		219		$4t_{CLCL}$-115	ns
t_{LLPL}	1	ALE low to $\overline{PSEN}$ low	28		t_{CLCL}-55		ns
t_{PLPH}	1	$\overline{PSEN}$ pulse width	190		$3t_{CLCL}$-60		ns
t_{PLIV}	1	$\overline{PSEN}$ low to valid instruction in		130		$3t_{CLCL}$-120	ns
t_{PXIX}	1	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	1	Input instruction float after $\overline{PSEN}$		59		t_{CLCL}-25	ns
t_{AVIV}	1	Address to valid instruction in		272		$5t_{CLCL}$-140	ns
t_{PLAZ}	1	$\overline{PSEN}$ low to address float		25		25	ns
Data Memory							
t_{RLRH}	2, 3	$\overline{RD}$ pulse width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	2, 3	$\overline{WR}$ pulse width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	2, 3	$\overline{RD}$ low to valid data in		232		$5t_{CLCL}$-185	ns
t_{RHDX}	2, 3	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	2, 3	Data float after $\overline{RD}$		82		$2t_{CLCL}$-85	ns
t_{LLDV}	2, 3	ALE low to valid data in		497		$8t_{CLCL}$-170	ns
t_{AVDV}	2, 3	Address to valid data in		565		$9t_{CLCL}$-185	ns
t_{LLWL}	2, 3	ALE low to $\overline{RD}$ or $\overline{WR}$ low	185	315	$3t_{CLCL}$-65	$3t_{CLCL}$+65	ns
t_{AVWL}	2, 3	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	188		$4t_{CLCL}$-145		ns
t_{QVWX}	2, 3	Data valid to $\overline{WR}$ transition	8		t_{CLCL}-75		ns
t_{WHQX}	2, 3	Data hold after $\overline{WR}$	18		t_{CLCL}-65		ns
t_{RLAZ}	2, 3	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	2, 3	$\overline{RD}$ or $\overline{WR}$ high to ALE high	18	148	t_{CLCL}-65	t_{CLCL}+65	ns
External Clock							
t_{CHCX}	5	High time[15]	20		20		ns
t_{CLCX}	5	Low time[15]	20		20		ns
t_{CLCH}	5	Rise time[15]		20		20	ns
t_{CHCL}	5	Fall time[15]		20		20	ns
Shift Register							
t_{XLXL}	4	Serial port clock cycle time[15]	1.0		$12t_{CLCL}$		µs
t_{QVXH}	4	Output data setup to clock rising edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	4	Output data hold after clock rising edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	4	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	4	Clock rising edge to input data valid		700		$10t_{CLCL}$-133	ns

NOTES: On following page.

NOTES:

1. These frequencies exceed the upper limit of 100kHz of the I²C-bus specification and cannot be used in an I²C-bus application.
2. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
5. Typical ratings are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temperature, 5V.
6. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
7. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{DD}$ specification when the address bits are stabilizing.
8. Pins of ports 1 (except P1.6, P1.7), 2, 3 and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
9. See Figures 8 through 11 for I_{DD} test conditions.
10. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
11. The following condition must not be exceeded: $V_{DD} - 0.2V < AV_{DD} < V_{DD} = 0.2V$.
12. Conditions: $AV_{REF-} = 0V$; $AV_{DD} = 5.0V$, $AV_{REF+} = 4.977V$. ADC is monotonic with no missing codes.
13. This should be considered when both analog and digital signals are simultaneously input to port 5.
14. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
15. These values are characterized but not 100% production tested.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A - Address
C - Clock
D - Input data
H - Logic level high
I - Instruction (program memory contents)
L - Logic level low, or ALE
P - $\overline{PSEN}$
Q - Output data
R - $\overline{RD}$ signal
t - Time
V - Valid
W - $\overline{WR}$ signal
X - No longer a valid logic level
Z - Float

Examples:

t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

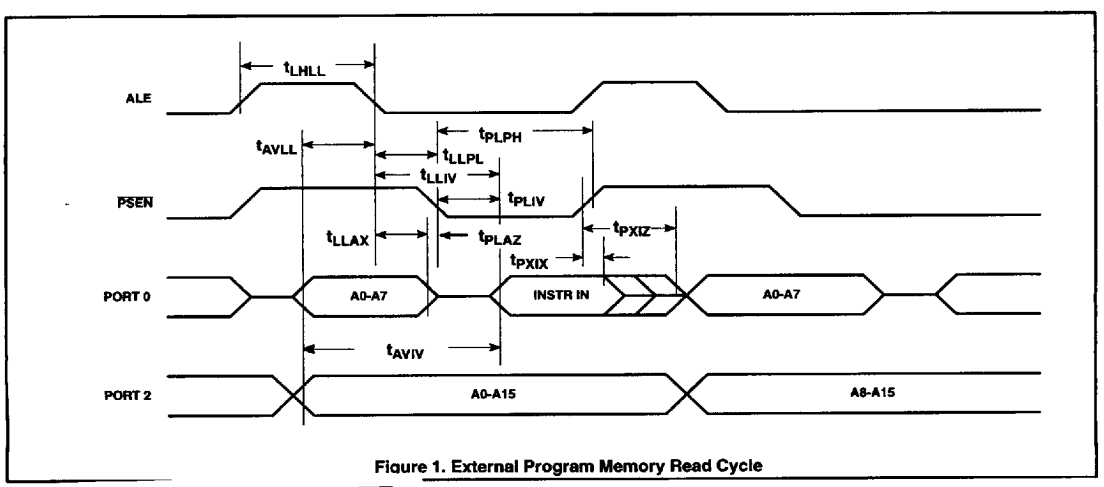


Figure 1. External Program Memory Read Cycle

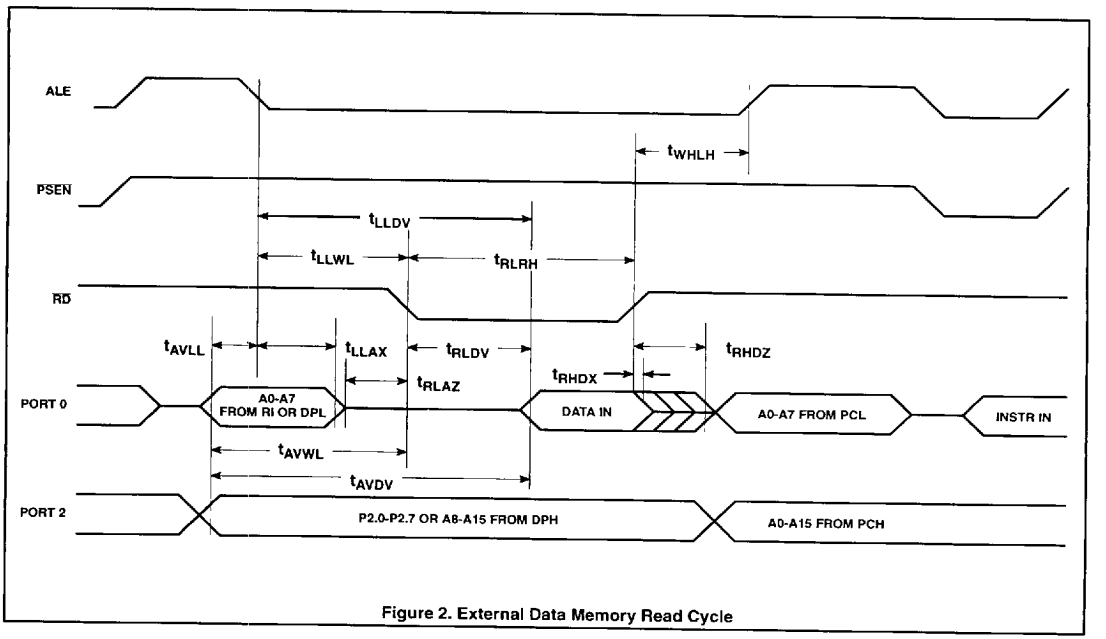


Figure 2. External Data Memory Read Cycle

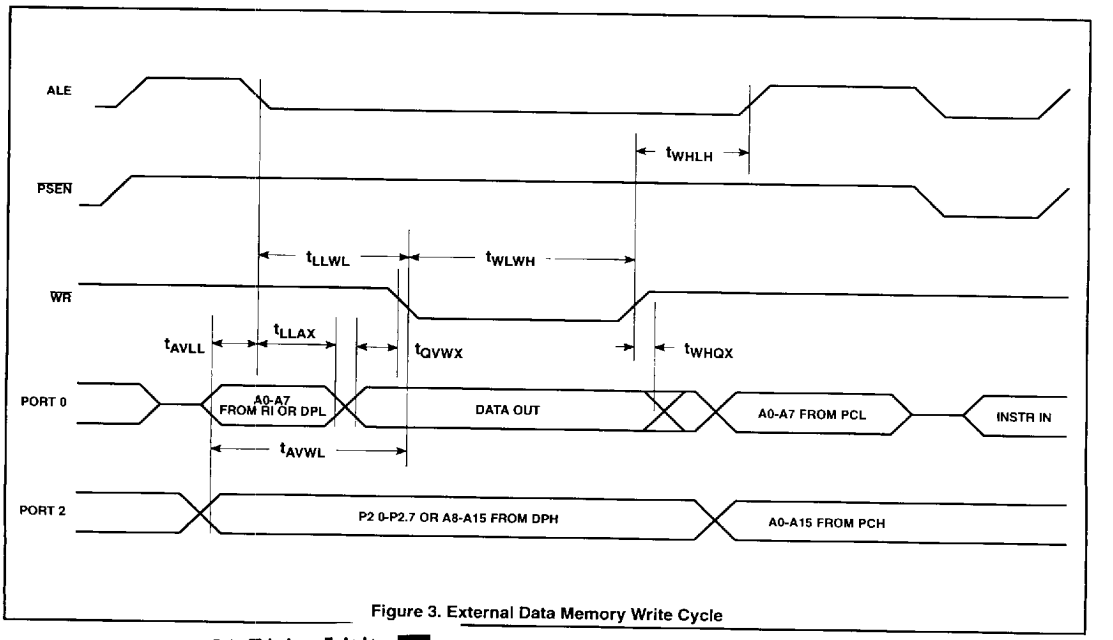


Figure 3. External Data Memory Write Cycle

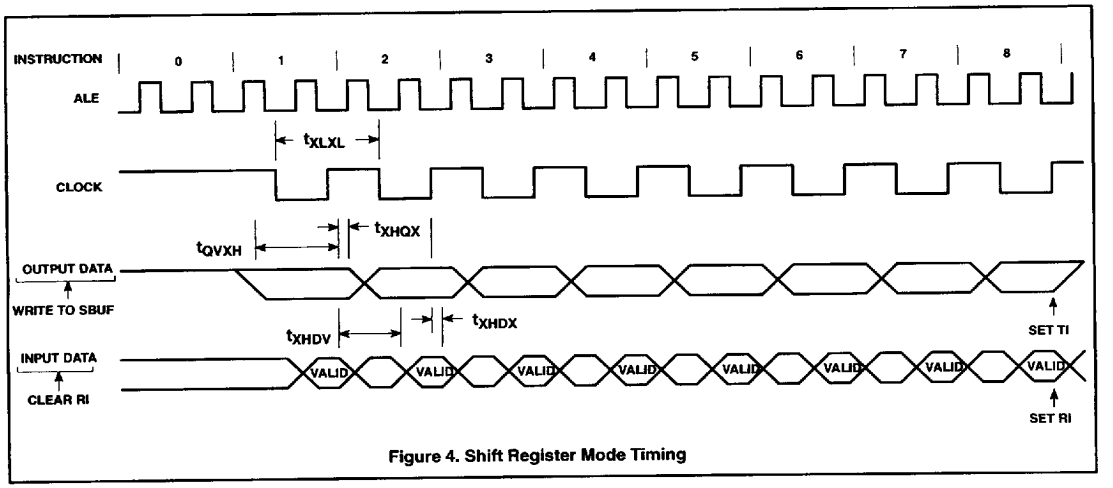


Figure 4. Shift Register Mode Timing

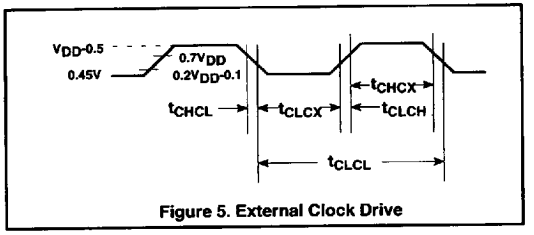
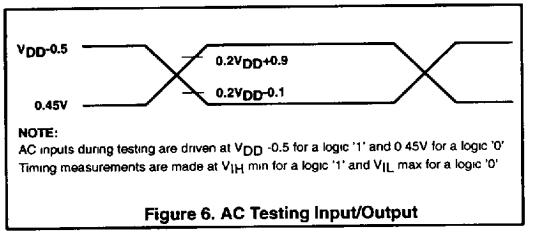
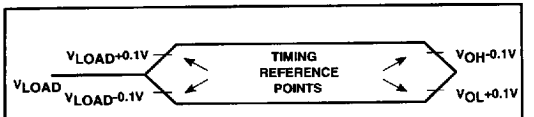


Figure 5. External Clock Drive



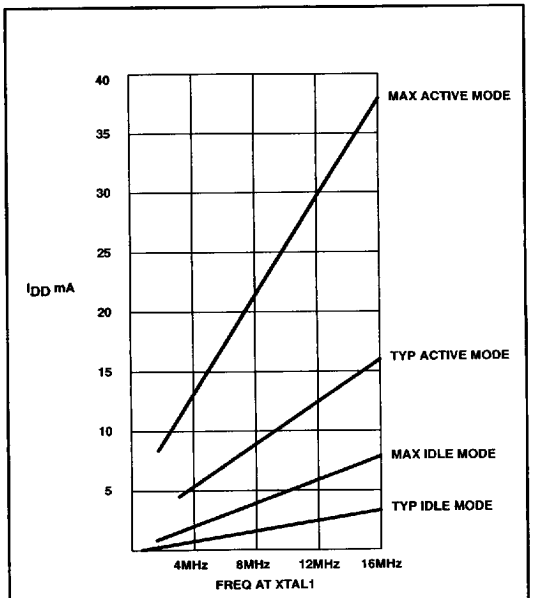
NOTE:
AC inputs during testing are driven at V_{DD} -0.5 for a logic '1' and 0.45V for a logic '0'
Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'

Figure 6. AC Testing Input/Output



NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs $I_{OH}/I_{OL} \geq \pm 20$mA

Figure 7. Float Waveform



NOTE:
Valid only within frequency specifications of the device under test
Maximum values takenat V_{DD} = 5.5V and worst case temperature
Typical values taken at V_{DD} = 5.0V and 25°C

Figure 8. I_{DD} vs. FREQ

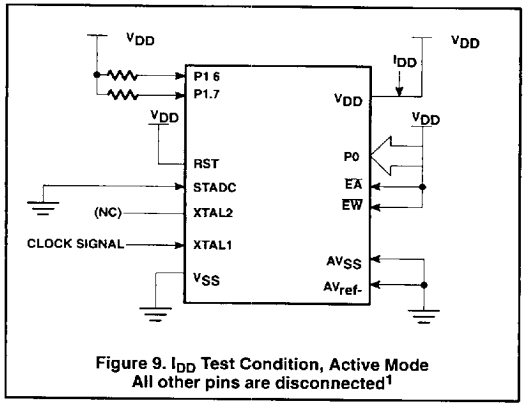


Figure 9. I_{DD} Test Condition, Active Mode
All other pins are disconnected[1]

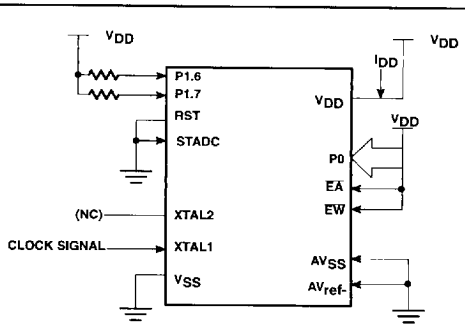


Figure 10. I_{DD} Test Condition, Idle Mode
All other pins are disconnected[2]

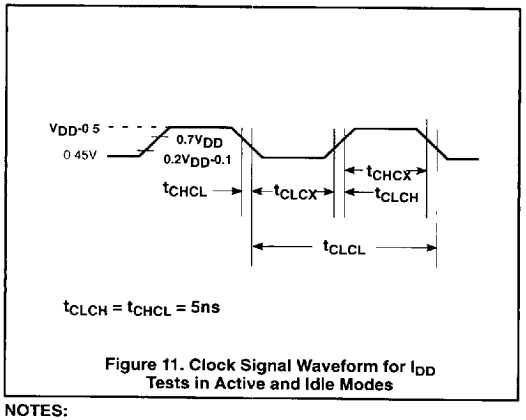


Figure 11. Clock Signal Waveform for I_{DD} Tests in Active and Idle Modes

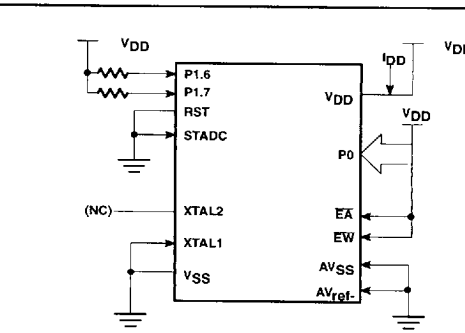


Figure 12. I_{DD} Test Condition, Power Down Mode
All other pins are disconnected. V_{DD} = 2V to 5.5V[3]

NOTES:

1 Active Mode:
- a. The following pins must be forced to V_{DD}: $\overline{EA}$, RST, Port 0, and $\overline{EW}$.
- b. The following pins must be forced to V_{SS}: STADC, AV_{ss}, and AV_{ref-}.
- c. Ports 1 6 and 1 7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins
- d The following pins must be disconnected XTAL2 and all pins not specified above.

2. Idle Mode
- a. The following pins must be forced to V_{DD}: $\overline{EA}$, Port 0, and $\overline{EW}$.
- b The following pins must be forced to V_{SS}. RST, STADC, AV_{ss}, and AV_{ref-}.
- c Ports 1 6 and 1 7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins. These pins must not have logic 0 written to them prior to this measurement
- d The following pins must be disconnected XTAL2 and all pins not specified above.

3 Power-Down Mode
- a. The following pins must be forced to V_{DD}: $\overline{EA}$, Port 0, and $\overline{EW}$
- b The following pins must be forced to V_{SS}: RST, STADC, XTAL1, AV_{ss}, and AV_{ref-}.
- c Ports 1 6 and 1 7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
- d. The following pins must be disconnected: XTAL2 and all pins not specified above.

Single-chip 8-bit EPROM microcontroller with 10-bit A/D, capture compare timer, high-speed outputs, PWM — 87C552

EPROM CHARACTERISTICS

The 87C552 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C552 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C552 manufactured by Philips Semiconductors.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, theencryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 13 and 14. Figure 15 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 13. Note that the 87C552 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 13. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$, and pins of ports 2 and 3 specified in Table 3 are held at the "Program Code Data" levels indicated in Table 3. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 14.

To program the encryption table, repeat the 25-pulse programming sequence for addresses 0 through 1FH, using the "Pgm Encryption Table" levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25-pulse programming sequence using the "Pgm Lock Bit" levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be red is applied to ports 1 and 2 as shown in Figure 15. The other pins are held at the "Verify Code Data" levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

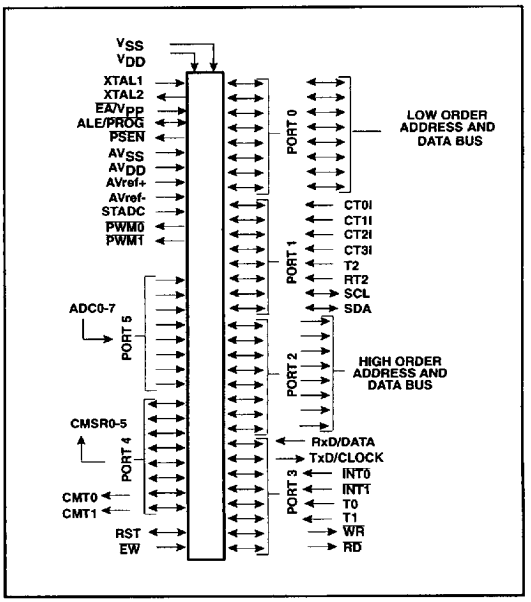
(030H) = 15H indicates manufactured by Signetics

(031H) = 94H indicates 87C552

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

LOGIC SYMBOL



Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to the light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000µW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient. Erasure leaves the array in an all 1s state.

™Trademark phrase of Intel Corporation.

Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
0 = Valid low for that pin; 1 = valid high for that pin.
V_{PP} = 12.75V ±0.25V
V_{DD} = 5V ±10% during programming and verification.
* ALE/PROG receives 25 programming pulses whill V_{PP} is held at 12.75V. Each programming pulse is low for 100µs (±10µs) and high for a minimum of 10µs.

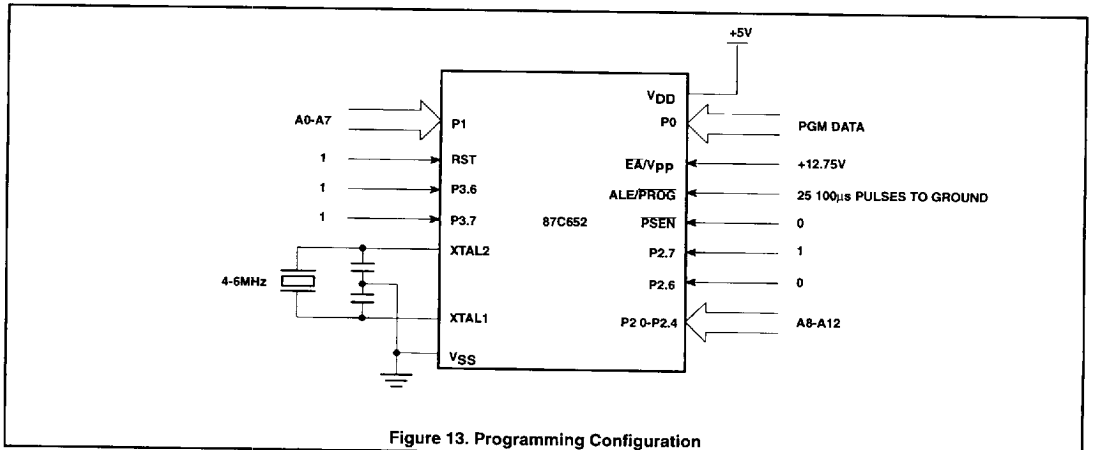


Figure 13. Programming Configuration

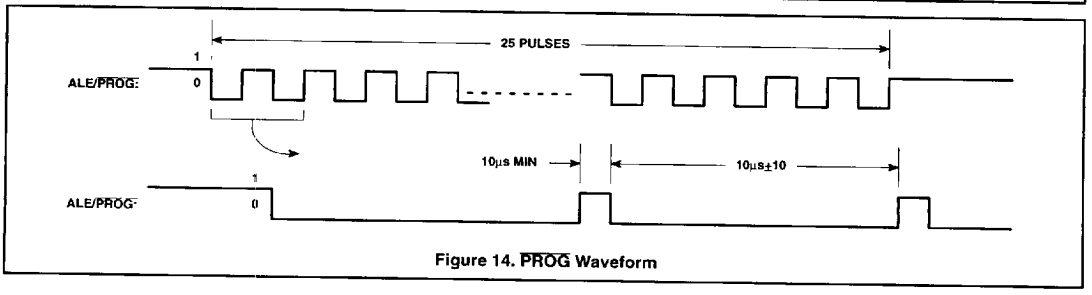


Figure 14. PROG Waveform

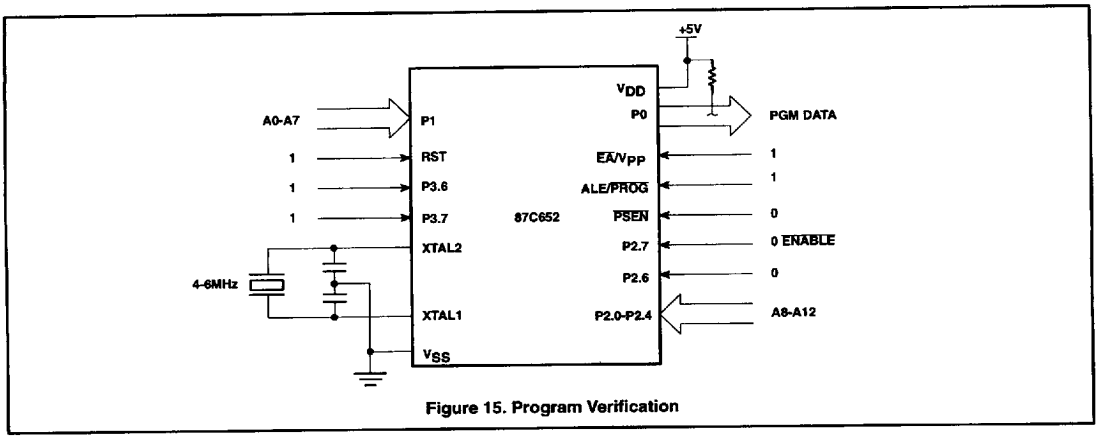


Figure 15. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{DD} = 5V±10%, V_{SS} = 0V (See Figure 16)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs

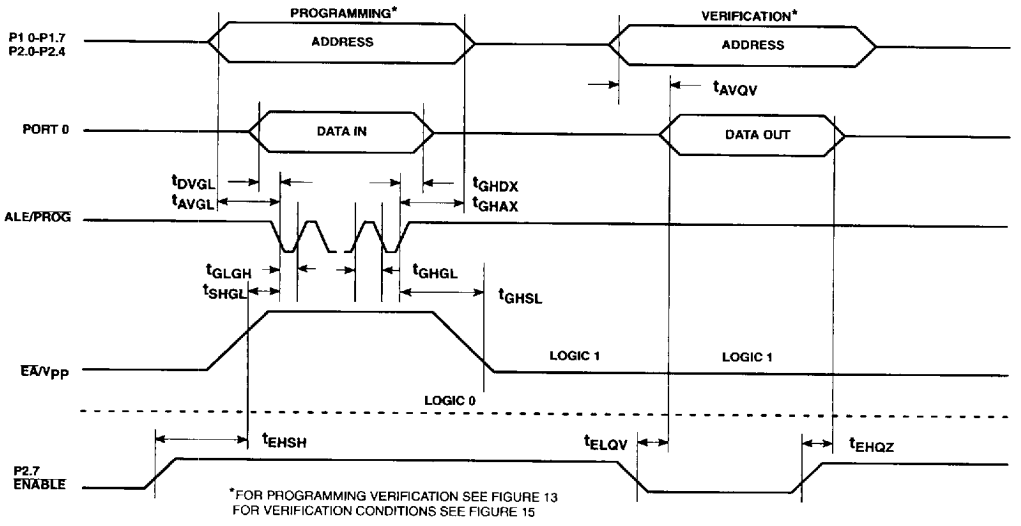


Figure 16. EPROM Programming and Verification