



T-52-07

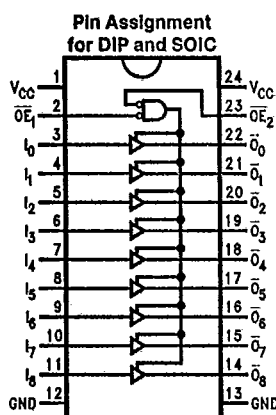
74FR9240 9-Bit Buffer/Line Driver with TRI-STATE Outputs

74FR9240**9-Bit Buffer/Line Driver with TRI-STATE® Outputs****General Description**

The 'FR9240 is an inverting 9-bit buffer and line driver designed to be employed as memory and address driver, clock driver and bus oriented transmitter or receiver.

Features

- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64 mA and source 15 mA
- Guaranteed multiple output switching, 250 pF delay and pin-to-pin skew
- Guaranteed 4000V minimum ESD protection
- 9-bit architecture for systems carrying parity

Connection Diagram**Pin Description**

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active Low)
I_0-I_8	Inputs
$\overline{O}_0-\overline{O}_8$	Outputs

Truth Table

$\overline{OE}_1$	$\overline{OE}_2$	I_n	$\overline{O}_n$
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

TL/F/10912-1

9000-2693

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Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in High State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in Low State (Max)

T-52-07Twice the Rated I_{OL} (mA)

ESD Last Passing Voltage (Min)

4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature

Commercial

0°C to +70°C

Supply Voltage

Commercial

+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74FR			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input High Voltage	2.0			V		Recognized High Signal
V _{IL}	Input Low Voltage			0.8	V		Recognized Low Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output High Voltage	2.4			V	Min	I _{OH} = -3 mA
		2.0			V	Min	I _{OH} = -15 mA
V _{OL}	Output Low Voltage			0.55	V	Min	I _{OL} = 64 mA
I _{IH}	Input High Current			5	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input High Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input Low Current			-150	μA	Max	V _{IN} = 0.5V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Circuit Leakage Current			3.75	μA	0.0	V _{IOD} = 150 mV, All Other Pins Grounded
I _{OZH}	Output Leakage Current			20	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-20	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	-100		-225	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.25V
I _{CC}	Power Supply Current		9	13	mA	Max	All Outputs High
I _{CCL}	Power Supply Current		37	45	mA	Max	All Outputs Low
I _{CCZ}	Power Supply Current		31	38	mA	Max	Outputs TRI-STATE
C _{IN}	Input Capacitance		8.0		pF	5.0	

AC Electrical Characteristics

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Symbol	Parameter	74FR			74FR		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = \text{Comm}$ $V_{CC} = \text{Comm}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.0	3.3	4.5	1.0	4.5	ns
		1.0	2.9	4.5	1.0	4.5	
t_{pZH} t_{pZL}	Output Enable Time	2.6	4.0	6.6	2.6	6.6	ns
		2.6	6.3	6.6	2.6	6.6	
t_{pHZ} t_{pLZ}	Output Enable Time	1.7	3.3	6.2	1.7	6.2	ns
		1.7	2.9	6.2	1.7	6.2	

Extended AC Characteristics

Symbol	Parameter	74FR		74FR		Units
		$T_A = \text{Comm}$ $V_{CC} = \text{Comm}$ $C_L = 50 \text{ pF}$ Eight Outputs Switching (Note 2)		$T_A = \text{Comm}$ $V_{CC} = \text{Comm}$ $C_L = 250 \text{ pF}$ (Note 3)		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.0 1.0	6.0 6.0	2.3 2.3	8.3 8.3	ns
t_{PZH} t_{PZL}	Output Enable Time	2.6 2.6	7.2 7.2			
t_{PHZ} t_{PLZ}	Output Disable Time	1.7 1.7	6.6 6.6			ns
t_{OSHL} (Note 1)	Pin to Pin Skew for HL Transitions		2.0			
t_{OSLH} (Note 1)	Pin to Pin Skew for LH Transitions		1.1			ns
t_{OST} (Note 1)	Pin to Pin Skew for HL/LH Transitions		3.0			ns

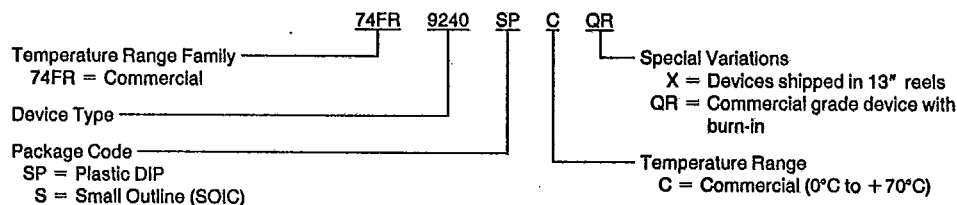
Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching high to low, (t_{OSHL}), low to high, (t_{OSLH}), or high to low and/or low to high, (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all low-to-high, high-to-low, TRI-STATE-to-high, etc.

Note 3: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



NATIONAL SEMICONDUCTOR (LOGIC)

0.300-0.320
(7.62-8.128)

0.009-0.015
(0.229-0.381)

95° ± 5°

0.260
(7.112) MIN

0.325+0.040/-0.015
(8.255-8.381)

N24C (REV F)

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