T-46-13-47

PALC18U8Q-25
PALC18U8Q-35

CMOS Universal Programmable Array Logic
U.S. Patents 4124899 and 4717912

DISTINCTIVE CHARACTERISTICS

- CMOS technology provides quarter power (only 55 mA) while matching bipolar speeds
- 20-pin universal-architecture programmable logic for ease of use
- Replaces discrete CMOS/TTL logic, reducing design time and cost and increasing reliability
- 10 dedicated inputs and 8 input/output macrocells for architectural flexibility
- Outputs programmable as registered or combinatorial in any combination
- Programmable output polarity
- Global asynchronous reset and synchronous preset for initialization
- Programmable enable/disable control
- Preloadable output registers for testability
- Automatic register reset on power up
- Security bit prevents design duplication by competitors
- UV-erasable in windowed 20-pin ceramic DIP package
- Cost-effective OTP 20-pin DIP and PLCC packages
- High-speed CMOS technology
  - –25 ns propagation delay for "-25" version
  - –35 ns propagation delay for "-35" version
- Supported by PALASM® 2 software
- Programmable on standard device programmers
- Fully tested for high programming and functional yields and high reliability

GENERAL DESCRIPTION

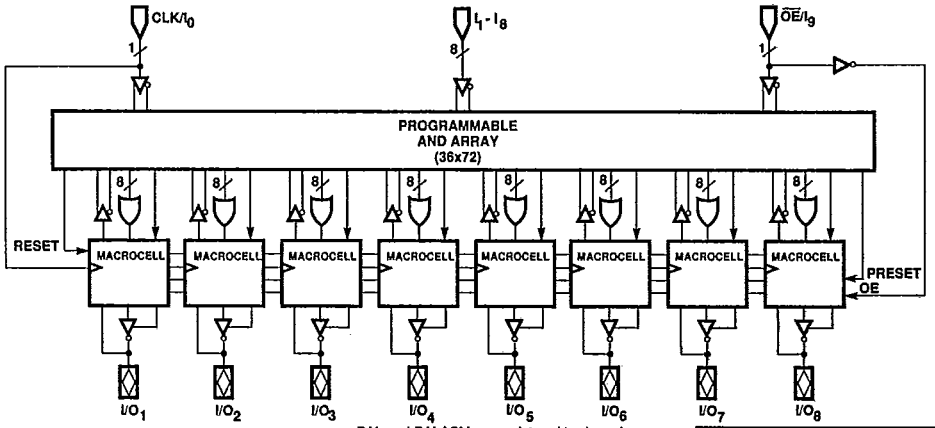
The PALC18U8Q is an advanced PAL® device built with low-power, high-speed, UV-erasable CMOS technology. Its eight macrocells provide a universal device architecture. The PALC18U8Q can functionally replace most 20-pin programmable logic devices.

Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM 2 design software, allowing automatic creation of a programming file based on Boolean or state equations. PALASM 2 software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALC18U8Q utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased by exposure to ultraviolet light.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, active HIGH or active LOW, with product term or pin enable control. The output configuration is determined by three bits controlling three multiplexers in each macrocell.

BLOCK DIAGRAM



Monolithic Memories
A Wholly Owned Subsidiary of Advanced Micro Devices

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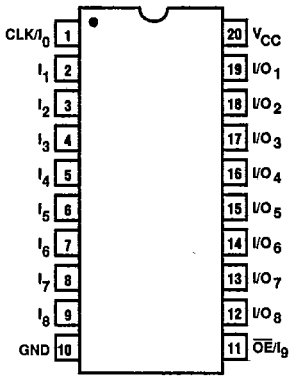
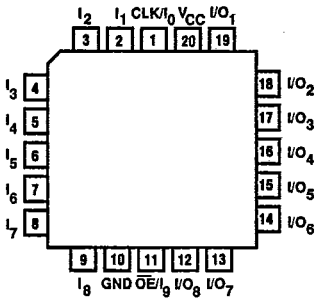
CONNECTION DIAGRAMS
(Top View)

DIP



PLCC



Pin Designations: I = Input
I/O = Input/Output
OE = Output Enable
CLK = Clock
V_{CC} = Supply Voltage
GND = Ground

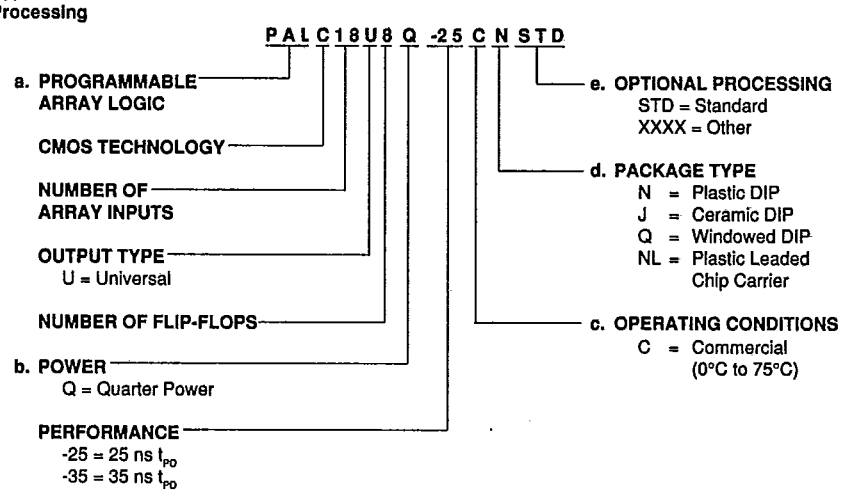
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Standard Products

AMD/MMI standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed/Power Option
c. Operating Conditions
d. Package Type
e. Optional Processing



Valid Combinations	
PALC18U8Q-25	CN, CJ, CQ, CNL
PALC18U8Q-35	

Valid Combinations
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The PALC18U8Q has ten dedicated input lines and eight programmable I/O macrocells. The macrocell is shown in Figure 1. Pin 1 serves either as an array input or as a clock for all flip-flops. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array.

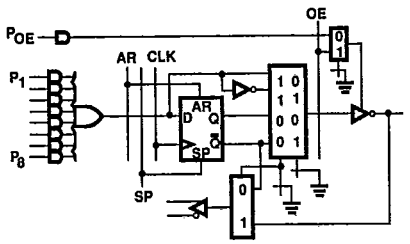


Figure 1. PALC18U8Q Macrocell

The programmable functions in the PALC18U8Q are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

Configuration Options

The output macrocell in the PALC18U8Q allows eight basic output configurations (Figure 2). The outputs can be either registered or combinatorial, and active HIGH or active LOW, to match the needs of the design. Two programmable bits in each macrocell control a 4:1 output multiplexer and a 2:1 feedback multiplexer. In addition, a third bit controls a 2:1 output enable multiplexer, allowing either a pin or a product term to control the output enable, providing global or local enable control, respectively. These three bits select one of the eight possible configurations for each output.

Multiplexer control lines are initially connected to GND (0) through a programmable cell, selecting the "0" path through the multiplexer. Programming the cell changes the control line to V_{cc} (1), selecting the "1" path.

Registered or Combinatorial Outputs

Each output of the PALC18U8Q includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH edge of the clock (pin 1). Any output can be configured to be combinatorial by selecting a multiplexer path that bypasses the output flip-flop. Bypass is automatically selected if requested in the design specification by using the equals sign (=) in the output equation, as opposed to the colon-equals (:=) for a registered output. The unprogrammed state is a registered output configuration. The registered configuration includes register feedback, while the combinatorial configuration includes I/O feedback.

Programmable I/O

Each macrocell has a three-state output buffer with programmable three-state control. Control can be programmed for each output as either global (pin) or local (product term). The unprogrammed state is local control. Local control will be provided if an equation is written for the enable function. If a product term controls the buffer, enable and disable can be a function of any combination of device inputs or output feedback. If no enable equation is written, PALASM 2 software selects global control for registered outputs and local control for combinatorial outputs, similar to standard devices. The macrocell provides a bidirectional I/O pin in the combinatorial configuration, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active HIGH or active LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by a programmable bit in the output macrocell, and affects both registered and combinatorial outputs. The unprogrammed configuration is active LOW. Selection is automatically performed according to the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active HIGH.

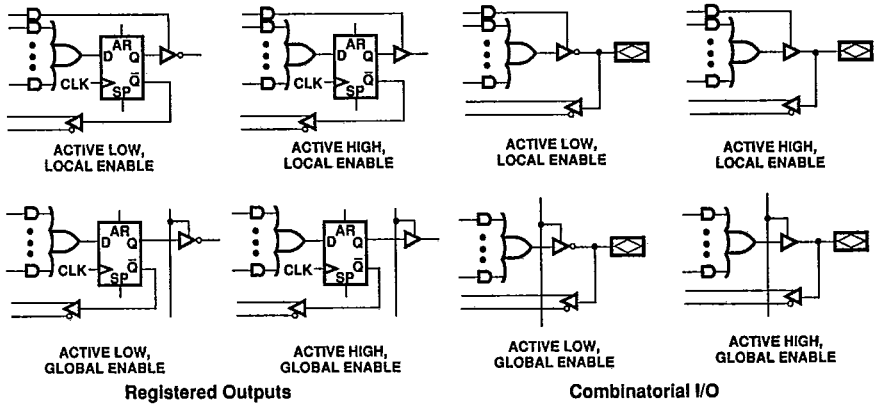


Figure 2. Configuration Options

Note that preset and reset control the flip-flop, not the output pin. Thus, if active-LOW polarity is selected, the effects of preset and reset on the output pin will be exchanged.

Programmable Preset and Reset

The eight macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic HIGH state following a LOW-to-HIGH transition of pin 1 (I_0/CLK) when the synchronous preset (SP) product term is asserted. The register will be forced to the logic LOW state independent of the clock when the asynchronous reset (AR) product term is asserted. Product term control allows preset and reset to be functions of any combination of device inputs and output feedback. Preset and reset are specified by Boolean equations. The outputs will be HIGH or LOW depending upon the polarity options chosen.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALC18U8Q will be HIGH or LOW depending on whether the output is active LOW or active HIGH, respectively. The V_{CC} rise must be monotonic, and the reset delay time is 1 µs maximum.

Register Preload

The register on the PALC18U8Q can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALC18U8Q design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors.

Quality and Testability

The PALC18U8Q offers a very high level of built-in quality. Extra programmable bits and the erasability of the device provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Programming and Erasing

The PALC18U8Q can be programmed on standard logic programmers. Approved programmers are listed in this datasheet. The PALC18U8Q may be erased by ultraviolet light when contained in the windowed package.

For erasure, the recommended ultraviolet light wavelength is 2537 Angstroms. The minimum dose required is 25000 mW-s/cm² (UV intensity x exposure time). For an ultraviolet lamp with a 12 mW/cm² power rating, the minimum exposure time would be 25000/12 seconds = 35 minutes. The device needs to be within 1 inch of the lamp during erasure.

Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. The recommended maximum dosage is 7258 W-s/cm².

Wavelengths of light less than 4000 Angstroms can partially erase the device in the windowed package. For this reason, an opaque label should be placed over the window, especially if the device will be exposed to sunlight or flourescent lighting for extended periods of time.

Basic PAL Device Notation

The multi-input gates in the PAL device's programmable AND-gate array are simplified in the logic diagrams. The PAL device notation for an AND gate, called a product term in a PAL device, is shown below.

Figure 3. PAL Device AND Gate

This is equivalent to the standard logic notation below.

Figure 4. Standard AND Gate

Each vertical line in the PAL device notation is a potential input to the AND gate. At each crosspoint is a programmable cell, which provides a connection in the unprogrammed state. When programmed, the input is disconnected. PAL device logic diagrams omit the X's at cell locations, for simplicity.

Since both the true and complement of every input is initially connected to the AND gate, the AND gate output will be LOW. Thus, unused AND gates are left unprogrammed.

Multiplexers in the PAL device logic diagrams use a simple notation for maximum clarity. A 2:1 multiplexer that selects X when the control is LOW and Y when the control is HIGH is shown below.

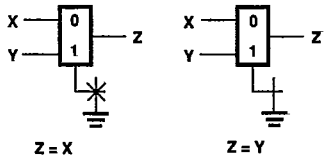


Figure 5. PAL Device Multiplexer

Note that the control is operated by a programmable cell that is initially connected to GND, selecting the "0" path through the multiplexer. When the cell is programmed, it is disconnected from GND and floats to V_{CC}, selecting the "1" path through the multiplexer.

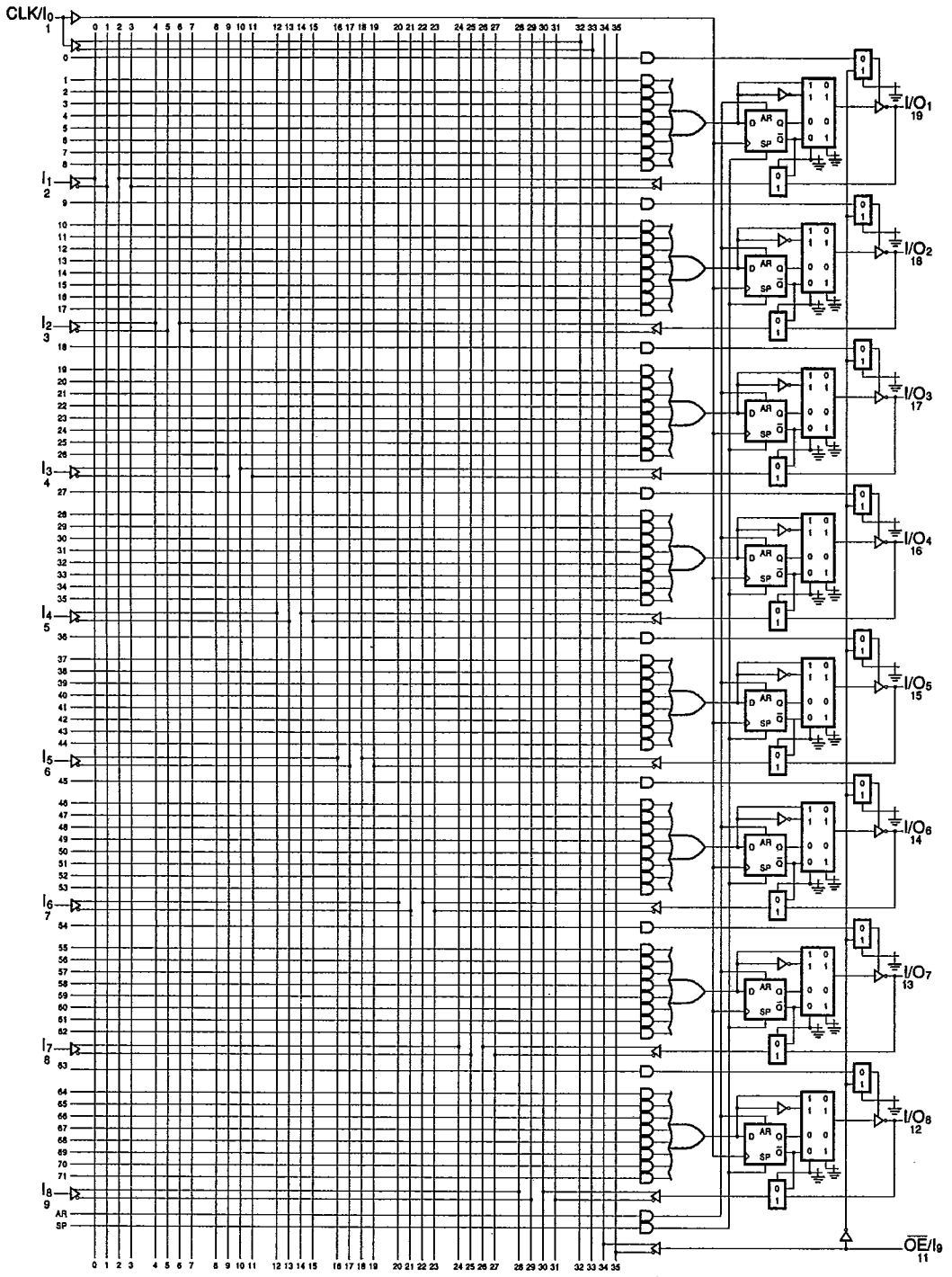


Figure 6. PALC18U8Q Logic Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature Under Bias ..... –55°C to +125°C
Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V
DC Output Voltage ..... –0.5 V to +7.0 V
DC Input Voltage ..... –3.0 V to +7.0 V
UV Light Exposure ..... 7258 W-s/cm²
Static Discharge Voltage ..... 2001 V
Latchup Current (T_A = 0°C to 75°C) ..... 200 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) Operating Free Air ..... 0°C to +75°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS Over operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input Leakage Current HIGH	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input Leakage Current LOW	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–10		µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)			10	µA
I_{OZH}	Off-State Output Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. (Note 2)			40	µA
I_{OZL}	Off-State Output Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. (Note 2)		–40		µA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0 V (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_O = 0), V_{CC} = Max.			55	mA

Notes: 1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, TA = +25°C, V_{IN} = 2.0 V at f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		8	

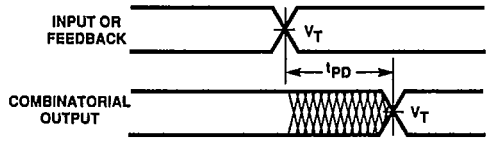
Notes: 1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS Over commercial operating range (Note 1)

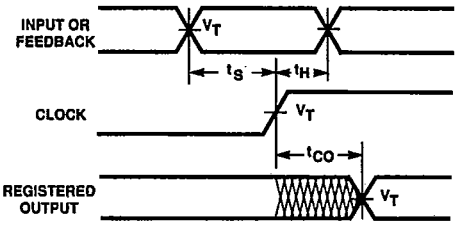
Parameter Symbol	Parameter Description		-35 Min.	-35 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Non-Registered Output (Note 2)	Active LOW		35		25	ns
		Active HIGH					
t_S	Setup Time from Input, Feedback or SP to Clock		25		20		ns
t_H	Hold Time		0		0		ns
t_{CO}	Clock to Output			25		15	ns
t_{CF}	Clock to Feedback (Note 3)			18		13	ns
t_{AR}	Asynchronous Reset to Registered Output			35		25	ns
t_{ARW}	Asynchronous Reset Width		35		25		ns
t_{ARR}	Asynchronous Reset Recovery Time		25		20		ns
t_{SPR}	Synchronous Preset Recovery Time		25		20		ns
t_{WL}	Width of Clock	LOW	20		15		ns
t_{WH}		HIGH	20		15		ns
f_{MAX}	Maximum frequency (Note 4)	External Feedback $1/(t_S + t_{CO})$	20		28.5		MHz
		Internal Feedback $1/(t_S + t_{CF})$	23.2		30		
		No Feedback $1/(t_{WH} + t_{WL})$	25		33		
t_{PZX}	Pin 11 to Output Enable (Note 5)			30		20	ns
t_{PXZ}	Pin 11 to Output Disable (Note 5)			30		20	ns
t_{EA}	Input to Output Enable (Notes 5, 6)			35		25	ns
t_{ER}	Input to Output Disable (Notes 5, 6)			35		25	ns

Notes:
1. Commercial Test Conditions: $R_1 = 560\ \Omega$, $R_2 = 1.1\ k\Omega$ (see Switching Test Circuit).
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF (including jig capacitance). $V_{IH} = 3$ V, $V_{IL} = 0$ V, $V_{OH} = V_{OL} = 1.5$ V.
3. Calculated from measured f_{MAX} internal
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high-impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high-impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.
6. Equivalent function to t_{PZX}, t_{PXZ} but using product term control.

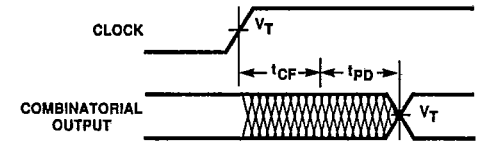
SWITCHING WAVEFORMS



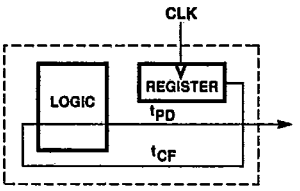
Combinatorial Output

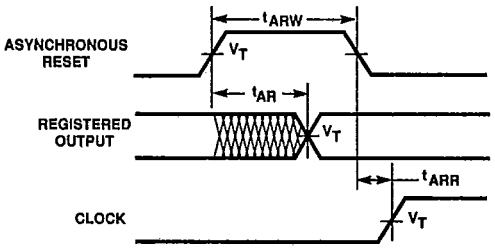


Registered Output

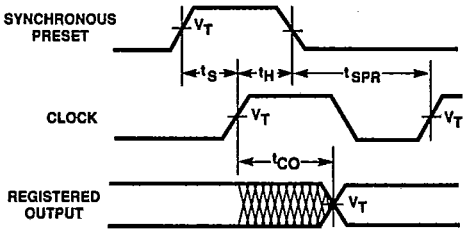


Clock to Feedback to Combinatorial Output(See Path at Right)

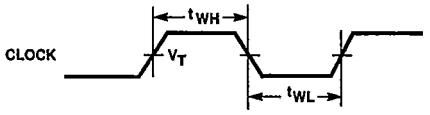




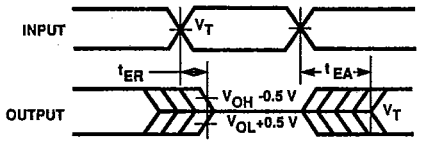
Asynchronous Reset



Synchronous Preset

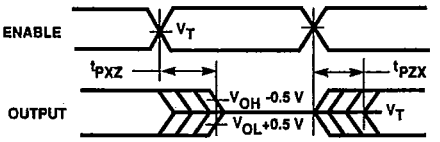


Clock Width



Input to Output Disable/Enable

Notes:
1. VT = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2 - 5 ns typical

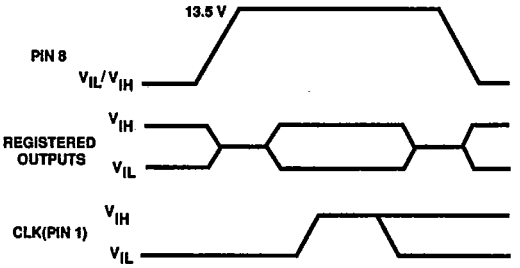


Pin 11 to Output Disable/Enable

OUTPUT REGISTER PRELOAD

The PRELOAD function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is as follows:

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Disable output registers by setting pin 8 to 13.5 V ± 0.5 V.
3. Apply the desired value (V_{IL}/V_{IH}) to all registered output pins. Leave combinatorial outputs floating.
4. Clock pin 1 from V_{IL} to V_{IH}.
5. Remove V_{IL}/V_{IH} from all registered output pins.
6. Lower pin 8 to V_{IL}/V_{IH}.
7. Enable output registers per programmed pattern.
8. Verify for V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.



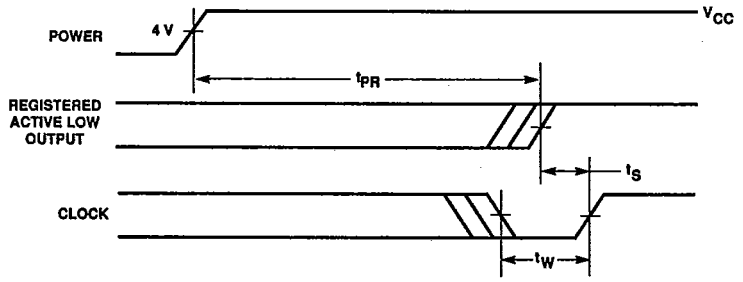
Output Register PRELOAD

POWER-UP RESET

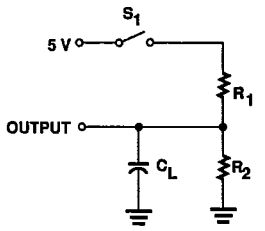
The PALC18U8Q has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_W	Clock Width			



SWITCHING TEST CIRCUIT



Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	560 Ω	1.1 kΩ	1.5 V
t_{PZX}, t_{EA}	Z–>H: open Z–>L: closed	50 pF	560 Ω	1.1 kΩ	1.5 V
t_{PXZ}, t_{ER}	H–>Z: open L–>Z: closed	5 pF	560 Ω	1.1 kΩ	H–>Z: V_{OH} –0.5 V L–>Z: V_{OL} +0.5 V

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

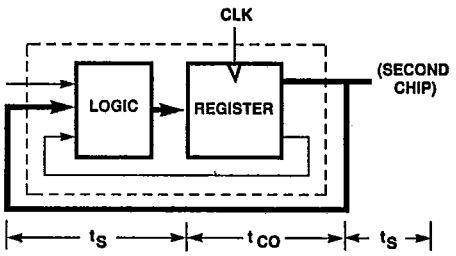
f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

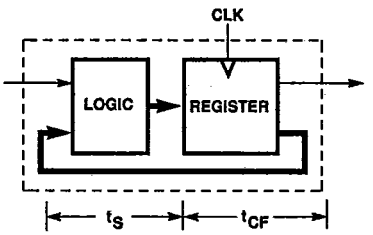
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs ($t_S + t_{CF}$). This f_{MAX} is designated "f_{MAX} internal."

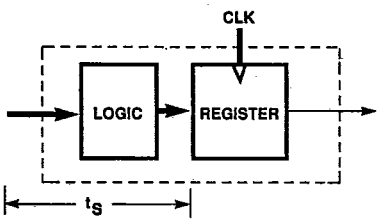
The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."



f_{MAX} External Feedback; $1/(t_S + t_{CO})$



f_{MAX} Internal Feedback; $1/(t_S + t_{CF})$



f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

T-46-13-47

Programmers/Development Systems (Subject to change)

MANUFACTURER	PROGRAMMER CONFIGURATION
Adams MacDonald 2999 Monterey/Salinas Hwy. Monterey, CA 93940 (408) 373-3607	Contact Manufacturer
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	System 29B LogicPak™ 303A-V04 Adapter 303A-011A/B-V5 Family/Pinout Code: DB-2E
Digelec Inc. 1602 Lawrence Ave., Suite 113 Ocean, NJ 07712 (201) 493-2420	Contact Manufacturer
Kontron Electronics Inc. 1230 Charleston Rd. Mountain View, CA 94039-7230 (415) 965-7020	Contact Manufacturer
Logical Devices 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309	Contact Manufacturer
Microprass Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47.90.40	Contact Manufacturer
Stag Microsystems Inc. 1600 Wyatt Dr., Suite 3 Santa Clara, CA 95054 (408) 988-1118	ZL30 Programmer, rev. 30A01 PPZ Programmer Module Zm2200, rev. 18 and later
Storey Systems 3201 N. Hwy 67, Suite E Mesquite, TX 75150 (214) 270-4135	Contact Manufacturer
Structured Design 333 Cobalt Way, Suite 107 Sunnyvale, CA 94086 (408) 988-0725	Contact Manufacturer
Varix Corporation 1210 E. Campbell Rd., Suite 100 Richardson, TX 75081 (214) 437-0777	Contact Manufacturer
MANUFACTURER	**SOFTWARE DEVELOPMENT SYSTEM**
Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94088-3453 (800) 222-9323	PALASM*2 Software, rev. 2.23 and later
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	ABEL 3.0 Software
Personal CAD Systems Assisted Technology Division 1290 Parkmoor Ave. San Jose, CA 95126 (408) 971-1300	CUPL Software

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PALASM 2 SOFTWARE SUPPORT FOR THE PALC18U8Q

About this Section

This section describes PALASM 2 software special considerations for the PALC18U8Q. It is intended as a supplement to the PALASM 2 software user documentation in part 4 of the 1988 PAL Device Data Book. If you do not already have the Data Book, contact your local AMD/MMI sales office for a copy.

1 Boolean Equation Design Entry

PALASM 2 software supports Boolean equation design entry for the PALC18U8Q.

Note: PALASM 2 software does not currently support state machine design entry for the PALC18U8Q. Future versions will include this additional design option.

When creating the design, consider the following items.

1. The three-state function can be controlled in two ways:

   - Using bank enable pin 11 for a registered equation with no three-state equation defined (refer to *Controlling Output Enable With SETF* in Section 6.2.1.2 of the PALASM 2 software documentation).

   - Using an individually programmable three-state function for each output (refer to Functional Equations, Section 4.1.3.4 of the PALASM 2 software documentation for the syntax).

   Note: The default setting for a combinatorial output with no .TRST function defined is V_{cc} (that is, permanently enabled). The default for a registered output with no .TRST function is bank enable.

2. You can create combinatorial or registered outputs by using the = or := operators to define the equations.

3. To use an I/O pin permanently as an input, do not use the pin as an output on the left side of any equation. Use the pin only as an input on the right side of the equation operators that define other outputs.

4. Pin 1 may be used as a clock and as an input for combinatorial outputs in the same design. Do not use the clock pin as an input in registered equations as this will cause timing problems. (See *Simulation* section in this document.)

5. The pin list for the PALC18U8Q defines a buried node at the 21st pin position for global preset or reset product terms. A sample pin list follows.

```
;1   2   3   4   5   6   7   8   9   10   11
I1   I2  I3  I4  I5  I6  I7  I8  I9  GND  I11

;12  13  14  15  16  17  18  19  20  21
O12  O13 O14 O15 O16 O17 O18 O19 VCC GLOBAL
```

Note: The name GLOBAL at position 21 serves only as an example. You can assign any name to this position.

6. The synchronous global preset sets all registers to high. Use the fictional 21st pin in the CHIP statement to define the global preset. Define this function once in the design:

Syntax

21st_Pin.SETF=One_Product_Term

Example

GLOBAL.SETF=I2 * I3

Refer to *Controlling Output Enable With SETF*, Section 6.2.1.2 in the PALASM 2 software documentation to control this function in simulation.

7. The asynchronous global reset sets all registers to low. Use the fictional 21st pin in the CHIP statement to define the global reset. Define this function once in the design:

Syntax

21st_Pin.RSTF=One_Product_Term

Example

GLOBAL.RSTF=I4 * I5

Refer to *Controlling Output Enable With SETF*, Section 6.2.1.2 in the PALASM 2 software documentation to control this function in simulation.

2 Simulation

PALASM 2 software supports simulation for the PALC18U8Q. Refer to the PALASM documentation in part 4 of the Data Book for a complete description of simulation.

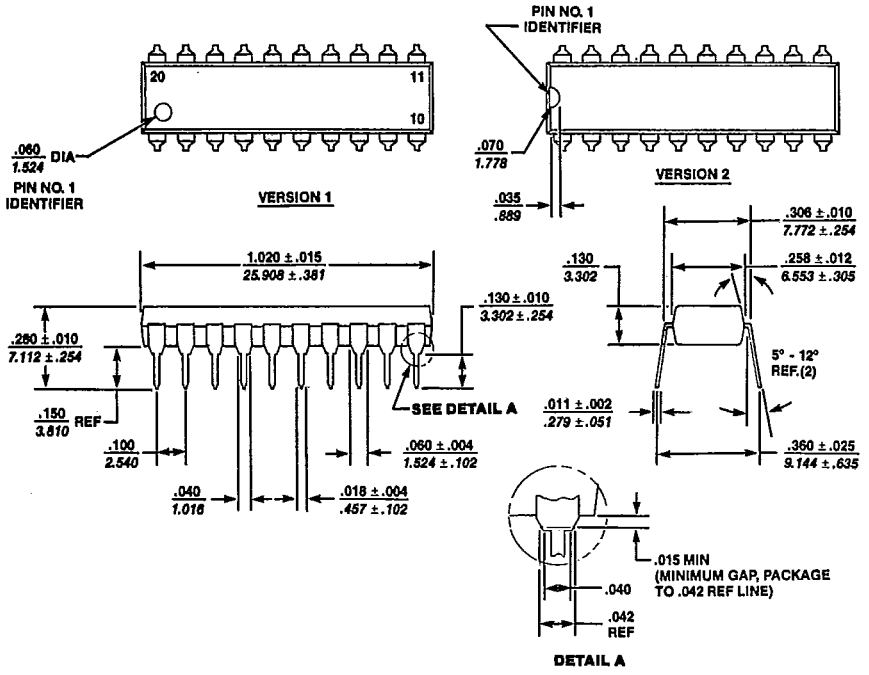
If you use registered equations for the PALC18U8Q, consider the following item.

- If the clock pin is used as an input, you must use SETF to control the clock. If you use the CLOCKF statement to control the clock signal, an error message appears.

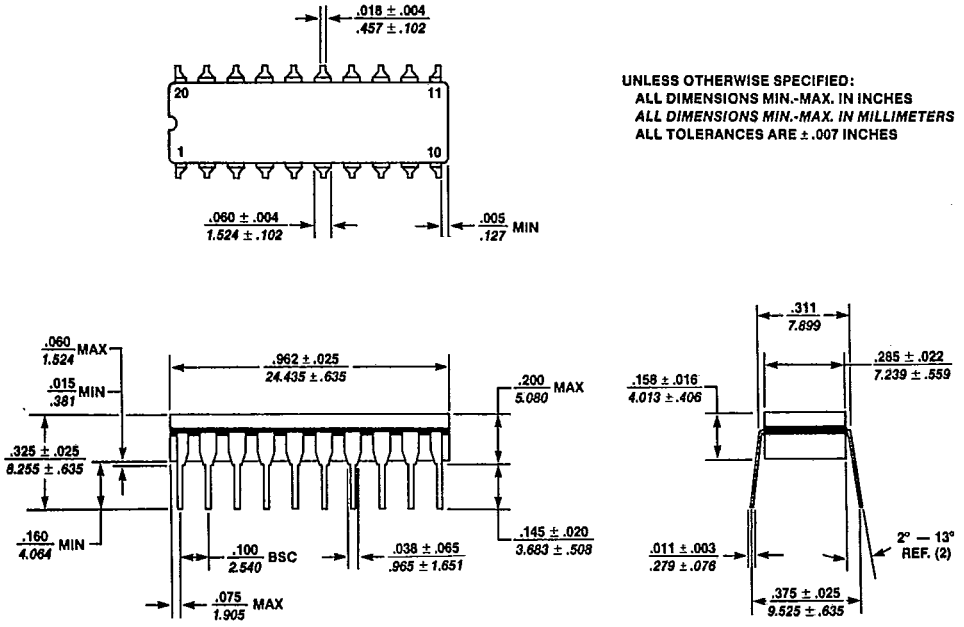
3 Programming

The current version of software (V05) on the Data I/O programmer does not allow the preload simulation feature. Future versions (V06 and later) of Data I/O software are expected to support this feature.

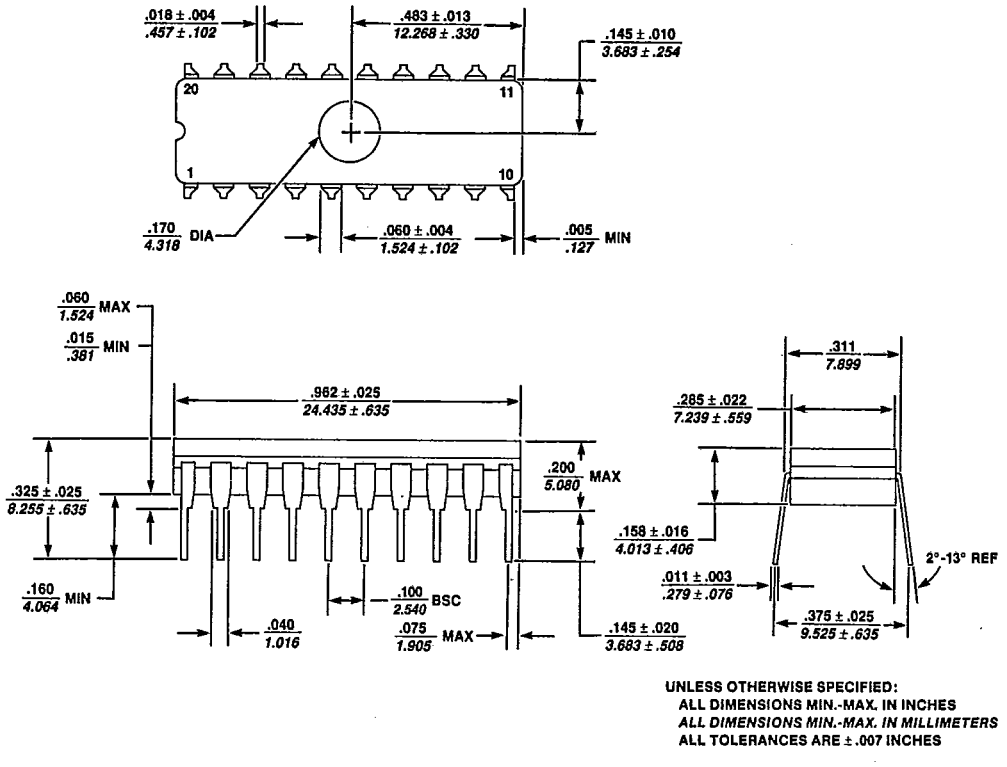
PHYSICAL DIMENSIONS
20N MOLDED DIP



20J CERAMIC DIP

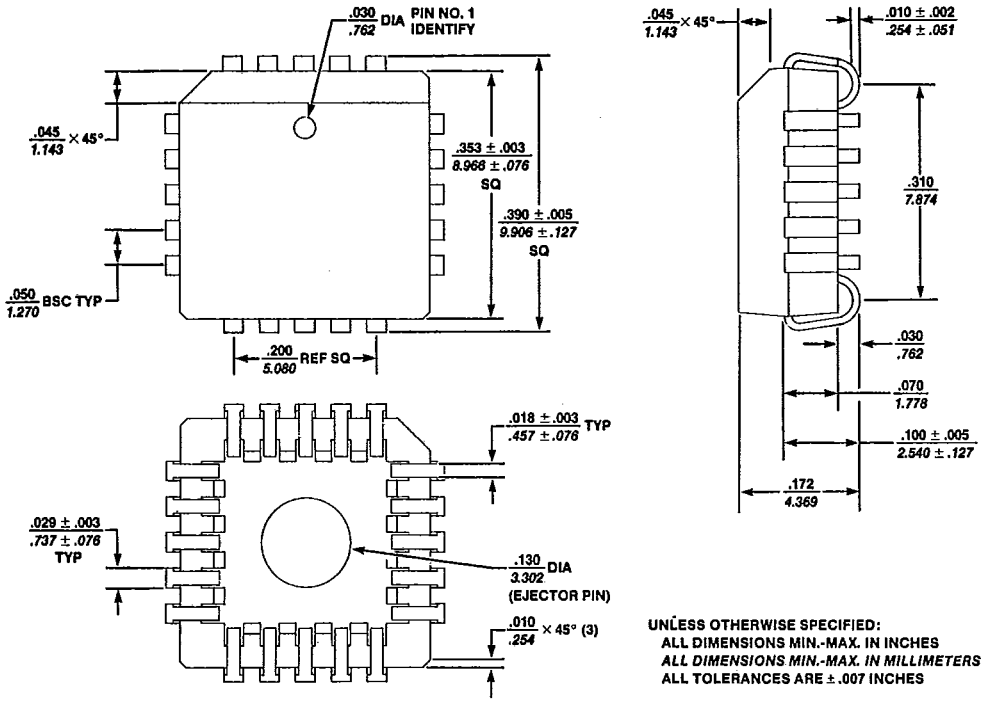


PHYSICAL DIMENSIONS
20Q WINDOW CERDIP



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

PHYSICAL DIMENSIONS
20NL MOLDED CHIP CARRIER
(0.351" X 0.352")



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ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES