

CYPRESS
SEMICONDUCTOR

PRELIMINARY

CY7C375

128-Macrocell Flash PLD

Features

- 128 macrocells in eight logic blocks
- 128 I/O pins
- 6 dedicated inputs including 4 clock pins
- No hidden delays
- High speed
 - $f_{MAX} = 100$ MHz
 - $t_{PD} = 12$ ns
 - $t_S = 9$ ns
 - $t_{CO} = 9$ ns
- Electrically alterable FLASH technology
- Available in 160-pin PQFP and CPGA packages

Functional Description

The CY7C375 is a Flash Erasable Programmable Logic Device (EPLD) and is part of the FLASH370 family of high-density, high-speed PLDs. Like all members of the FLASH370 family, the CY7C375 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 128 macrocells in the CY7C375 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

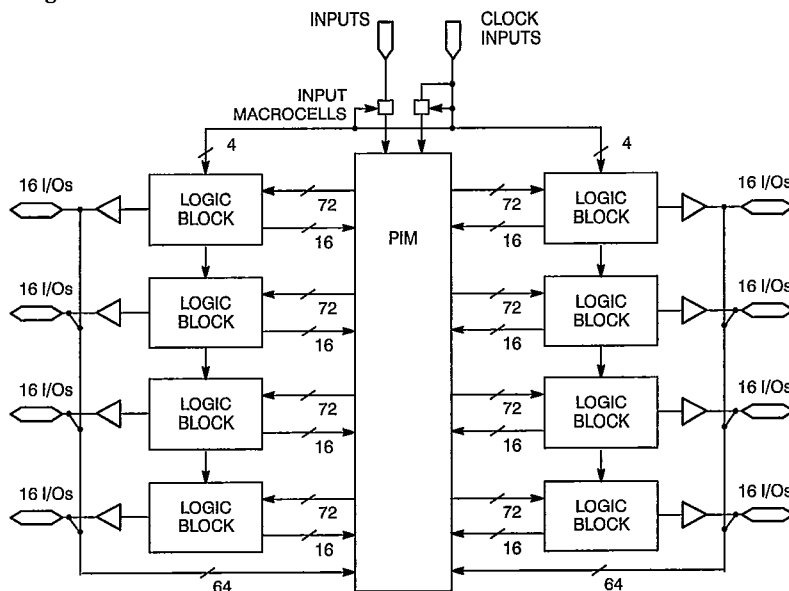
The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix

(PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C375 is rich in I/O resources. Every macrocell in the device features an associated I/O pin, resulting in 128 I/O pins on the CY7C375. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C375 features a very simple timing model. Unlike other high-density PLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C375 remain the same.

Logic Block Diagram



Selection Guide

		7C375-100	7C375-83	7C375-66
Maximum Propagation Delay (ns)		12	15	20
Maximum Standby Current, I_{CC1} (mA)	Commercial	300	300	300
	Military		370	370
Maximum Operating Current, I_{CC2} (mA)	Commercial	330	330	330
	Military		400	400

Shaded area contains advanced information.



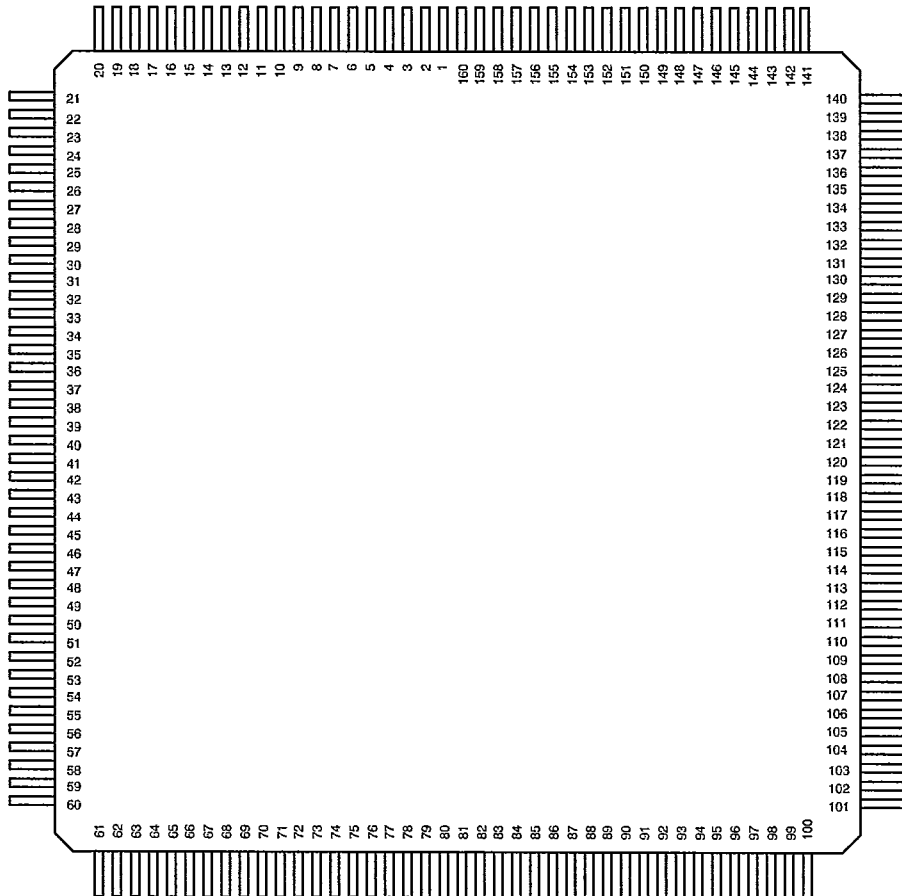
PRELIMINARY

CY7C375

Pin Configuration

Ceramic Quad Flatpack (CQFP)

Top View

4
PLDs

7C375-2



Functional Description (continued)

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C375 includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72x86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 PLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C375 has a separate I/O pin associated with it. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and four global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C375 to the inputs and to each other. All

inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Development Tools

Development software for the CY7C375 is available from Cypress's *Warp2™* and *Warp3™* software packages. Both of these products are based on the IEEE standard VHDL language. Cypress also supports third-party vendors such as ABEL™, CUPL™, and LOG/IC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to +150°C
Ambient Temperature with	
Power Applied	- 55°C to +125°C
Supply Voltage to Ground Potential	- 0.5V to +7.0V
DC Voltage Applied to Outputs	
in High Z State	- 0.5V to +7.0V
DC Input Voltage	- 0.5V to +7.0V
DC Program Voltage	12.5V
Output Current into Outputs	16 mA
Static Discharge Voltage	>2001V
(per MIL-STD-883, Method 3015)	
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 5%
Military ^[1]	- 55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.



PRELIMINARY

CY7C375

Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions	7C375		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	2.4		V
					V
V _{OL}	Output LOW Voltage	V _{CC} = Min.		0.5	V
					V
V _{IH}	Input HIGH Voltage		2.0	7.0	V
V _{IL}	Input LOW Voltage		-0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-50	+50	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = 0.5V	-30	-90	mA
I _{CC1}	Power Supply Current (Standby)	V _{CC} = Max., I _{OUT} = 0 mA, f = 0 mHz, V _{IN} = GND, V _{CC}	Com'l	300	mA
			Mil	370	
I _{CC2}	Power Supply Current	V _I = V _{CC} or GND, f = 40 MHz	Com'l	330	mA
			Mil	400	

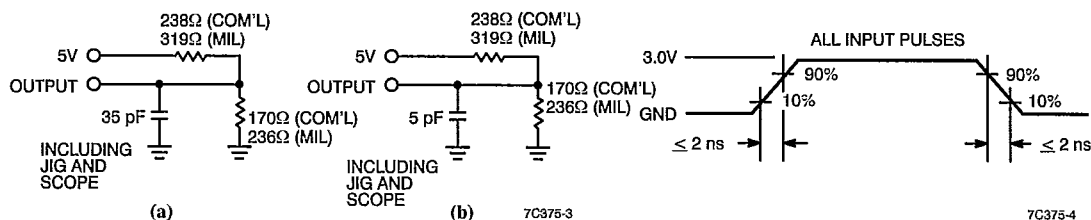
Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0V at f = 1 MHz	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0V at f = 1 MHz	12	pF

Notes:

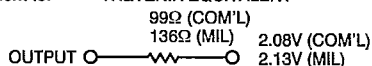
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to:

THÉVENIN EQUIVALENT





PRELIMINARY

CY7C375

Switching Characteristics Over the Operating Range^[5]

Parameter	Description	7C375–100		7C375–83		7C375–66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters								
t _{PD}	Input to Combinatorial Output		12		15		20	ns
t _{PDL}	Input to Output Through Transparent Input or Output Latch		14		17		22	ns
t _{PDLL}	Input to Output Through Transparent Input and Output Latches		16		19		24	ns
t _{EA}	Input to Output Enable		16		19		24	ns
t _{ER}	Input to Output Disable		16		19		24	ns
Input Registered/Latched Mode Parameters								
t _{WL}	Clock or Latch Enable Input LOW Time	5		6		8		ns
t _{WH}	Clock or Latch Enable Input HIGH Time	5		6		8		ns
t _{IS}	Input Register or Latch Set-Up Time	2		3		4		ns
t _{IH}	Input Register or Latch Hold Time	2		3		4		ns
t _{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		16		19		24	ns
t _{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		18		21		26	ns
f _{MAX1}	Maximum Frequency of (2) CY7C375s in Input Registered Mode (Lesser of 1/(t _{ICO} + t _{IS}) and 1/(t _{WL} + t _{WH}))	55.5		45.5		35.7		MHz
f _{MAX2}	Maximum Frequency Data Path in Input Registered/Latched Mode (Least of 1/t _{ICO} , 1/(t _{WL} + t _{WH}), 1/(t _{IS} + t _{IH}))	62.5		52.6		41.7		MHz
Output Registered/Latched Mode Parameters								
t _{CO}	Clock or Latch Enable to Output		9		12		15	ns
t _S	Set-Up Time from Input to Clock or Latch Enable	9		12		15		ns
t _H	Register or Latch Data Hold Time	0		0		0		ns
t _{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		16		19		24	ns
t _{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	10		12		15		ns
t _{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	12		15		20		ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		ns
f _{MAX3}	Maximum Frequency of (2) CY7C375s in Output Registered Mode (Lesser of 1/(t _{CO} + t _S) and 1/(t _{WL} + t _{WH}))	55.5		41.7		33.3		MHz
f _{MAX4}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of 1/(t _{WL} + t _{WH}), 1/(t _S + t _H), or 1/t _{CO})	100		83.3		62.5		MHz
f _{MAX5}	Maximum Frequency with Internal Feedback in Output Registered Mode (Least of 1/t _{SCS} , 1/(t _S + t _H), or 1/t _{CO}) ^[4]	100		83		66		MHz
Pipelined Mode Parameters								
t _{ICS}	Input Register Clock to Output Register Clock	12		15		20		ns
f _{MAX6}	Maximum Frequency in Pipelined Mode (Least of 1/(t _{CO} + t _{IS}), 1/t _{ICS} , 1/(t _{WL} + t _{WH}), 1/(t _S + t _{IH}), or 1/t _{SCS})	83.3		66.6		50.0		MHz

Shaded area contains advanced information.

Note:

5. All AC parameters are measured with 16 outputs switching.



PRELIMINARY

CY7C375

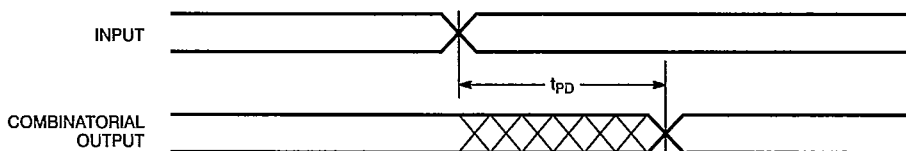
Switching Characteristics Over the Operating Range^[5] (continued)

Parameter	Description	7C375-100		7C375-83		7C375-66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Preset Parameters								
t _{rw}	Asynchronous Reset Width	12		15		20		ns
t _{rr}	Asynchronous Reset Recovery Time	14		17		22		ns
t _{ro}	Asynchronous Reset to Output		18		21		26	ns
t _{pw}	Asynchronous Preset Width	12		15		20		ns
t _{pr}	Asynchronous Preset Recovery Time	14		17		22		ns
t _{po}	Asynchronous Preset to Output		18		21		26	ns

Shaded area contains advanced information.

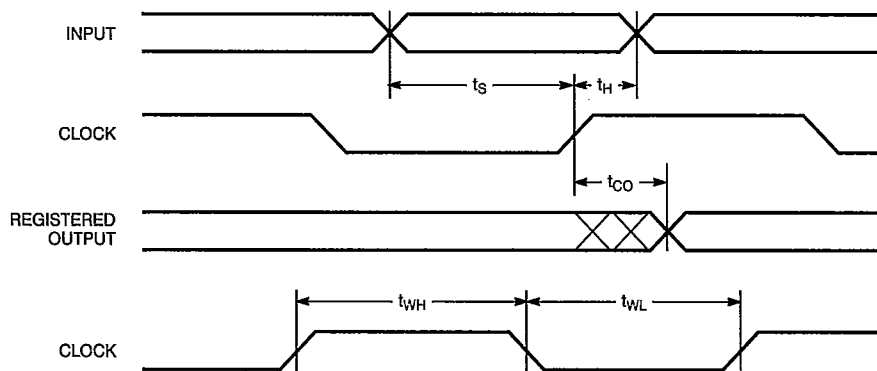
Switching Waveforms

Combinatorial Output



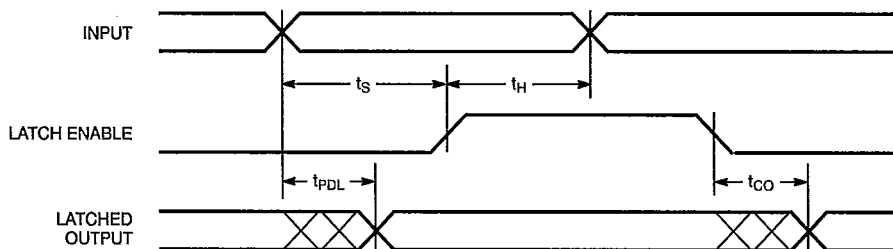
7C375-5

Registered Output



7C375-6

Latched Output



7C375-7

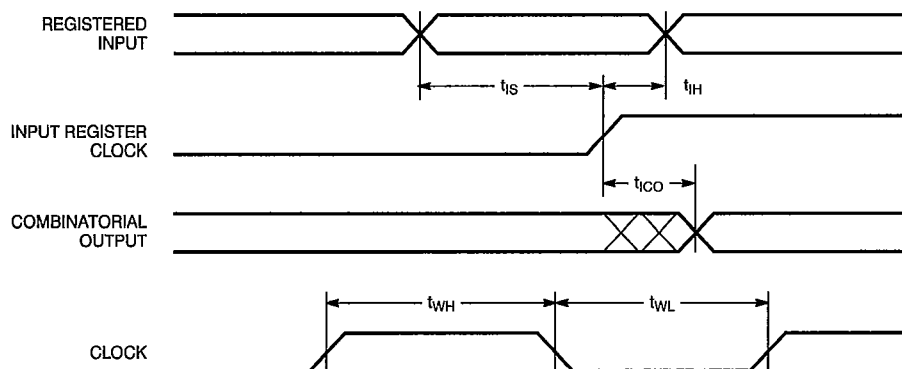


PRELIMINARY

CY7C375

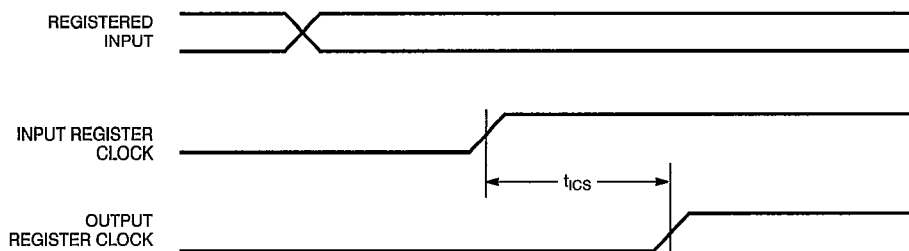
Switching Waveforms (continued)

Registered Input



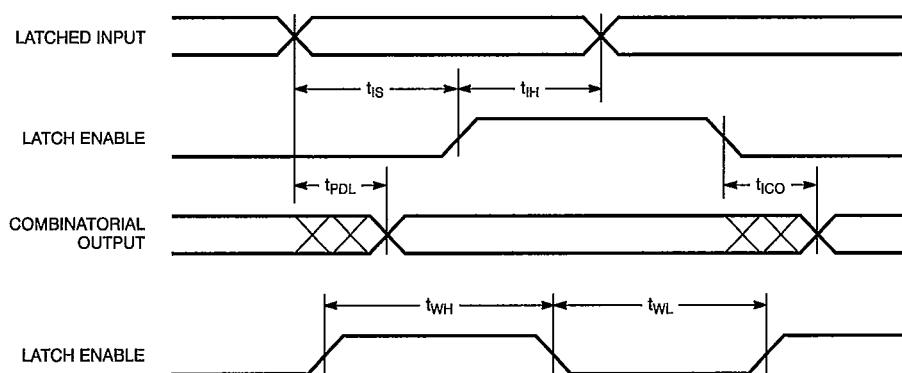
7C375-8

Input Clock to Output Clock



7C375-9

Latched Input



7C375-10

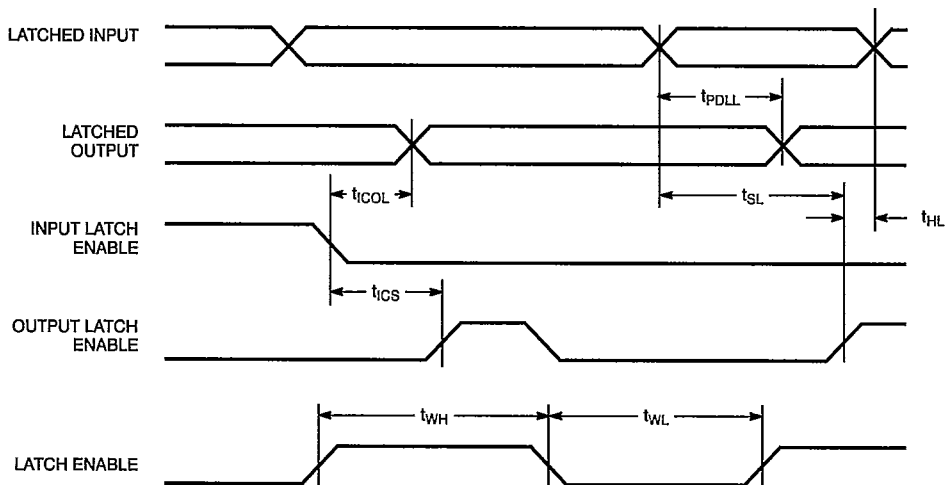


PRELIMINARY

CY7C375

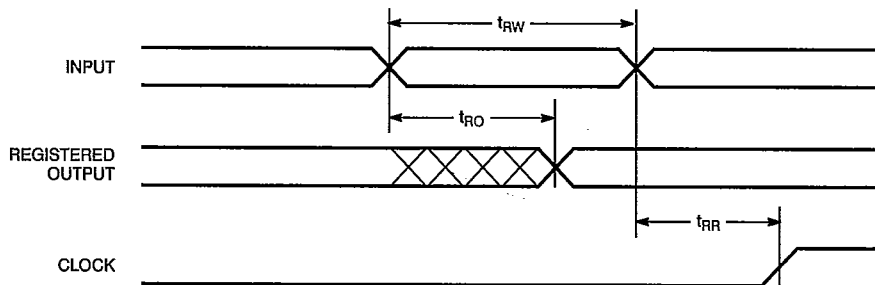
Switching Waveforms (continued)

Latched Input and Output



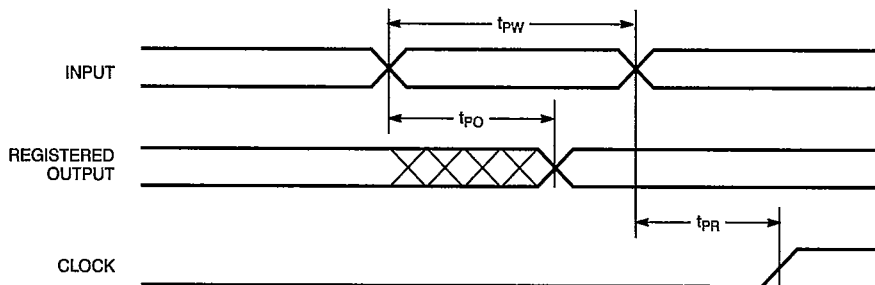
7C375-11

Asynchronous Reset



7C375-12

Asynchronous Preset



7C375-13

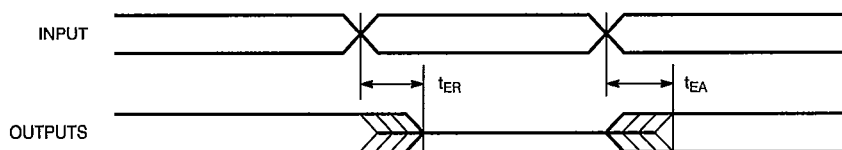


PRELIMINARY

CY7C375

Switching Waveforms (continued)

Output Enable/Disable



7C375-14

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
100	CY7C375-100NC	N160	160-Lead PQFP	Commercial
83	CY7C375-83NC	N160	160-Lead PQFP	Commercial
	CY7C375-83GMB	G160	160-Pin PGA	Military
66	CY7C375-66NC	N160	160-Lead PQFP	Commercial
	CY7C375-66GMB	G160	160-Pin PGA	Military

Shaded areas contain advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{PDL}	7, 8, 9, 10, 11
t_{PDLL}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{ICOL}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_{SL}	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11
t_{HL}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{ICS}	7, 8, 9, 10, 11
t_{EA}	7, 8, 9, 10, 11
t_{ER}	7, 8, 9, 10, 11