

54AC11190, 74AC11190 SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS

TIO170—D3461, MARCH 1990

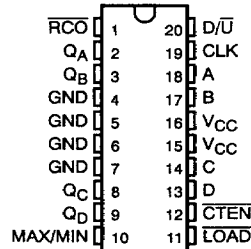
- Single Down/Up Count Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presetable with Load Control
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

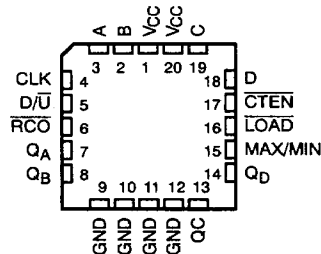
The 'AC11190 is a synchronous, 4-bit decade reversible up/down counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high transition of the clock input if the enable input ($\overline{CTEN}$) is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up ($D/\overline{U}$) input. When the $D/\overline{U}$ input is low, the counter counts up. When the $D/\overline{U}$ input is high, the counter counts down.

54AC11190 ... J PACKAGE
74AC11190 ... DW OR N PACKAGE
(TOP VIEW)



54AC11190 ... FK PACKAGE
(TOP VIEW)



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description (continued)

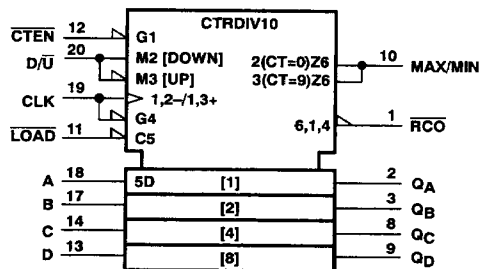
These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/U) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, they may be preset to any number between 0 and 9 by placing a low on the load input and entering the desired data at the data inputs. The outputs change to agree with the data inputs independently of the level of the clock input. This feature allows the counter to be used as modulo-N dividers by modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple-clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9) counting up. The ripple-clock output ($\overline{RCO}$) produces a low-level output pulse under those same conditions but only while the clock input is low. The counter can be cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The 54AC11190 is characterized for operation over the full military temperature range of -55°C to 125°C . The 74AC11190 is characterized for operation from -40°C to 85°C .

logic symbol†



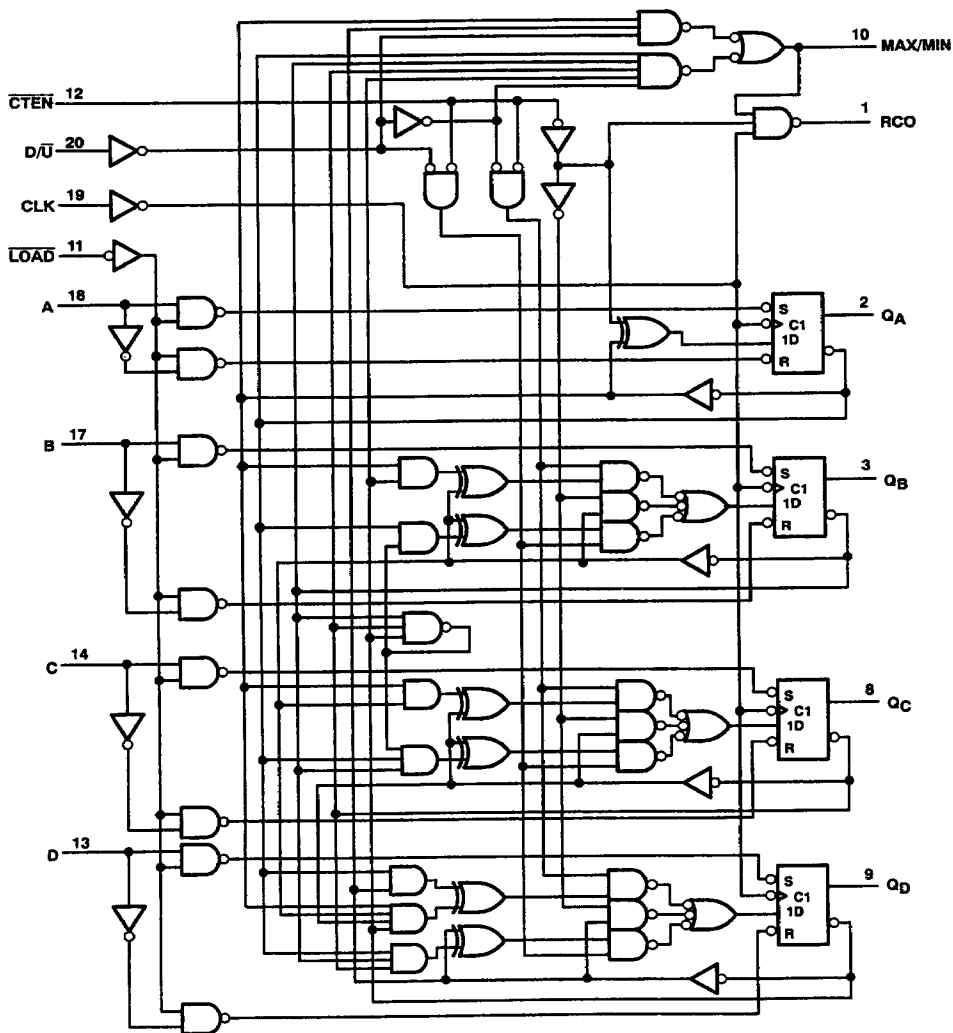
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

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logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

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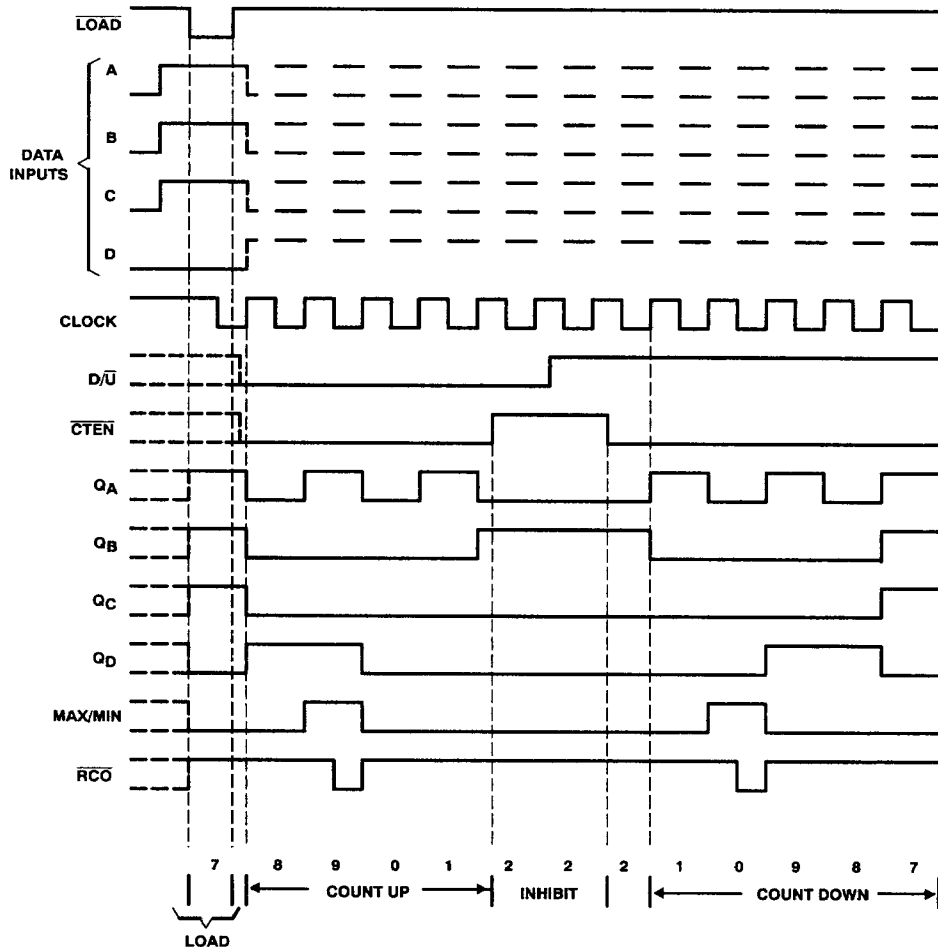
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timing diagram (typical load, count, and inhibit sequences)

This timing diagram illustrates the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±150 mA
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11190			74AC11190			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 3 V	2.1			2.1			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 5.5 V	3.85			3.85			
V _{IL}	Low-level input voltage	V _{CC} = 3 V				0.9			V
		V _{CC} = 4.5 V	1.35			1.35			
		V _{CC} = 5.5 V	1.65			1.65			
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 3 V				−4			mA
		V _{CC} = 4.5 V	−24			−24			
		V _{CC} = 5.5 V	−24			−24			
I _{OL}	Low-level output current	V _{CC} = 3 V	12			12			mA
		V _{CC} = 4.5 V	24			24			
		V _{CC} = 5.5 V	24			24			
Δt/Δv	Input transition rise or fall rate		0		10	0		10	ns/V
T _A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54AC11190		74AC11190		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I _{OH} = -50 mA†	5.5 V				3.85				
V _{OL}	I _{OL} = 50 µA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I _{OL} = 12 mA	3 V			0.36		0.5		0.44	
		4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I _{OL} = 50 mA†	5.5 V				1.65				
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	160		80		µA
		5 V		4						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 1 MHz	66	pF

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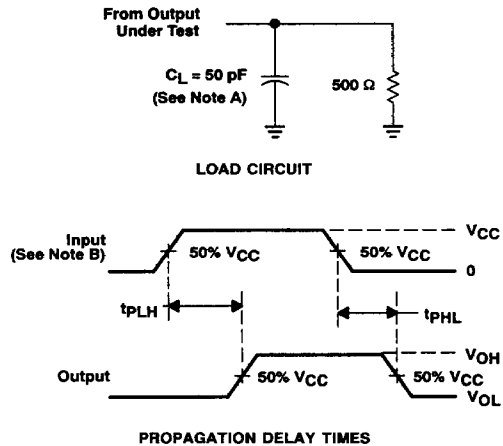
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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