TFT LCD Preliminary Specification

MODEL NO.: V420H1 - L01

LCD TV Head Division

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 0.1	Mar. 23,'05	All	All	Preliminary Specification was first issued.
Ver 0.2	Mar. 30,'05	26	7.2	Delete Original Note (3). Drive Signal of LCD Panel graph Update Note (3). Definition of Gray to Gray Switching Time graph
		35		Update Mechanical Characteristics: Screw: M4 (Pitch 0.7/Machine) Torque: 4~5kgf.cm
Ver1.1	May. 20,'05	7	3.1	Electrical Characteristics-3.1 TFT LCD Module: Ripple Voltage: Max.:350 Rush Current: Typ.3.5
		9		3.2 Backlight Unit: Lamp Life Time Min. Value: 50,000 Total Power Consumption Typ.:186 (5), I_L = 5.0mA Auxiliary Power Supply Current Max.:330 Input Ripple Noise Max. : 2.5 V_{BL}=114V
		16	5.4	Inverter Unit: CN3 (Header): S10B-PH-SM3-TB (D)(LF)(JST) or equivalent. Pin No.6 Description: GND CN28-CN31 (Header): AL7204-A0G1Z(PTWO)
		25	7.2	Updated Optical Specifications: Color Chromaticity and Color Gamut Min. & Max. data
Ver1.2	Jul.27.'05	9	3.2	Backlight Unit: CCFL Characteristics Lamp Input Voltage: I_L = 4.7 mA Lamp Current: Min.4.2; Typ.4.7; Max.5.2 Inverter Characteristics Total Power Consumption: Typ.171; I_L = 4.7mA Power Supply Current: typ.1.38 Auxiliary Power Supply Current: Max.280
		11	3.2.2	Note(4) I_L = 4.2 ~ 5.2 mArms.
		25	7.1	Optical Characteristics: Lamp Current: Value 4.7±0.5
Ver1.3	Aug.31.05	4	1.2	High brightness (550 nits)
			1.5	Weight Min(11000) Typ.(11200) Max.(11400)
		9	3.2.2	Total Power Consumption (Typ.) 172 Power Supply Current (Typ.) 1.4 The sum of P_{BL} and P_{Aux}
		25	7.2	Updated Optical Specifications: Color Chromaticity data and Color Gamut Min. data.
		33-35	11	Update Mechanical Characteristic

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V420H1- L01 is a 42" TFT Liquid Crystal Display module with 24-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- Ultra wide viewing angle – Super MVA technology
- High brightness (550 nits)
- High contrast ratio (1000:1)
- Fast response time (8 ms)
- High color saturation (NTSC 75%)
- HD (1920 x 1080 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- 180 degree rotation display option
- Optimized response time for 50 / 60 Hz frame rate

1.3 APPLICATION

- TFT LCD TVs

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	930.24(H) x 523.26 (V) (42.02" diagonal)	mm	(1)
Bezel Opening Area	938.3 (H) x 531.3 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1615 (H) x 0.4845 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-reflective coating Hard coating (3H) Reflection rate : < 2%	-	-

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

1.5 MECHANICAL SPECIFICATIONS

Item			Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)		982.3	983	984	mm	Note (1)
	Vertical(V)		575.3	576	577	mm	
	Depth(D)	W/PCB-Cover	43.1	43.8	44.8	mm	
		W/I INV	52.3	53	54	mm	-
Weight			11000	11200	11400	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	(50)	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

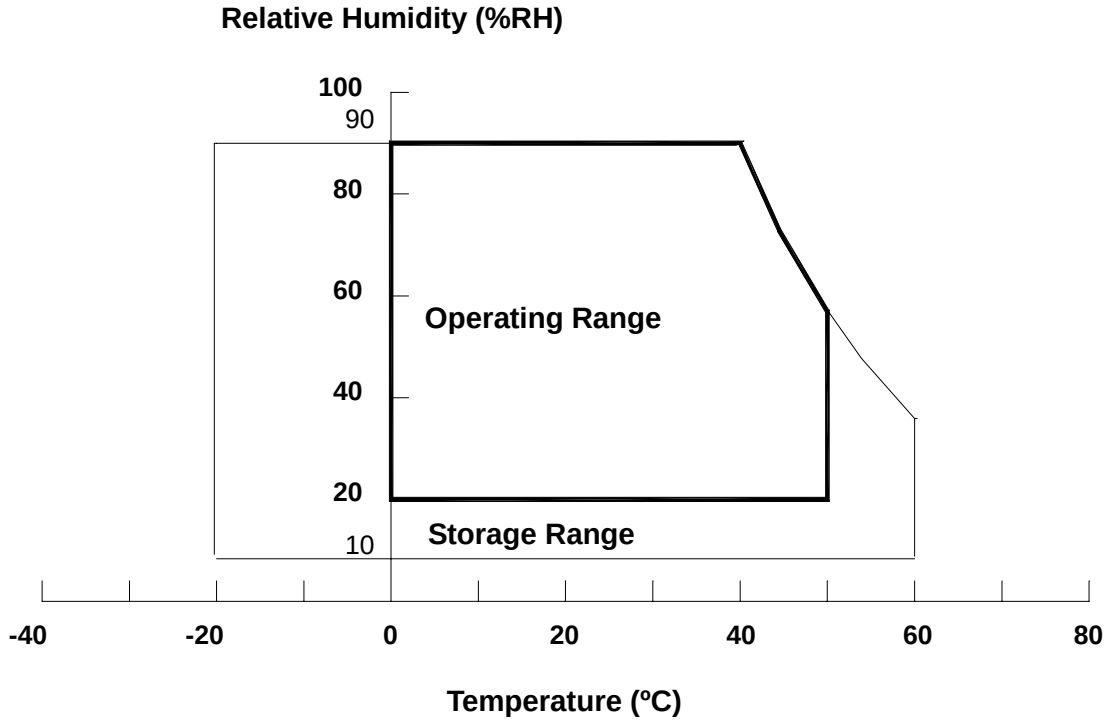
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 60 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	20	V	(1)
Logic Input Voltage	V_{IN}	-0.3	(3.6)	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	-	3000	V_{RMS}	-
Power Supply Voltage	V_{BL}	0	140	V	(1)
Auxiliary Power Supply Voltage	V_{AUX}	0	23	V	(1)
Control Signal Level	-	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

3. ELECTRICAL CHARACTERISTICS

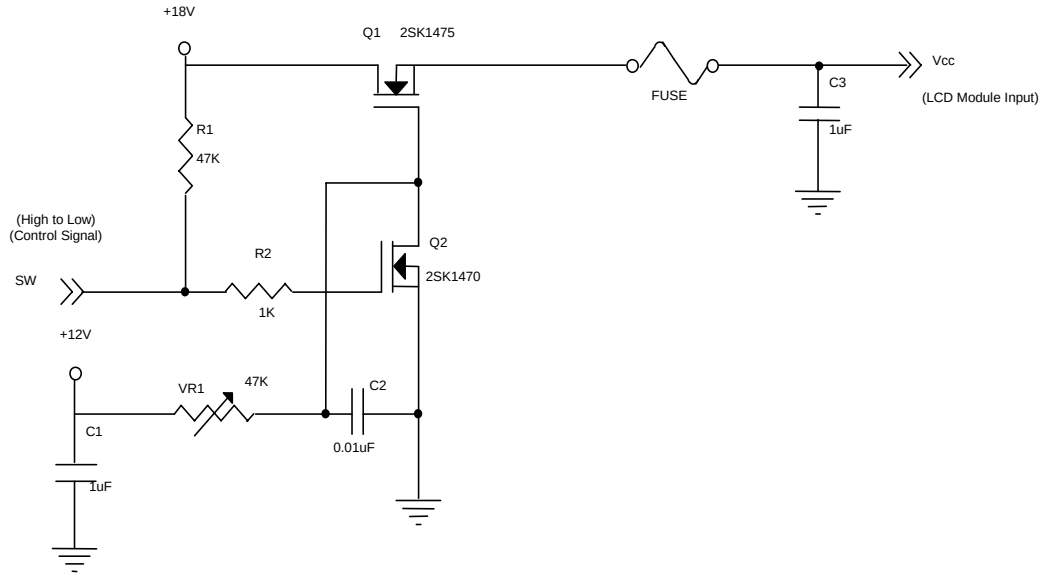
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

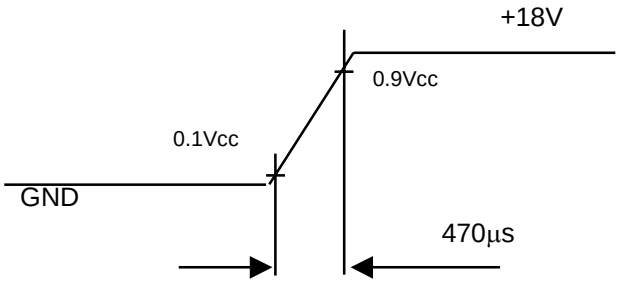
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	16.2	18	19.8	V	(1)
Ripple Voltage		V_{RP}	-	-	350	mV	-
Rush Current		I_{RUSH}	-	3.5	-	A	(2)
Power Supply Current	White	Icc	-	0.75	-	A	(3)a
	Black		-	0.30	-	A	(3)b
	Vertical Stripe		-	0.55	-	A	(3)c
LVDS differential input high threshold voltage		V_{TH}	-	-	+100	mV	
LVDS differential input low threshold voltage		V_{TL}	-100	-	-	mV	
LVDS common input voltage		Vic	1.125	1.25	1.375	V	
Terminating Resistor		RT	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

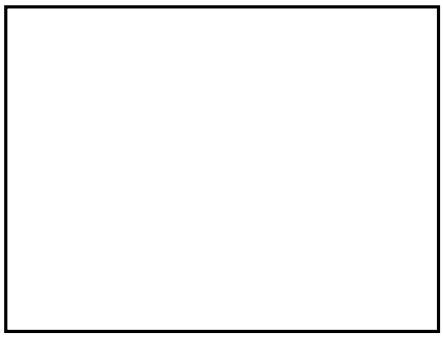


Vcc rising time is 470μs



Note (3) The specified power supply current is under the conditions at Vcc = 18 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

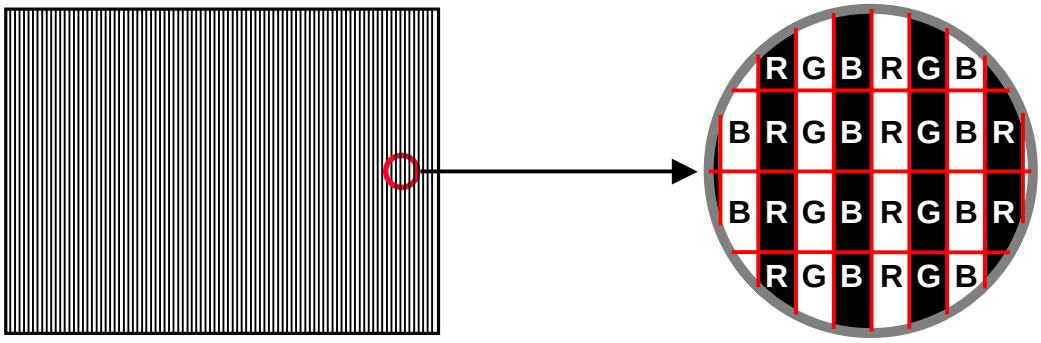
a. White Pattern



Active Area

b. Black Pattern

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

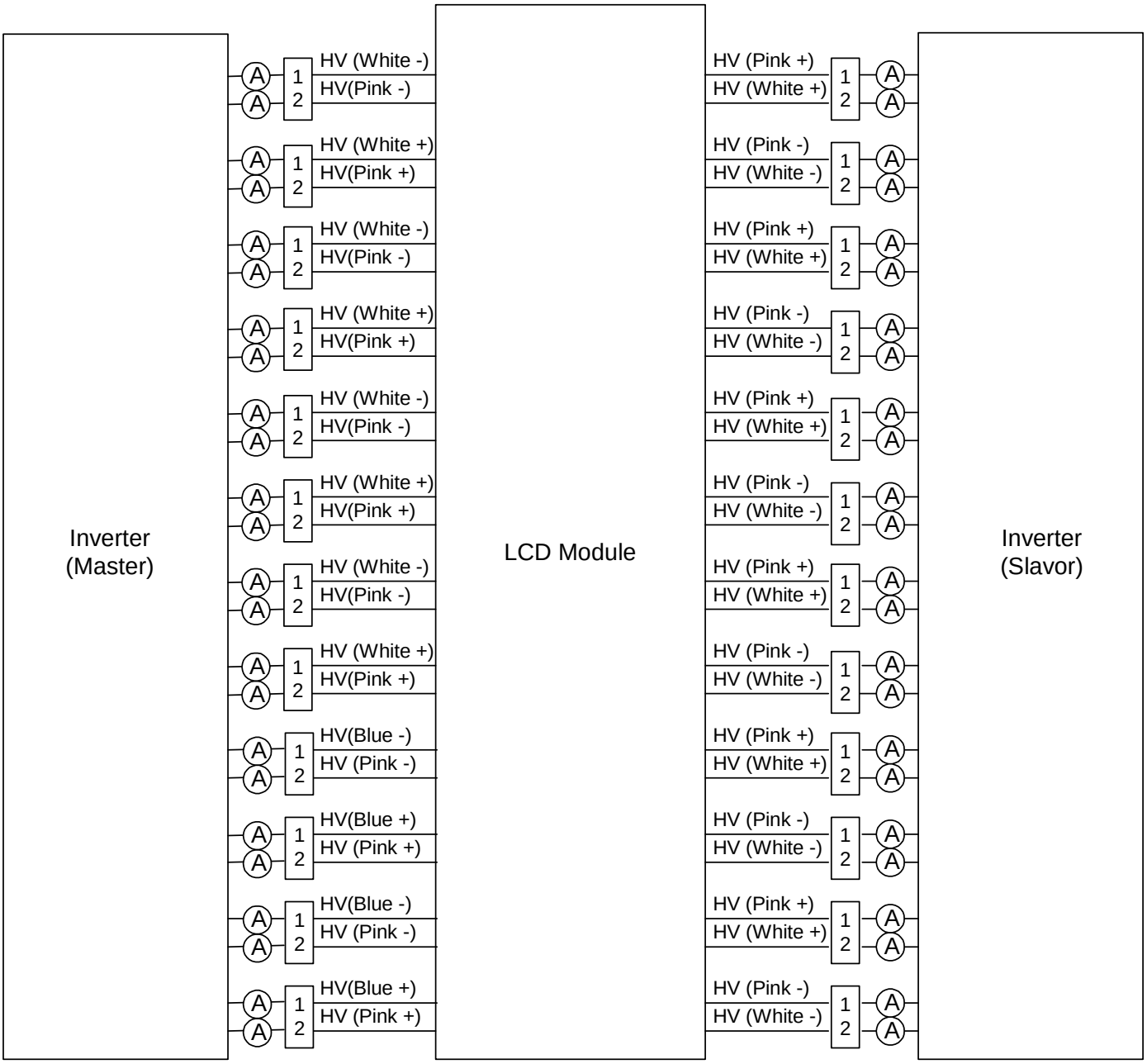
3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	---	1390	---	V_{RMS}	I_L = 4.7 mA
Lamp Current	I_L	4.2	4.7	5.2	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	2055	V_{RMS}	(2), Ta = 0 ºC
		-	-	1740	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_L	40	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Power Consumption	P_{TOL}	-	172	-	W	(5), I_L = 4.7mA The sum of P_{BL} and P_{Aux}
Power Supply Voltage	V_{BL}	114	120	126	V_{DC}	-
Power Supply Current	I_{BL}	-	1.4	-	A	Non Dimming
Auxiliary Power Supply Voltage	V_{AUX}	17	18	19	V_{DC}	-
Auxiliary Power Supply Current	I_{AUX}	-	-	280	mA	-
Input Ripple Noise	-	-	-	2.5	V_{P-P}	V_{BL}=114V
Backlight Turn on Voltage	V_{BS}	2055	-	-	V_{RMS}	Ta = 0 ºC
		1740	-	-	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	47	50	53	kHz	-
Dimming frequency	F_B	150	160	170	Hz	-
Minimum Duty Ratio	D_{MIN}	-	20	-	%	-

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25±2ºC

and I_L = 4.2 ~ 5.2 mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

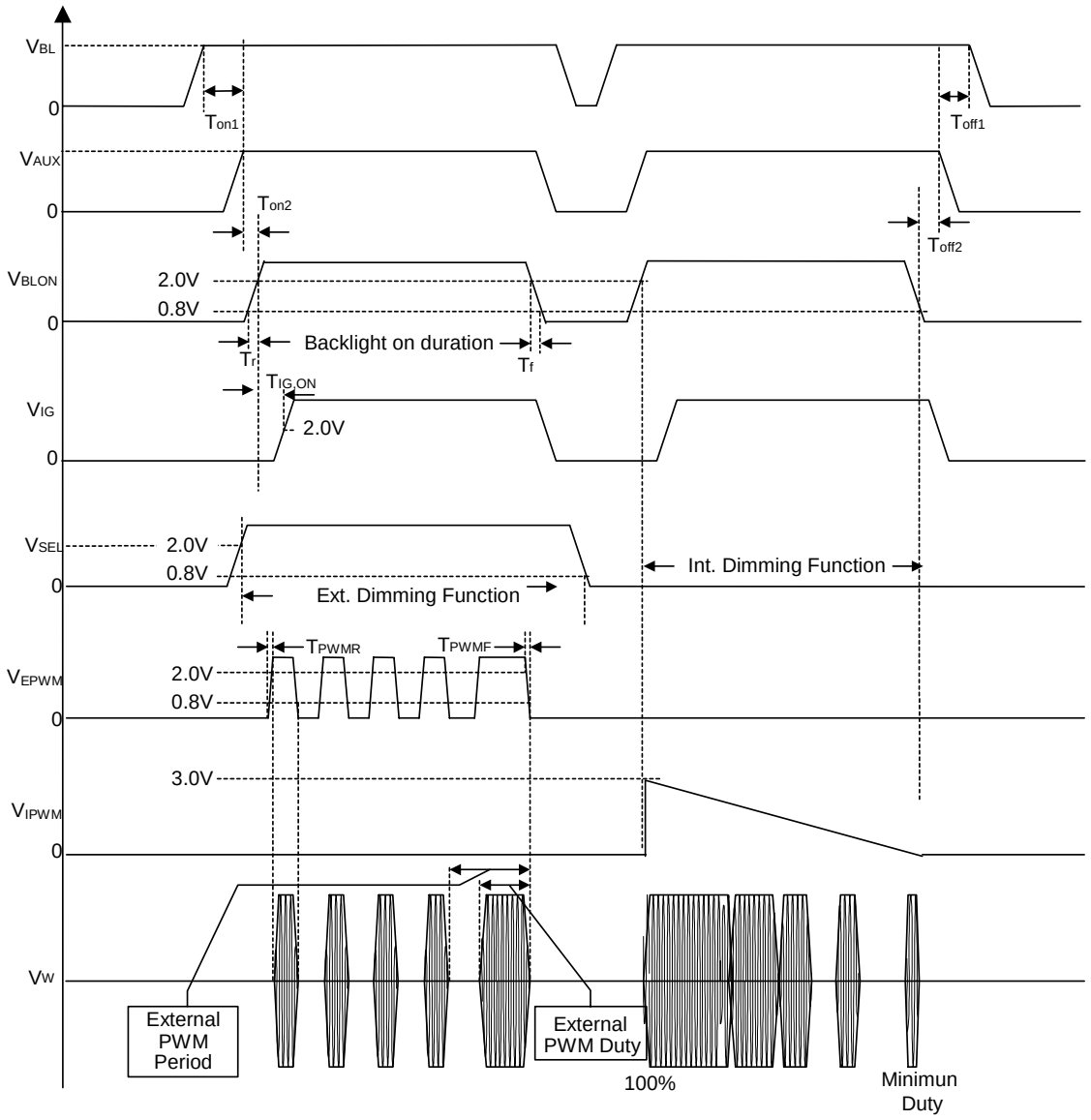
3.2.3 INVERTER INTERTFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
Inverter Good Signal	HI	V_{IG}	V_{IG} = High	2.0	-	5.0	V	Normal Output Voltage
	LO		V_{IG} =Low	0	-	0.8	V	Abnormal Output Voltage
On/Off Control Voltage	ON	V_{BLON}	-	2.0	-	5.0	V	
	OFF		-	0	-	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	-	2.0	-	5.0	V	
	LO		-	0	-	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	-	-	3.0	V	maximum duty ratio
	MIN			-	0	-	V	minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	-	5.0	V	duty on
	LO			0	-	0.8	V	duty off
Control Signal Rising Time		Tr	-	-	-	100	ms	
Control Signal Falling Time		Tf	-	-	-	100	ms	
PWM Signal Rising Time		T_{PWMR}	-	-	-	50	us	
PWM Signal Falling Time		T_{PWMF}	-	-	-	50	us	
Input impedance		R_{IN}	-	1	-	-	MΩ	
BLON Delay Time1		T_{on1}	-	1	-	-	ms	
BLON Off Time1		T_{off1}	-	1	-	-	ms	
BLON Delay Time2		T_{on2}	-	1	-	-	ms	
BLON Off Time2		T_{off2}	-	1	-	-	ms	
Inverter Good Signal Delay Time		$T_{IG,on}$	-	-	-	3	sec	

Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

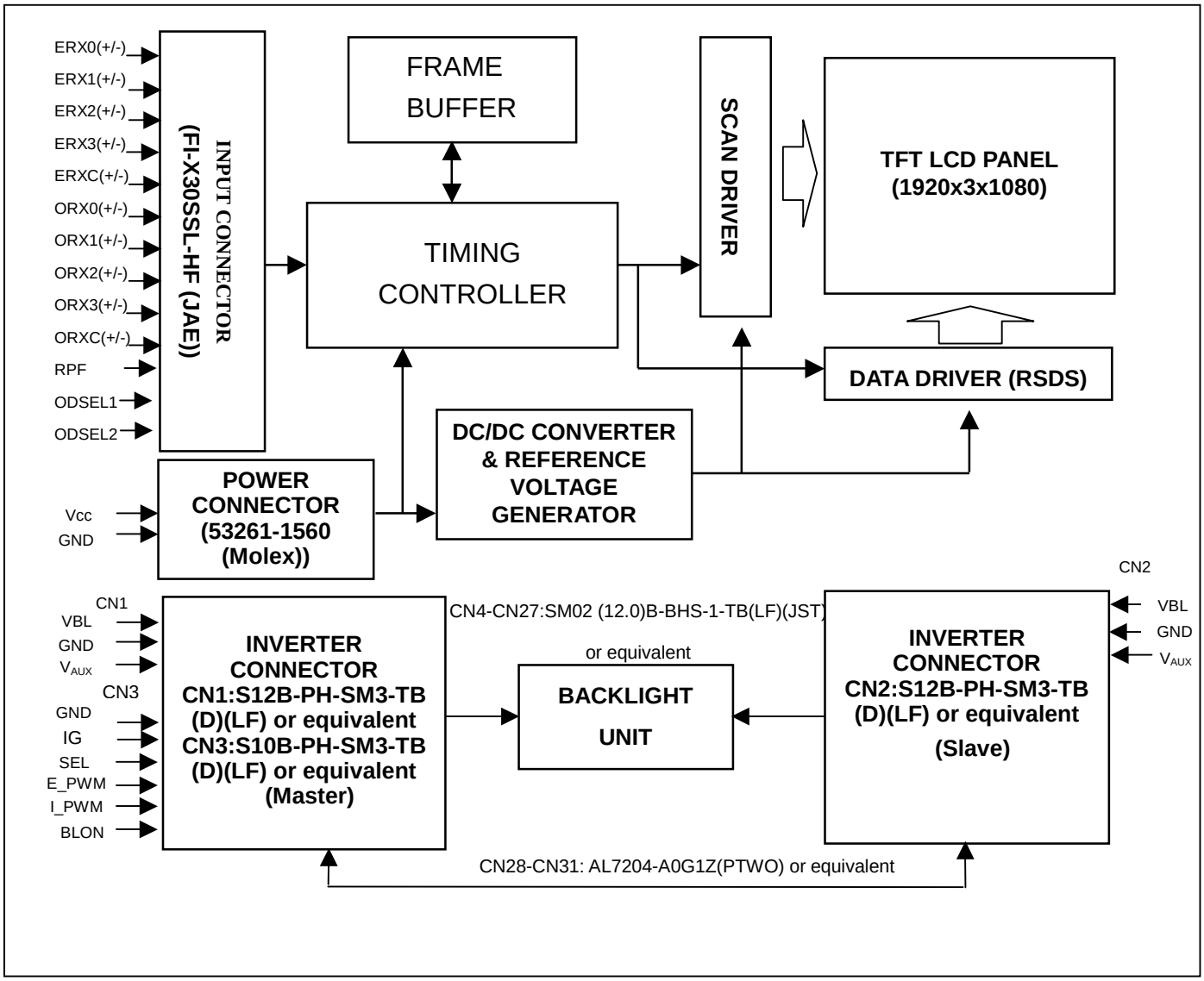
Note (2) The power sequence and control signal timing are shown in the following figure.

Note (3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. V420H1-L01 LCD INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE SIGNAL INPUT

CNF1 Connector Pin Assignment (1)

Pin	Name	Description	Note
1	NC	No Connection	(4)
2	RPF	Display Rotation	(3)
3	NC	No Connection	(4)
4	NC	No Connection	
5	NC	No Connection	
6	ODSEL1	Overdrive Lookup Table Selection	(5)
7	ODSEL2	Overdrive Lookup Table Selection	
8	GND	Ground	
9	ERX0-	Even pixel, negative LVDS differential data input, channel 0	
10	ERX0+	Even pixel, positive LVDS differential data input, channel 0	
11	ERX1-	Even pixel, negative LVDS differential data input, channel 1	
12	ERX1+	Even pixel, positive LVDS differential data input, channel 1	
13	ERX2-	Even pixel, negative LVDS differential data input, channel 2	
14	ERX2+	Even pixel, positive LVDS differential data input, channel 2	
15	ECLK-	Even pixel, negative LVDS differential clock input	
16	ECLK+	Even pixel, positive LVDS differential clock input	
17	ERX3-	Even pixel, negative LVDS differential data input, channel 3	
18	ERX3+	Even pixel, positive LVDS differential data input, channel 3	
19	GND	Ground	
20	ORX0-	Odd pixel, negative LVDS differential data input, channel 0	
21	ORX0+	Odd pixel, positive LVDS differential data input, channel 0	
22	ORX1-	Odd pixel, negative LVDS differential data input, channel 1	
23	ORX1+	Odd pixel, positive LVDS differential data input, channel 1	
24	ORX2-	Odd pixel, negative LVDS differential data input, channel 2	
25	ORX2+	Odd pixel, positive LVDS differential data input, channel 2	
26	OCLK-	Odd pixel, negative LVDS differential clock input	
27	OCLK+	Odd pixel, positive LVDS differential clock input	
28	ORX3-	Odd pixel, negative LVDS differential data input, channel 3	
29	ORX3+	Odd pixel, positive LVDS differential data input, channel 3	
30	GND	Ground	

5.2 TFT LCD MODULE Power input

CNF2 Connector Pin Assignment (2)

Pin	Name	Description	Note
1	VCC	Power input (+18V)	
2	VCC	Power input (+18V)	
3	VCC	Power input (+18V)	
4	VCC	Power input (+18V)	
5	VCC	Power input (+18V)	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	No Connection	(4)
12	NC	No Connection	
13	NC	No Connection	
14	NC	No Connection	
15	NC	No Connection	

Note (1) CNF1 Connector part no.: FI-X30SSL-HF (JAE) or equivalent.

Note (2) CNF2 Connector part no.: 53261-1560 (Molex) or equivalent.

Note (3) Low : normal display (default), High : display with 180 degree rotation

Note (4) Reserved for internal use. Please leave it open.

Note (5) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL2	ODSEL1	Note
L	L	Lookup table was optimized for 60 Hz frame rate.
L	H	Lookup table was optimized for 50 Hz frame rate.
H	L	Reserved. Do not use.
H	H	Reserved. Do not use.

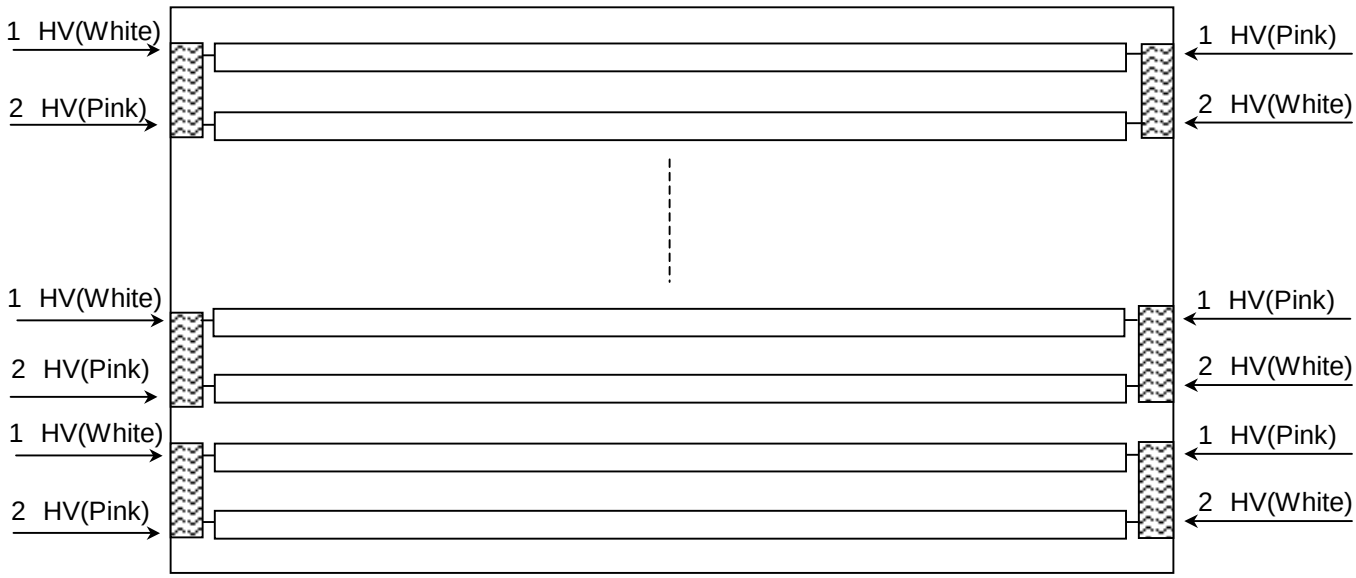
5.3 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN4-CN27: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST. The mating header on inverter part number is SM02(12.0)B-BHS-1-TB(LF).



5.4 INVERTER UNIT

CN1-CN2 (Header):S12B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+120V_{DC} power input
2		
3		
4	NC	NC
5		
6	GND	GND
7		
8		
9		
10		
11	V_{AUX}	+18V_{DC}
12		

CN3 (Header): S10B-PH-SM3-TB (D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	GND	GND
2		
3		
4	NC	NC
5	IG	Inverter Good Signal
6	GND	GND
7	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
8	E_PWM	External PWM control signal E_PWM should be connected to ground when internal PWM was selected (SEL = low).
9	I_PWM	Internal PWM control signal I_PWM should be connected to ground when external PWM was selected (SEL = high).
10	BLON	Backlight on/off control

CN4-CN27 (Header): SM02(12.0)B-BHS-1-TB (LF)(JST) or equivalent

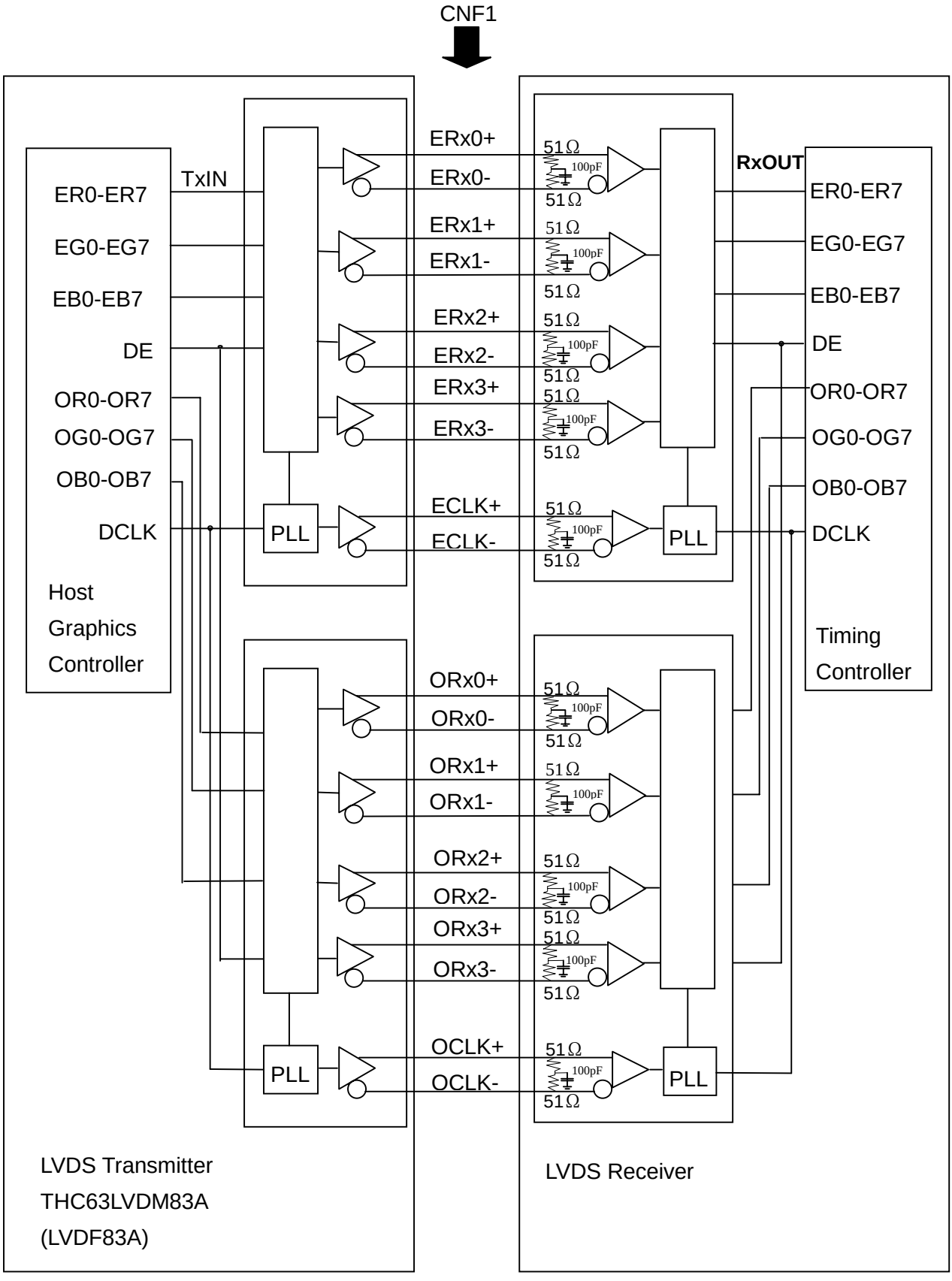
Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN28-CN31 (Header): AL7204-A0G1Z(PTWO) or equivalent

Pin No.	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board
11		Board to Board
12		Board to Board
13		Board to Board
14		Board to Board
15		Board to Board
16		Board to Board
17		Board to Board
18		Board to Board
19		Board to Board
20		Board to Board

Note (1) Floating of any control signal is not allowed.

5.5 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7 : Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is even pixel and the second pixel is odd pixel.

5.6 LVDS INTERFACE

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT
		PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	
24bit	R0	51	TxIN0			27	Rx OUT0	R0
	R1	52	TxIN1			29	Rx OUT1	R1
	R2	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2
	R3	55	TxIN3			32	Rx OUT3	R3
	R4	56	TxIN4			33	Rx OUT4	R4
	R5	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5
	G0	4	TxIN7			37	Rx OUT7	G0
	G1	6	TxIN8			38	Rx OUT8	G1
	G2	7	TxIN9			39	Rx OUT9	G2
	G3	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3
	G4	12	TxIN13			45	Rx OUT13	G4
	G5	14	TxIN14			46	Rx OUT14	G5
	B0	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0
	B1	19	TxIN18			51	Rx OUT18	B1
	B2	20	TxIN19			53	Rx OUT19	B2
	B3	22	TxIN20			54	Rx OUT20	B3
	B4	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4
	B5	24	TxIN22			1	Rx OUT22	B5
	DE	30	TxIN26			6	Rx OUT26	DE
	R6	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6
	R7	2	TxIN5			34	Rx OUT5	R7
	G6	8	TxIN10			41	Rx OUT10	G6
	G7	10	TxIN11			42	Rx OUT11	G7
	B6	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6
	B7	18	TxIN17			50	Rx OUT17	B7
	RSVD 1	25	TxIN23			2	Rx OUT23	Not connect
	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	Not connect
	RSVD 3	28	TxIN25			5	Rx OUT25	Not connect
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes (1) RSVD(reserved)pins on the transmitter shall be “H” or “L”.

5.7 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

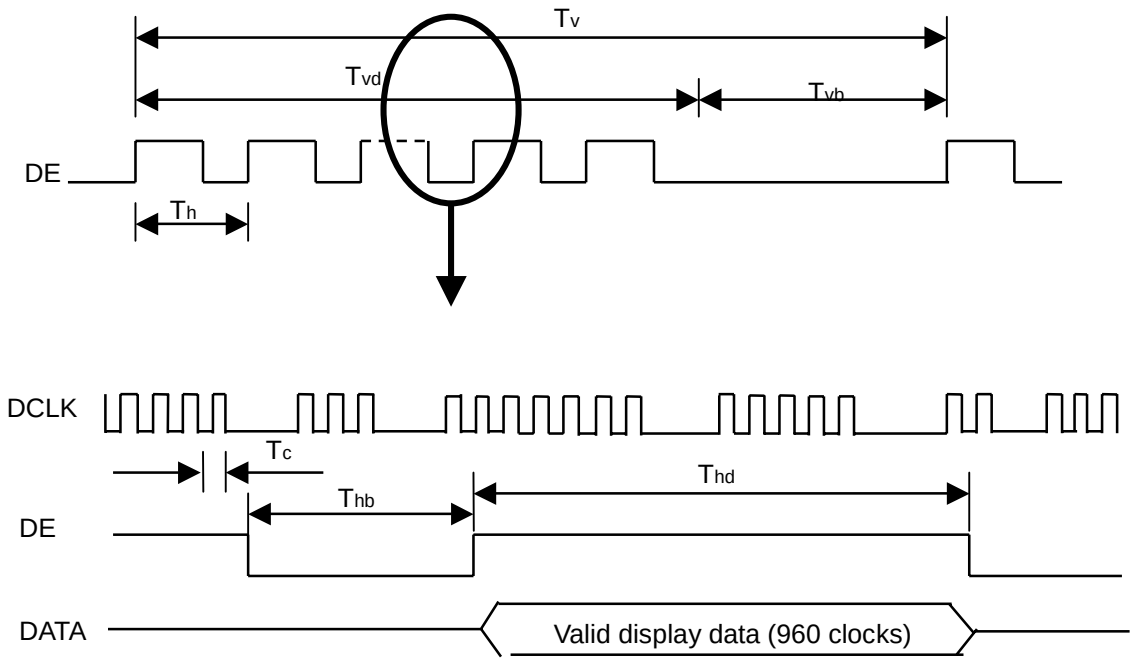
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	80	MHZ	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(2)
		Fr6	57	60	63	Hz	(3)
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	2100	2200	2300	Tc	Th=Thd+Thb
	Display	Thd	1920	1920	1920	Tc	-
	Blank	Thb	180	280	380	Tc	-

Note (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

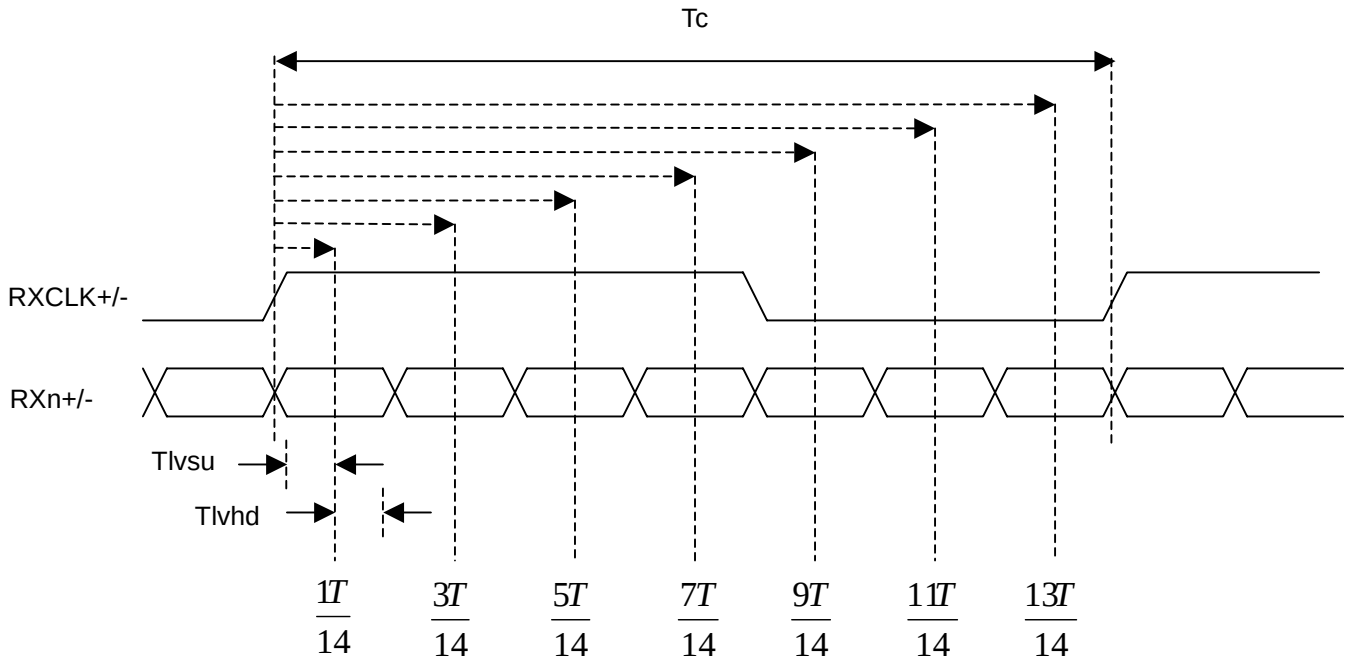
Note (2) (ODSEL2, ODSEL1) = (L,H). Please refer to 5.1 for detail information.

Note (3) (ODSEL2, ODSEL1) = (L,L). Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM

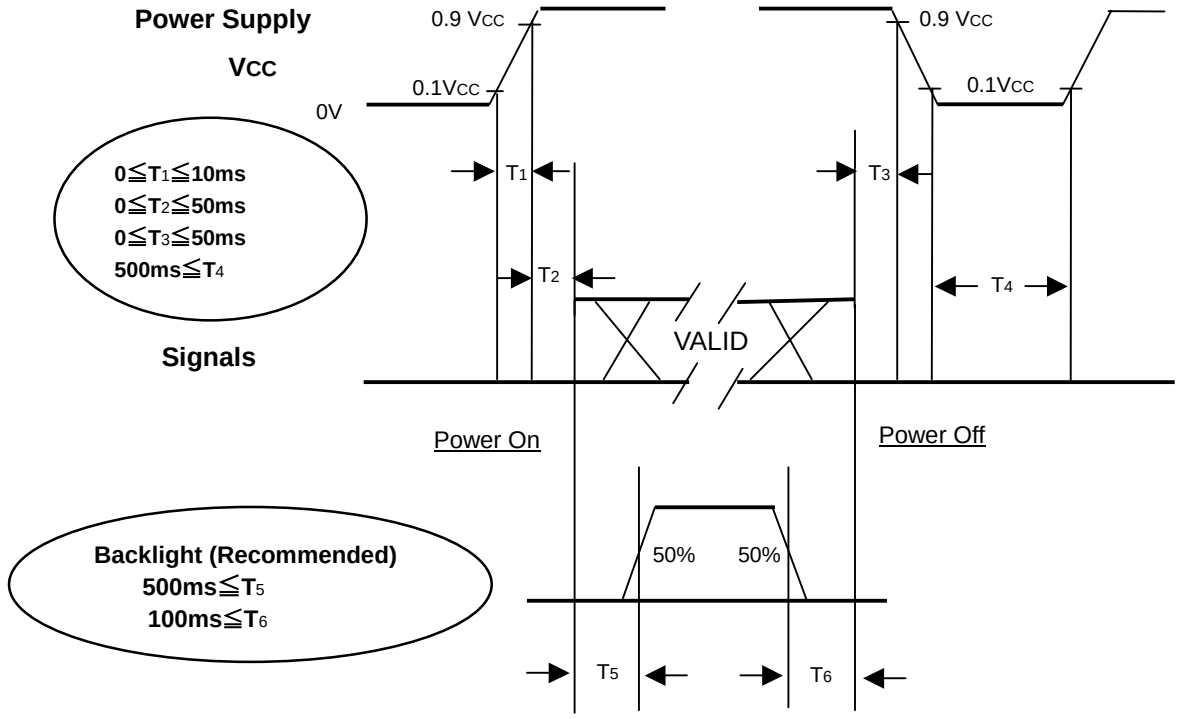


LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	18	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	4.7±0.5	mA
Oscillating Frequency (Inverter)	F_L	50±3	KHz
Frame Rate	Fr	60	Hz

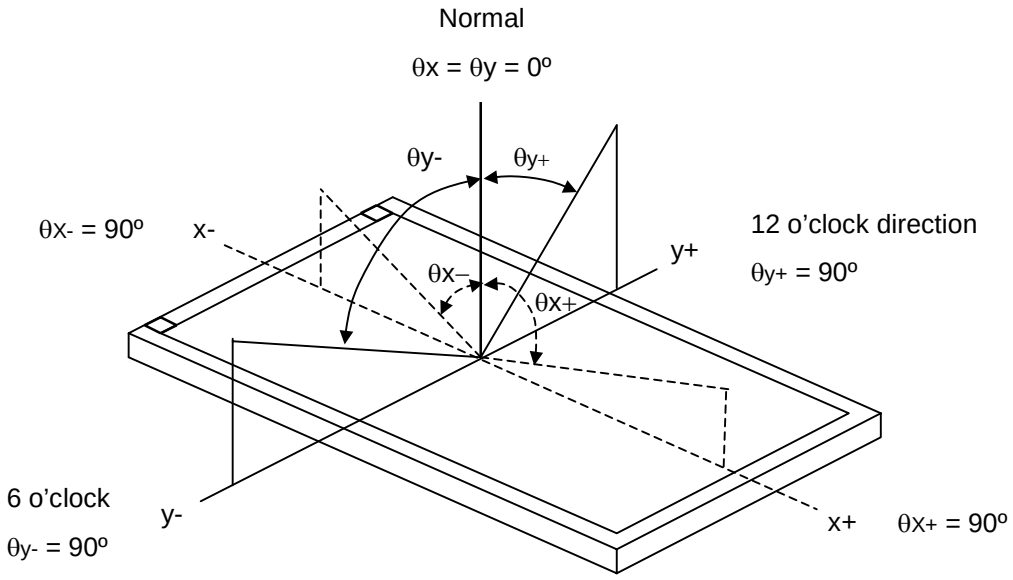
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	-	(800)	-	-	Note (2)
Response Time		Gray to gray		-	(8)	(12)	ms	Note (3)
				-				
				-				
Center Luminance of White		L_C		-	(550)	-	cd/m^2	Note (4)
White Variation		δW		-	-	(1.3)	-	Note (7)
Cross Talk		CT		-	-	(4)	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	(0.651)	Typ. +0.03	-	Note (6)
		Ry			(0.330)		-	
	Green	Gx			(0.275)		-	
		Gy			(0.596)		-	
	Blue	Bx			(0.142)		-	
		By			(0.067)		-	
	White	Wx			0.285		-	-
		Wy			0.293		-	
	Color Gamut	C.G		(72)	(75)	-	%	-
Viewing Angle	Horizontal	θ_x+	CR≥20	(80)	(88)	-	Deg.	Note(1)
		θ_x-		(80)	(88)	-		
	Vertical	θ_Y+		(80)	(88)	-		
		θ_Y-		(80)	(88)	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

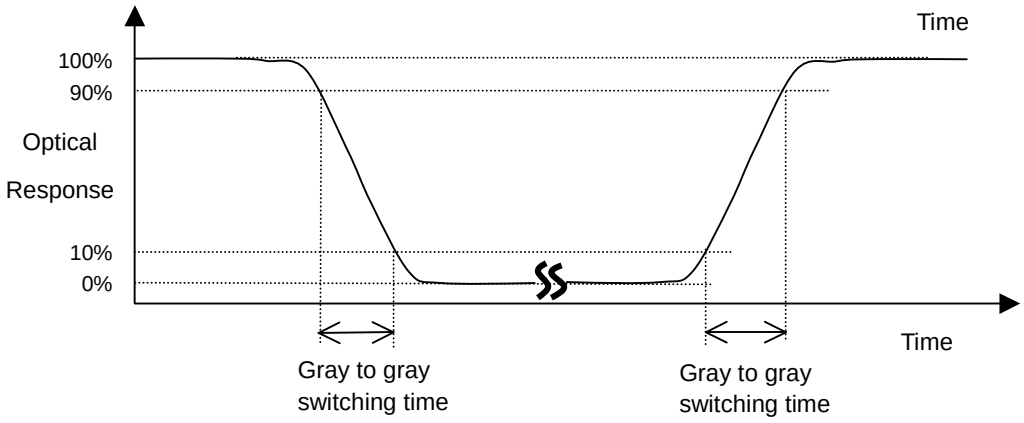
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time:



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

L (x) is corresponding to the luminance of the point X at the figure in Note (7).

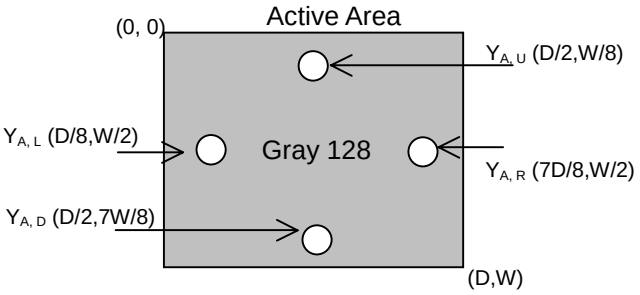
Note (5) Definition of Cross Talk (CT):

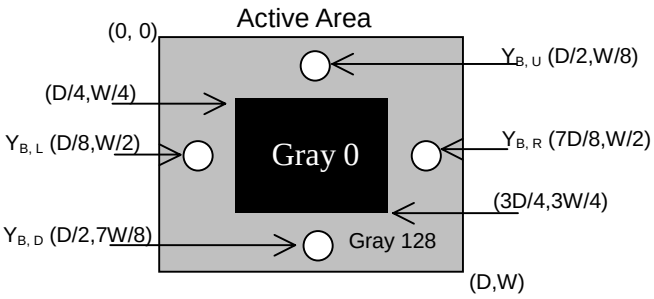
$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

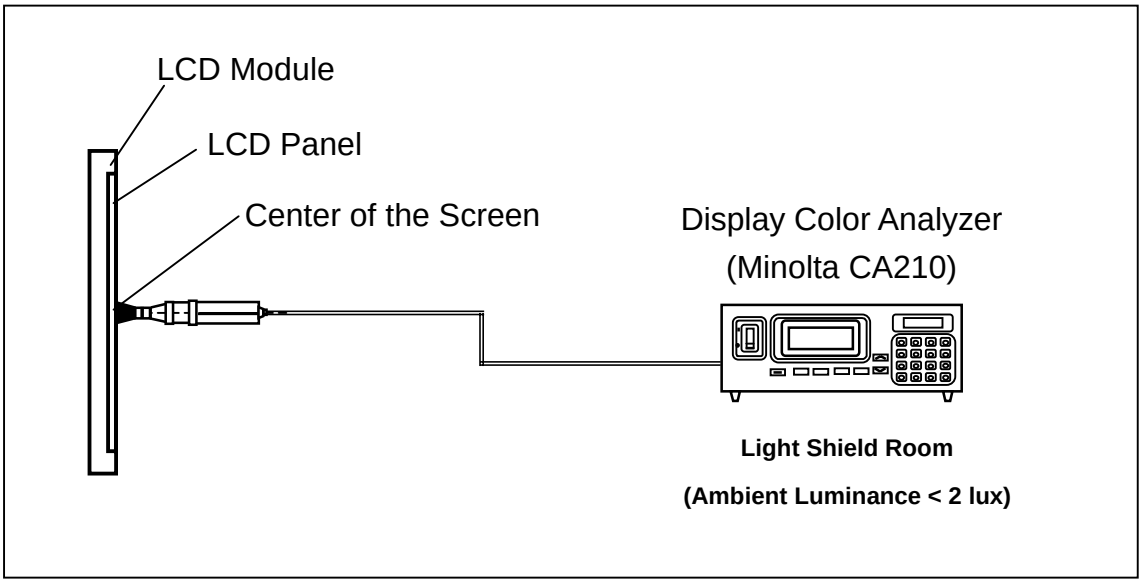
Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)





Note (6) Measurement Setup:

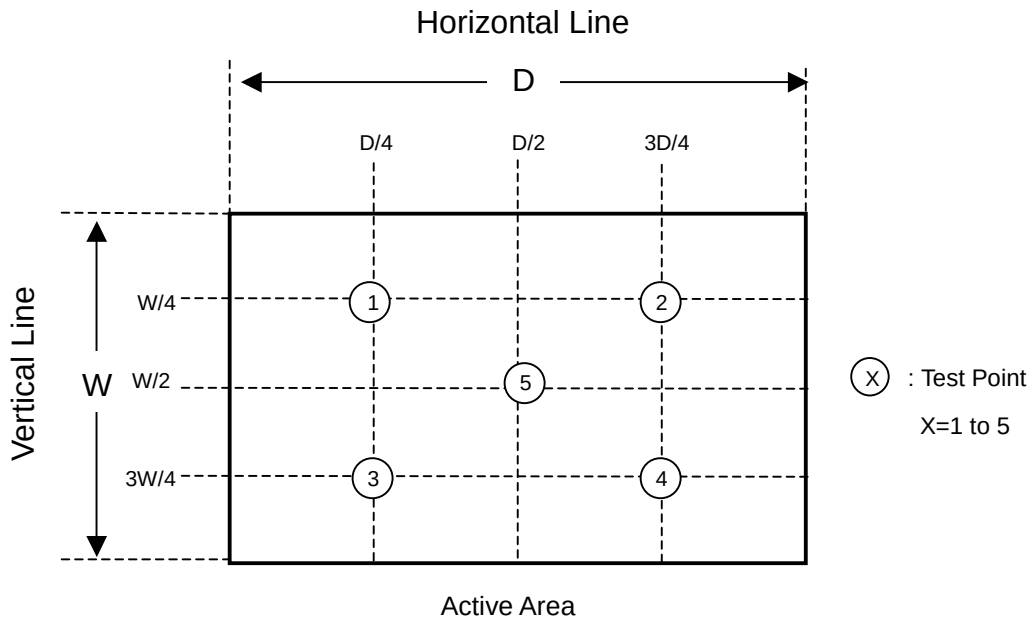
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

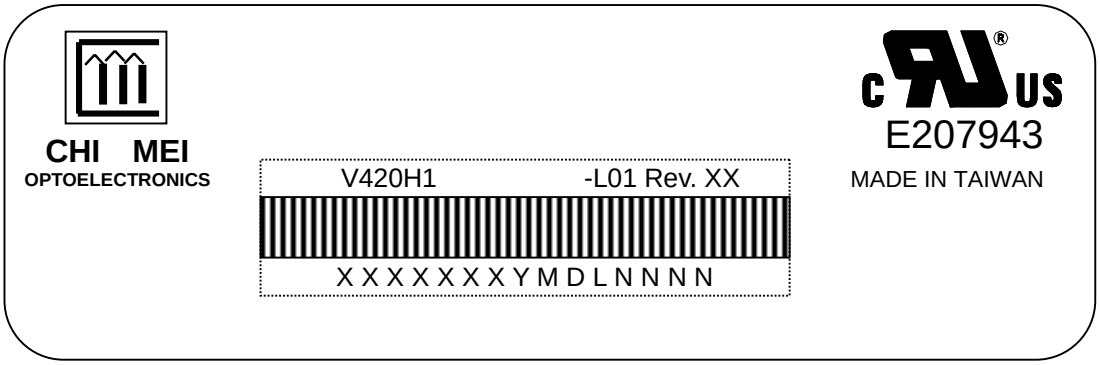
(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

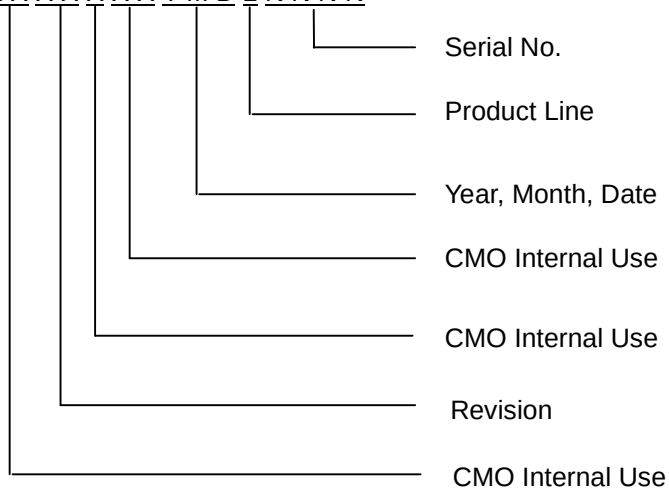
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V420H1-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKING SPECIFICATIONS

(1) 3 LCD TV modules / 1 Box

(2) Box dimensions : 1086(L) X 356 (W) X 715 (H)

(3) Weight : approximately 40Kg (3 modules per box)

10.2 PACKING METHOD

Figures 10-1 and 10-2 are the packing method

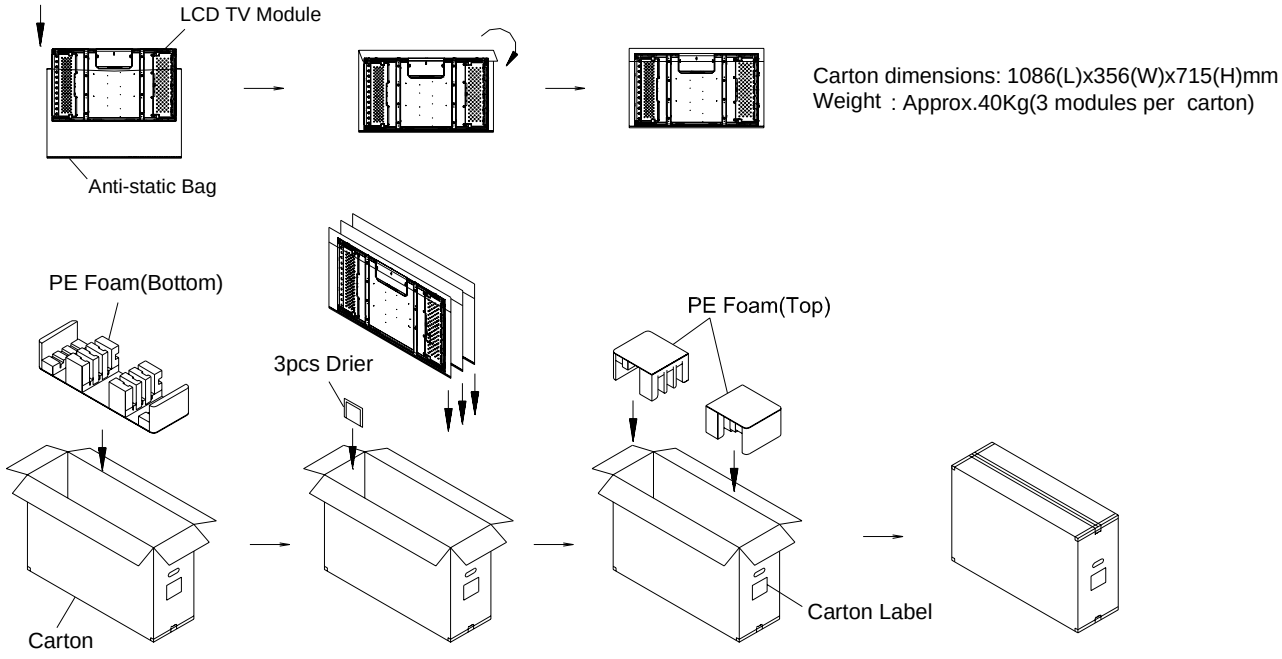


Figure.10-1 packing method

Corner Protector:L1420*50mm*50mm
Pallet:L1100*W1100*H145mm
Corrugated Fiberboard:L1100*W1100mm
Pallet Stack:L1100*W1100*H1575mm
Gross:257kg

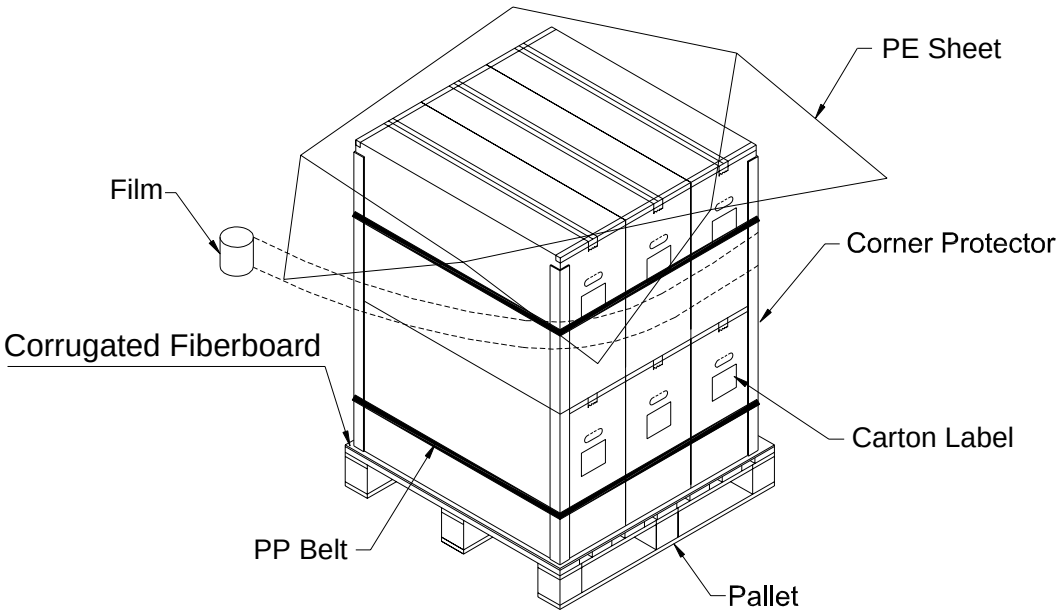


Figure. 10-2 Packing method

11. MECHANICALCHARACTERISTIC