



STD78N75F4 STP78N75F4

N-channel 75 V, 0.008 Ω , 78 A TO-220, DPAK
STripFET™ DeepGATE™ Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STD78N75F4	75 V	< 0.011 Ω	70 A
STP78N75F4	75 V	< 0.011 Ω	78 A

- N-channel enhancement mode
- 100% avalanche rated
- Low gate charge
- Very low on-resistance

Application

- Switching applications

Description

This STripFET™ DeepGATE™ Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state Resistance, with a new gate structure, providing superior switching performances.

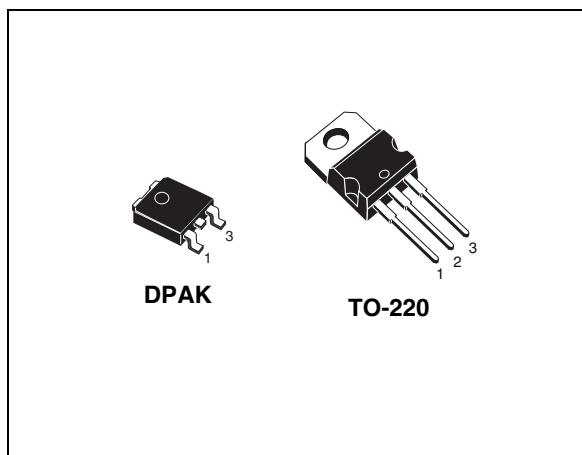
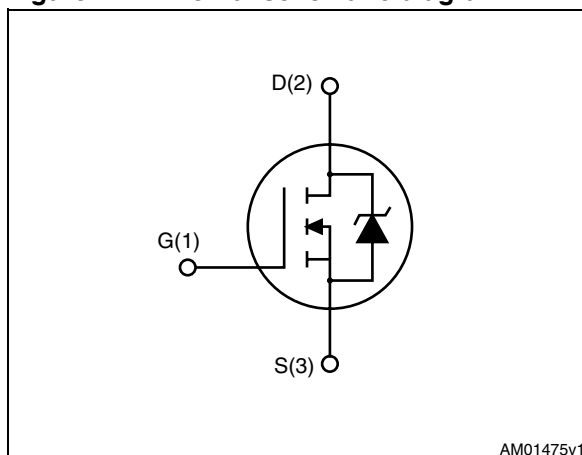


Figure 1. Internal schematic diagram



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Table 1. Device summary

Order codes	Marking	Package	Packaging
STD78N75F4	78N75F4	DPAK	Tape and reel
STP78N75F4	78N75F4	TO-220	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
3	Test circuit	6
4	Package mechanical data	7
5	Packaging mechanical data	10
6	Revision history	11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	DPAK	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	75		V
V_{GS}	Gate-source voltage	± 20		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	78	70	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	55	50	A
$I_{DM}^{(1)}$	Drain current (pulsed)	312	280	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	125	W
	Derating factor	1	0.83	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	TBD		mJ
T_{stg}	Storage temperature	– 55 to 175		$^\circ\text{C}$
T_j	Operating junction temperature			

1. Pulse width limited by safe operating area
2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 32.5\text{ A}$, $V_{DD} = 45\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1	1.2	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max		50	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300		$^\circ\text{C}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	75			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 37.5\text{ A}$		0.008	0.011	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			5130		pF
C_{oss}	Output capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	415	-	pF
C_{rss}	Reverse transfer capacitance			20		pF
Q_g	Total gate charge	$V_{DD} = 60\text{ V}$, $I_D = 78\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 3)		90		nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge			TBD		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 37.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)		TBD		ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off-delay time	$V_{DD} = 50\text{ V}$, $I_D = 37.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)		TBD		ns
t_f	Fall time		-	TBD	-	ns

Table 7. Source drain diode

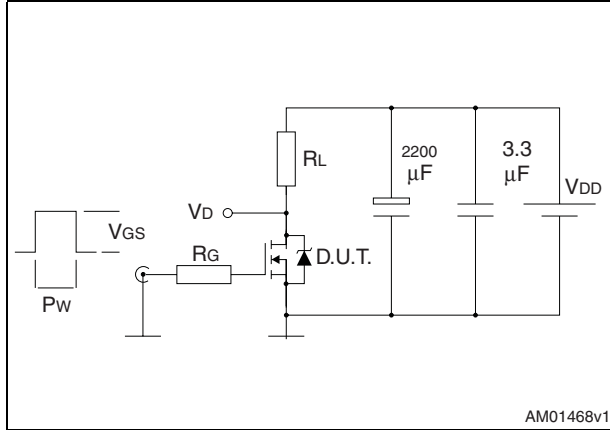
Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current	TO-220	-		78	A
		DPAK	-		70	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	TO-220	-		312	A
		DPAK	-		280	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 78 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 78 \text{ A}, V_{DD} = 25 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 4)	-	TBD		ns
Q_{rr}	Reverse recovery charge					nC
I_{RRM}	Reverse recovery current					A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Test circuit

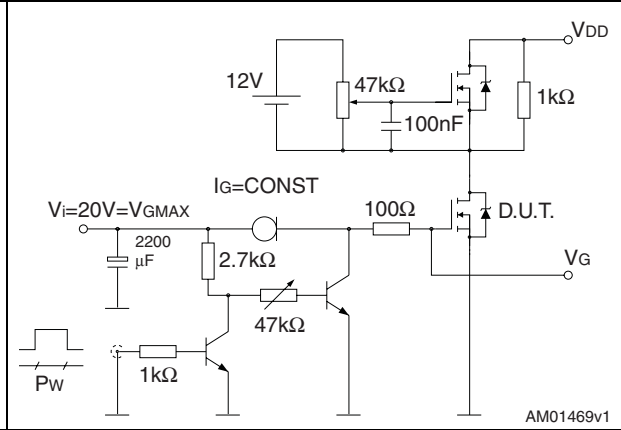
3 Test circuit

Figure 2. Switching times test circuit for resistive load



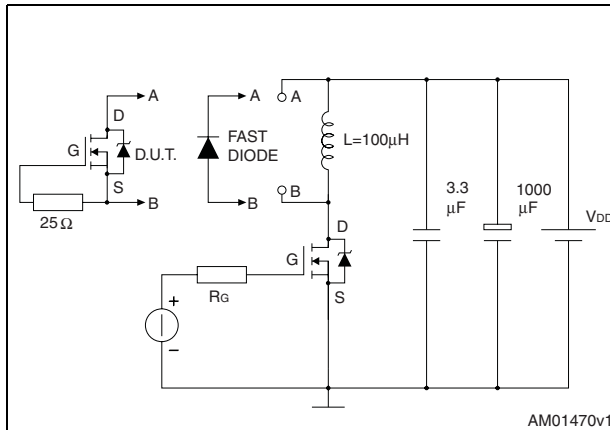
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Figure 3. Gate charge test circuit



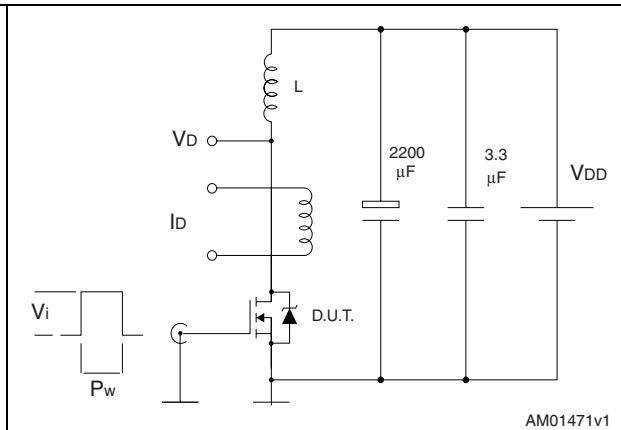
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Figure 4. Test circuit for inductive load switching and diode recovery times



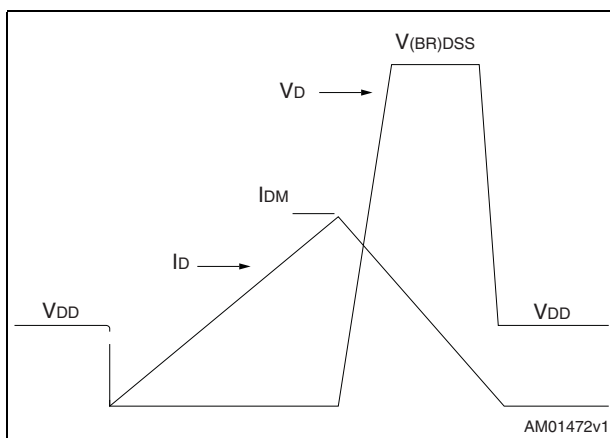
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Figure 5. Unclamped inductive load test circuit



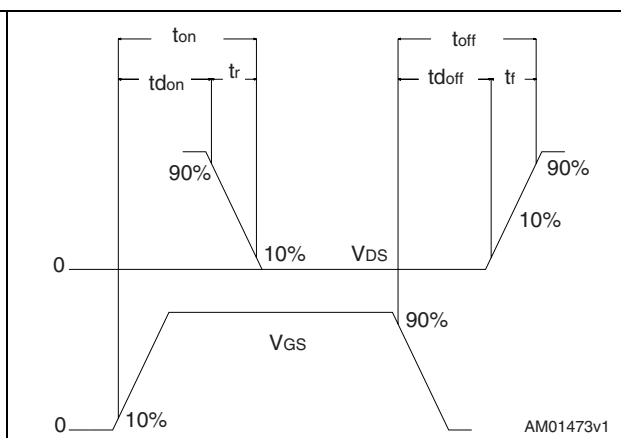
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Figure 6. Unclamped inductive waveform



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Figure 7. Switching time waveform



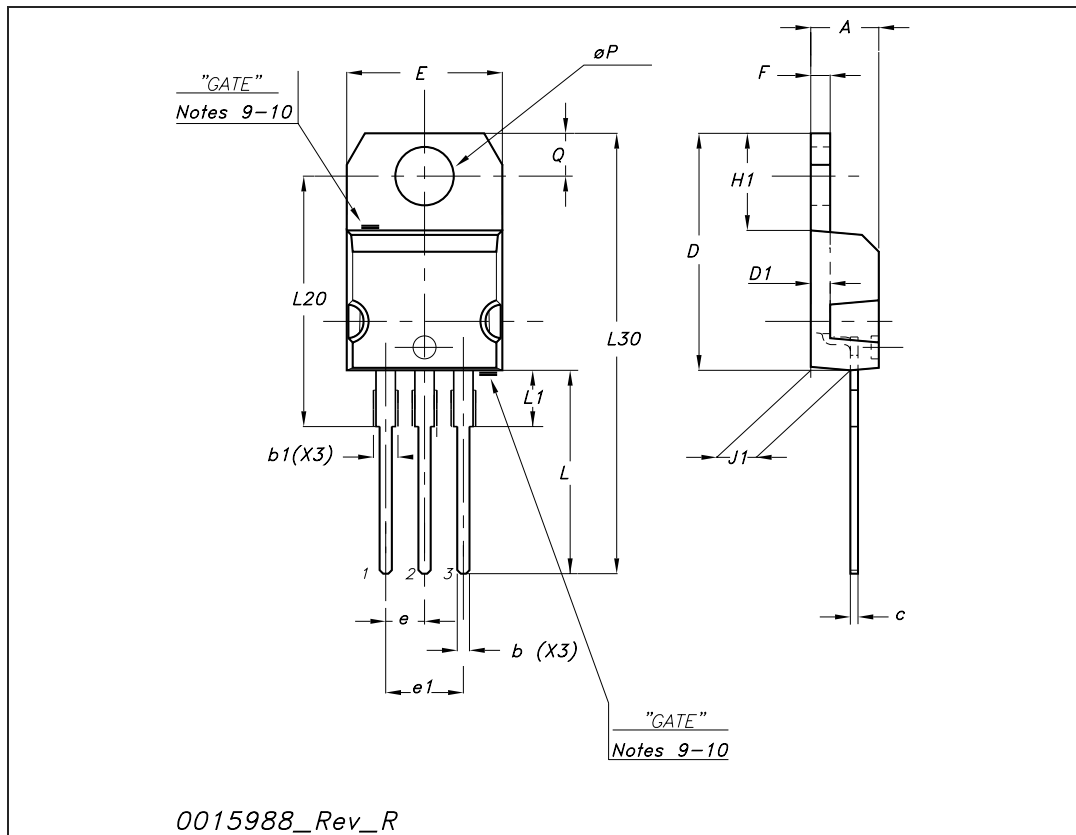
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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

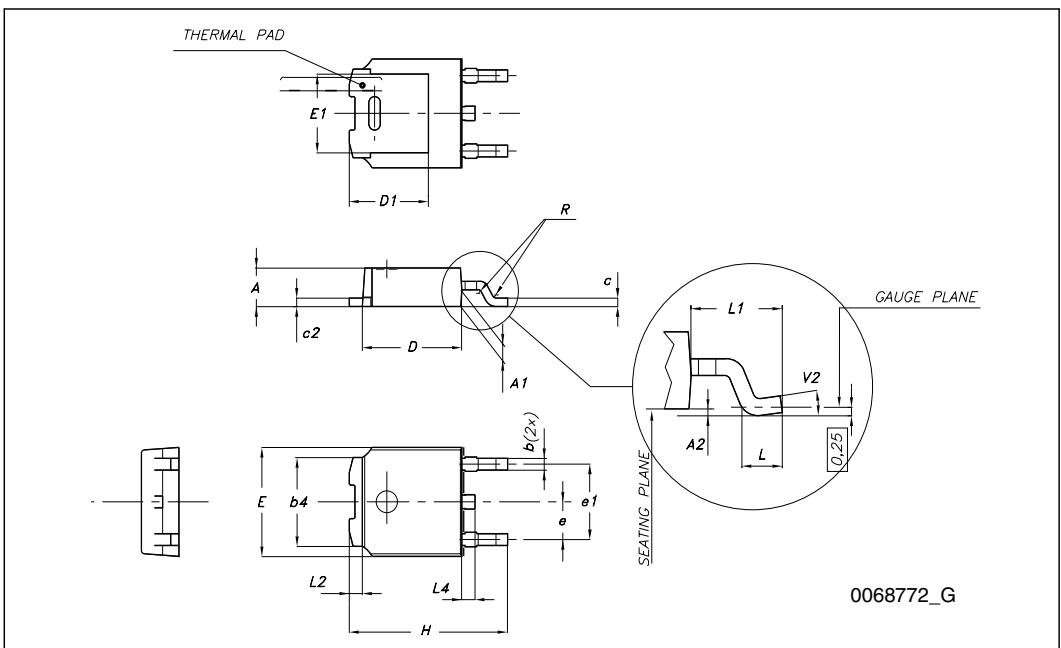
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



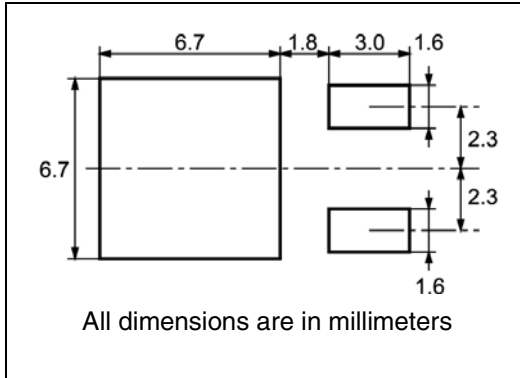
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
12-May-2009	1	First release

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